Low Power High Efficiency Excess-Loop-Delay Compensation Techniques in Continuous-Time Delta-Sigma Modulators

by

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Approved by _____
Supervisor

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Co-Supervisor

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ABSTRACT

Because of the convenient and powerful function of mobile telecommunication devices, the demand of it is tremendously increased in the whole world wide nowadays. As the connection element between the analog and digital signal world, the modulators are obligatory. On account of the merits of low power consumption, small silicon area, large signal bandwidth, and also inherent anti-aliasing function, the Continuous-Time (CT) ΣΔ modulator has been extensively used in wideband telecommunication systems.

However, the performance of CT ΣΔ modulators is restricted by the non-idealities of practical circuit elements. Excess Loop Delay (ELD) is one of the dominant effects induces the error in the Transfer Function, and then reduces the performance of the CT ΣΔ modulator. Even worse, the error may cause the instability of the modulator.

This thesis proposes three different techniques with the properties of low-power and high-efficiency to compensate the ELD effect of CT ΣΔ modulators. The first technique is based on the Gm-C loop filter and with one passive resister added. After verifying it in 65nm CMOS technique, the proposed technique can reduce the power consumption up to 32% and compensate up to half of clock cycle delay amount. The second technique employs digital logic elements and an RC feedback network for the active-RC loop filter to track the amount of ELD up to half of clock cycle synchronously on a real-time modulator, and then compensate it. It is verified in 65nm CMOS process, compare with the traditional technique, power reduced from 6.5mW to 5.45mw. And the third technique is for hybrid active-passive integrators. The efficiency of the proposed compensation techniques are implemented in the designed modulators and verified by the transistor-level simulation as well. This technique can compensate the delay amount up to one clock cycle and reduced more than half of power dissipation. Compare with the traditional techniques, these three techniques are quite low power dissipation and can compensate the ELD effect effectively.

KEY WORDS

Continuous-Time Sigma-Delta Modulator

Excess-Loop-Delay Effect

Proportional-Integrating Excess-Loop-Delay Compensation

Passive Excess-Loop-Delay Compensation Technique

Excess-Loop-Delay Tracking Compensation Technique

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Last, I express my deepest gratitude to my family for their loves, kindness encouragement and support. Finally, I express sincerely my gratitude once more to all of the people who have contributed to this work.

To my family

LIST OF ABBREVIATIONS

ADC	Analog to Digital Convertor
AMS	Analog Mixed-Signal
AP	Active-Passive
CC	Compensation Component
CIFB	Chain of Integrators with distributed FeedBack
CIFF	Chain of Integrators with weighted Feed-Forward
CLG	Control Logic Generator
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DFF	D-Flip-Flop
DSP	Digital Signal Processor
DT	Discrete-Time
DWA	Data Weighted Averaging
ELD	Excess-Loop Delay
GSM	Global System for Mobile
HRZ	Half-Return-to-Zero
HSPA	High Speed Packet Access
IIT	Impulse Invariant Transform
IBN	In-Band-Noise
MASH	Multi-stAge noise SHaping
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
OSR	OverSampling Ratio
Op-Amp	Operational Amplifier
PA	Power Amplifier

PLL	Phase Lock Loop
PM	Power Management
PP	Pulse-Position
PS	Pulse Shape
PSD	Power Spectral Density
PW	Pulse-Width
RZ	Return-to-Zero
SNDR	Signal-to-Noise-and-Distortion-Ratio
SNR	Signal-to-Noise Ratio
STF	Signal Transfer Function
TD-SCDMA	Time Division Synchronous Code Division Multiple Access
UMTS	Universal Mobile Telecommunication System
VCO	Voltage Controlled Oscillator
WCDMA	Wideband Code Division Multiple Access
ZCD	Zero-Crossing Detector
ΣΔ	Sigma-Delta
3G	3rdGeneration

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND AND APPLICATION

1.1.1 3G WIRELESS COMMUNICATIONS

Nowadays, the wireless communication device has become one of the essential components in our modern life. Mobile phone plays the important role in our daily life and it has evolved to the 3rd Generation (3G) technology. 3G wireless communication technology is the most dominant technique in the global handset market presently, and the following Fig.1.1depicts the estimation of wireless communication technology [1].

According to the estimation in the following Fig.1.1, 3G wireless communication technologies will occupy up to 80% of handset market till 2020 and the subscribers of the 3G technology is still increasing significantly in the coming decade.

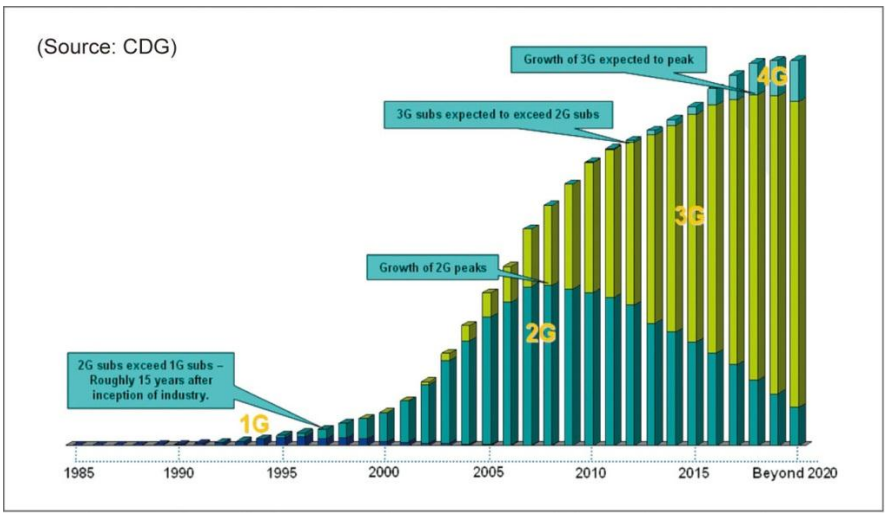

Fig.1.1Estimation of wireless communication technology

More and more people choose 3G mobile phone rather than other generations. In contrast to the previous generations of communication technology, the subscribers nowadays have higher requirement for their mobile phones, they want their handset contains more and more functions. For communication point of view, they want not only to make audio phone calls but also the real-time visual calls, these demands are even stronger for subscribers are in two different places, as shown in the following Fig.1.2 [2]. This type of real-time visual phone calls makes the subscribers feel that they are talking face-to-face and they are becoming closer. Besides the visual phone calls, consumers hope that they can deal with their email on-time. Hence, the mobile phones with the function that can process the email fast and efficiently have more dominance in the market than those do not have this function. In general, the consumers hope their handset has more functions, can be used for a longer time and the size of the handset is as small as possible.

Fig.1.2 Function of the 3G mobile phone.

After the introduction about the advantages of the 3G communication technology, the infrastructure of the 2G and 3G communication technologies will be depicted briefly. Similar with GSM (Global System for Mobile Communications) is the standard for the 2G communication technology; the 3G technology has its own standards as well. Based on the GSM standard for the mobile cellular system, Universal Mobile Telecommunication System (UMTS) is the third generation system, and there are three main typical standards: WCDMA (Wideband Code Division Multiple Access) which is the original and most commonly used radio interface, TD-SCDMA (Time Division Synchronous Code Division Multiple Access) which is only used in China and the High Speed Packet Access (HSPA) [3]-[9]. According to the knowledge of the main categories of the 3G technology and the development trends of telecommunication technology, the investigation of mobile infrastructure in the worldwide is depicted as below [10].

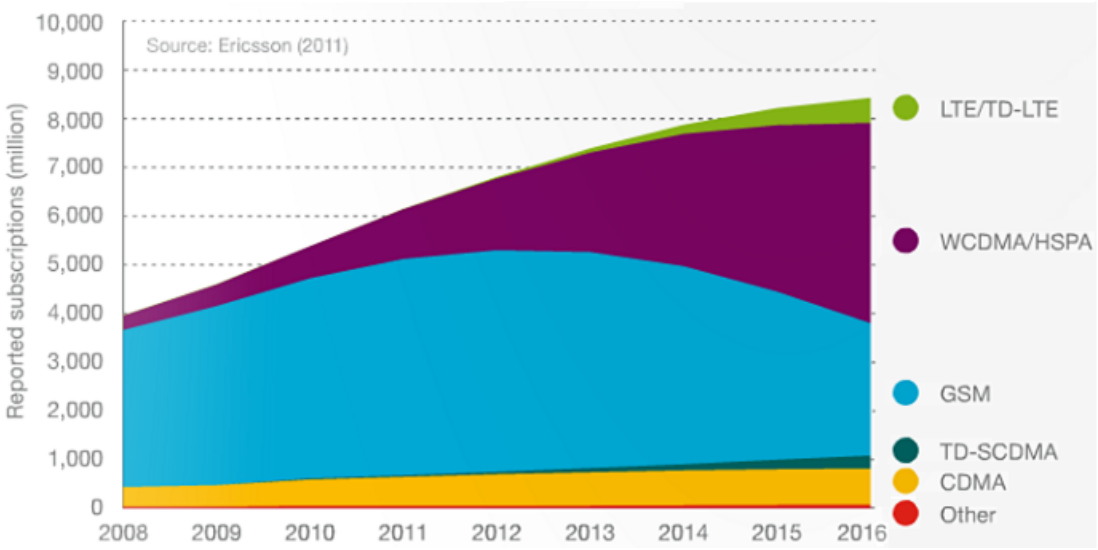

Fig.1.3 The investigation of mobile infrastructure in the worldwide.

The figure describes that the 2G telecommunication technology occupies more than half of the mobile market nowadays. However, this situation will change within the coming several years, the occupancy factor of GSM will decrease and the subscribers of the 3G technology will increase significantly (mainly with the access of WCDMA/ HSPA, and TD-SCDMA will also increase).

Fig.1.1and Fig.1.3gives the large demand of 3G communication technology in the coming several years, this brings huge revenue in the worldwide; the revenue nowadays and the forecasting based on these data in the coming years is in the following figure[10].

The following forecasting figure depicts that the revenue of the 3G mobile phone will reach to about 900 billion U.S dollars in 2014; hence, there is large revenue to develop the 3G communication technology.

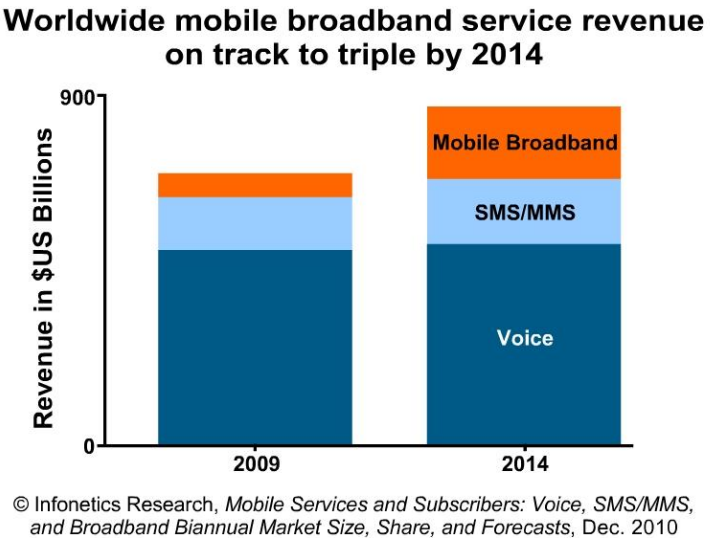

Fig.1.4 Worldwide mobile broadband service revenue forecasting.

1.1.2 APPLICATION OF ADCS IN 3G WCDMA RECEIVER

As introduced in the previous parts, the 3G telecommunication technology has high development potential and large market demands, it develops very rapidly and WCDMA is the most commonly used access of it. For the wireless telecommunication technology, the Analog to Digital Converter (ADC) which connects the analog world (signals in our real-world are in analog mode) and the digital world is essential. The following figure gives the circuit functions of a typical mobile communication system [11].

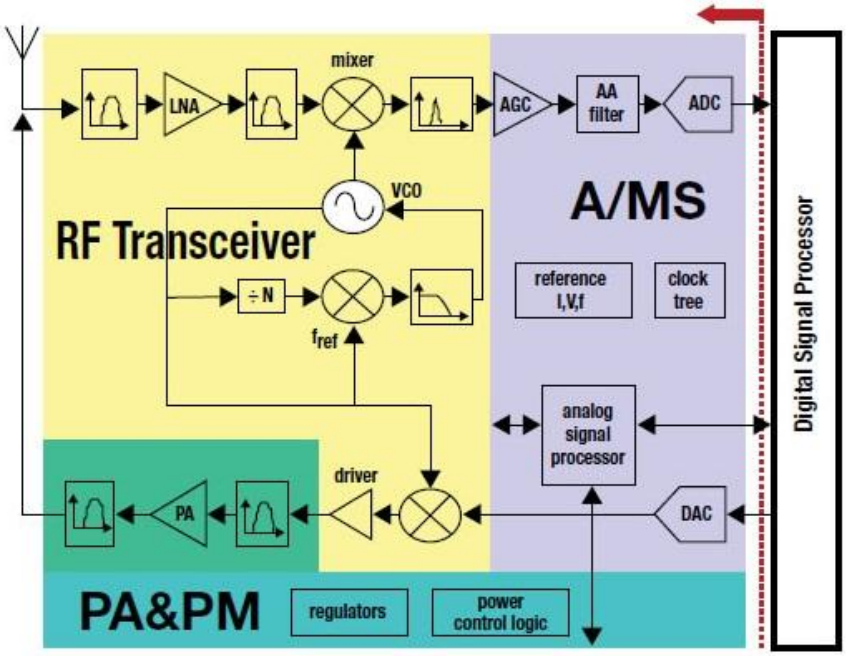

Fig.1.5 The circuit functions of a typical mobile communication system.

In the above figure, the four basic circuit functions are Power Management (PM), Power Amplifier (PA), Radio Frequency (RF) transceiver and, Analog Mixed-Signal (AMS), which interfaces with the Digital Signal Processor (DSP). As the rapidly development of the wireless communication, the segment ADC also should be well designed to satisfied the high performance requirements. The consumers of 3G communication technology require the handset to make calls with high quality, the display of the handset should have high resolution, and the processing speed of it also should be fast. There are lots of ADC's structures, and the type suitable for the wireless broadband communication receivers is shown as below[12].

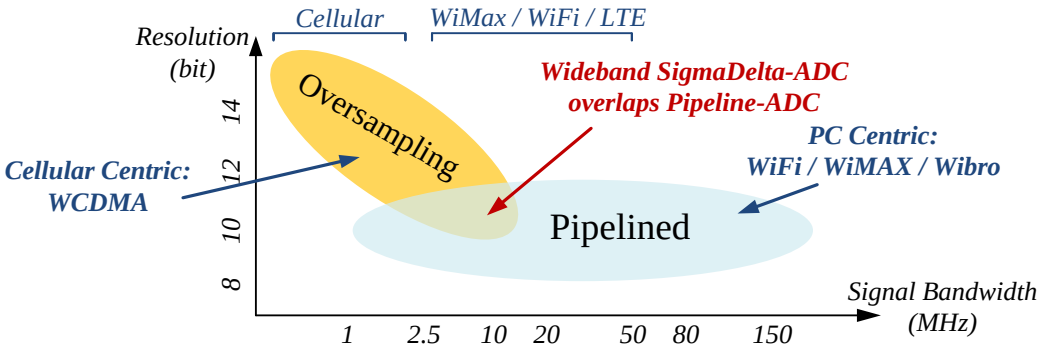

Fig.1.6 The application range of over-sampling Sigma Delta and Pipeline ADC.

According to the above figure and since the requirements for the 3G WCDMA receivers are high resolution, low power consumption, and small silicon area, Sigma Delta (ΣΔ) modulator is the most suitable option. Besides, ΣΔ modulator employs the over-sampling technique and it is anti-aliasing with low power dissipation. There are two structures of the ΣΔ modulator, one is Discrete-Time (DT) ΣΔ modulator and the other is the Continuous-Time (CT). Compare these two different modulators, CT one has the benefits of lower power consumption, lower switch noise, higher bandwidth and smaller silicon area. Besides these benefits, CT ΣΔ modulator is implicit anti-aliasing which reduces the anti-aliasing block exists in the DT ΣΔ modulator, therefore, the power consumption of CT ΣΔ modulator can be further reduced and it is more suitable and widely used in the wireless telecommunication technology.

1.2 RESEARCH MOTIVATION

As discussed before, the CT ΣΔ modulator is widely used in the wireless telecommunication technology because of the benefits of low power dissipation, small silicon area, and broad bandwidth. However, in the practical implementation, there are some non-idealities which will reduce the performance significantly.

One significant non-ideality called Excess Loop Delay (ELD), which is due to the non-zero switching time of the transistors in the quantizer and DAC. It is

ineluctable in the system and due to this ELD, the performance will be reduced. Hence, the study and analysis of ELD effect is essential and techniques to compensate the effect of ELD are important and necessary as well. Refer to the existed literatures, there are compensation techniques based on setting the identical of the Noise Transfer Function (NTF) in different conditions. And most of the compensation techniques such as the traditional compensation technique, it requires the additional adder and feedback path in front of the quantizer. This technique increases the power consumption and makes the system more complicated. And most of the compensation techniques are based on the certain amount of the loop delay, which means that the delay amount is assumed to be a fixed value and then according to the identical of the NTFs, the ELD effect will be compensated. Hence, the compensation methodology that can track the delay amount due to the real-time modulator has very sharp advantage, and on the other hand, the power consumption also should be as low as possible. This leads to the development of the passive element to compensate the ELD effect.

In this thesis, the novel proposed compensation techniques will be introduced. And the aims of them are target to the low power consumption and can compensate the ELD effect efficiency. The first idea is a passive ELD compensation technique for the Gm.-C based integrator in the CT ΣΔ modulator; after applying this technique in 65nm CMOS process, power reduction is up to 32% and delay amount up to half of clock cycle can be compensated. And the second idea is an ELD tracking compensation technique which can track the ELD up to half of clock cycle in the real-time modulator and the circuit implementation of this technique is simple, the power is reduced from 6.5mW to 5.45mW after verification is 65nm CMOS process. The third idea is the compensation technique for the hybrid Active-Passive CT ΣΔ modulator, with the help of this technique, the delay amount up to one of the clock cycle can be compensated. All these three compensation techniques can reduce more power dissipation and compensate the delay effect effectively with the traditional compensation techniques in comparison. And the thereafter parts of the thesis will introduce them in detail.

1.3 THESIS ORGANIZATION

This thesis covers totally 8 chapters. For **this chapter**, it takes a brief glance at the background of 3G wireless telecommunication and the development potential of it. And then according to the requirements of the ADCs in WCDMA, the CTΔΣ modulator is the most suitable option. But the non-ideality ELD which will reduce the performance significantly, hence the analysis of the ELD effect and the compensation methods of it are essential.

Chapter 2 introduces the elementary of ΔΣ modulator starting from the quantization and over-sampling. And then the structure of it is depicted, in order to get the higher resolution and more accuracy, higher order and more complicated structure are expressed.

Chapter 3 focuses on the CT ΔΣ modulator because of its lower power dissipation small silicon area and anti-aliasing filter function. And in traditional, the CT ΔΣ modulator is got from the equivalent DT case. Hence, the transfer methods between the DT and CT ΔΣ modulator are described. There are some CT filters can be implemented in CT ΔΣ modulator such as the active RC integrator, Gm.-C integrator and so forth, different types of filters have different properties and they are employed in different conditions. And the final part of this chapter is the non-idealities issues of practical CT ΔΣ modulator which will make the performance of it reduce sharply.

Chapter 4 focuses on the non-ideality ELD effect in the classical active RC integrator. It is one of the most dominant non-idealities in the CT ΔΣ modulator. The ELD effects are related with the different DAC feedback waveforms. Since the effect of ELD reduces the performance of the CT ΔΣ modulator so sharply, the compensation techniques to reduce the ELD effect are essential. The existed ELD compensation techniques for the classical active RC integrators are briefly introduced.

Chapter 5 introduces a proposed ELD tracking compensation technique for active RC CT ΔΣ modulators. With the proposed novel method, the delay amount due to the ELD effect can be tracked according to the real-time circuit synchronously.

And at the same time, the lacked or the redundant feedback amount is stored in the RC network. Hence, the redundant or lacked feedback amount will be subtracted or added back to the feedback waveform and make it identical to that of ideal case. Compare with the existed compensation techniques, the novel technique can be implemented easily in the circuit level and can compensate the ELD effect efficiency.

Chapter 6 covers an ELD compensation technique for Gm-C based CT ΔΣ modulators. As mentioned in the previous chapters, the compensation techniques focus on the active RC integrator. However, there are other filters as mentioned in chapter 2. And in order to reduce the power consumption of the modulator, the low power consumption simply structure filter Gm-C filter is now widely used. This chapter introduces the novel compensation technique for the Gm-C filter based CT ΔΣ modulator. By using this compensation technique, the ELD effect in the Gm-C filter based CT ΔΣ modulator can be compensated.

Chapter 7 introduces an ELD compensation technique for CT ΔΣ modulators with hybrid active-passive (AP) loop-filters. Since the loop filter is the dominant power consumption element in the CT ΔΣ modulator, passive RC filter is the passive element which does not dissipate power; at the same time, in order to maintain the high linearity of the modulator, active element also should be used. Therefore, the hybrid AP loop-filter has high potential in the CT ΔΣ modulator to maintain the performance and with low power consumption. This chapter analysis the ELD effect in the modulator with hybrid AP filters, and the classical compensation technique in it is also discussed. However, after discussion we can find that the classical compensation technique cannot be implemented. Therefore, the low power dissipation high efficiency ELD compensation technique in hybrid AP loop filters is necessary. The proposed novel ELD compensation technique is raised, with the technique, there is no additional power consumption and ELD effect can be tolerated up to one clock cycle.

Chapter 8 is the conclusion of the thesis and the future work based on the proposed techniques is described as well.

1.4 STATEMENT OF ORIGINALITY

For this thesis, the main purpose is to develop the novel high efficiency, low power consumption techniques for the significant effect of ELD in the CT ΔΣ modulators. And the research work lead to the following original contributions.

For the first work, it proposed an ELD tracking compensation technique for active RC CT ΔΣ modulators, which can track the delay amount of the real-time circuit and then the lacked or redundant part less than half of the clock cycle due to the ELD will be compensated back easily. It can be implemented in the circuit efficiency and easily.

[1]Chen-Yan Cai, Yang Jiang, Sai-Weng Sin, Seng-Pan U and R.P. Martins, "An ELD Tracking Compensation Technique for Active-RC CT ΣΔ Modulators", *Proc. IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2012.

The second work proposed an ELD compensation technique for Gm-C integrator based CT ΔΣ modulators because the wide implementation of the low power integration Gm-C. And the technique can compensate the delay amount less than half of the clock cycle.

[2]Chen-Yan Cai, Yang Jiang, Sai-Weng Sin, Seng-Pan U and R.P. Martins, "A passive Excess-Loop-Delay compensation technique for Gm-C based continuous-time ΣΔ modulators", *Proc. IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011.

The third work discussed the ELD effect in the CT ΔΣ modulators with hybrid active-passive (AP) loop-filters and the possibilities of implement different compensation techniques in it. With the implementation of certain technique, there is no additional power dissipation and the ELD effect up to one of clock period can be compensated.

[3]Chen-Yan Cai, Yang Jiang, Sai-Weng Sin, Seng-Pan U and R.P. Martins,"Excess-Loop-Delay Compensation Techniques for Hybrid Active Passive

Continuous-Time ΣΔ Modulators", under review with minor revision in the Int. Journal of *"Analog Integrated Circuits and Signal Processing", Springer*.

CHAPTER 2

ELEMENTARY OF ΔΣ MODULATION

2.1 INTRODUCTION

In this chapter, the fundamental principles of the modulator such as the quantization, over-sampling and the ΔΣ modulator will also be introduced. And then the comparisons between some commonly used structures of the ΔΣ modulator such as the second order and higher order modulators, single-bit and multi-bit modulators, and single-stage and multi-stage modulators are introduced as well.

2.2 QUANTIZATION AND OVERSAMPLING

In order to transfer the signal from the analog domain to digital domain, the digital modulations with the both functions to quantize the amplitude and sampling in time are necessary. Comparing these two operations, there will be distortion errors in the operation of quantization and no matter how accuracy of it. Hence, the reduction of the distortion in quantizer is the improvement trends for the analog signal quantizer. The essential of the quantizer in digital modulation is because of the digital signal can just be discrete sets of values but the analog signal can be any values within a certain continuous range. And the number of codes depicts the analog signal decides the precision of the digital signal [13].

Quantizer or ADC is the building block designed to perform quantization. There are always several quantization intervals in the signal dynamic range and the corresponding analog amplitude value is always the mid-point of the quantization interval. Since the quantization is usually uniform, the quantization step which

describes the differences between two adjacent quantization intervals is fixed and symbol it a Δ. The following Fig.2.1describes the quantization for an analog signal.

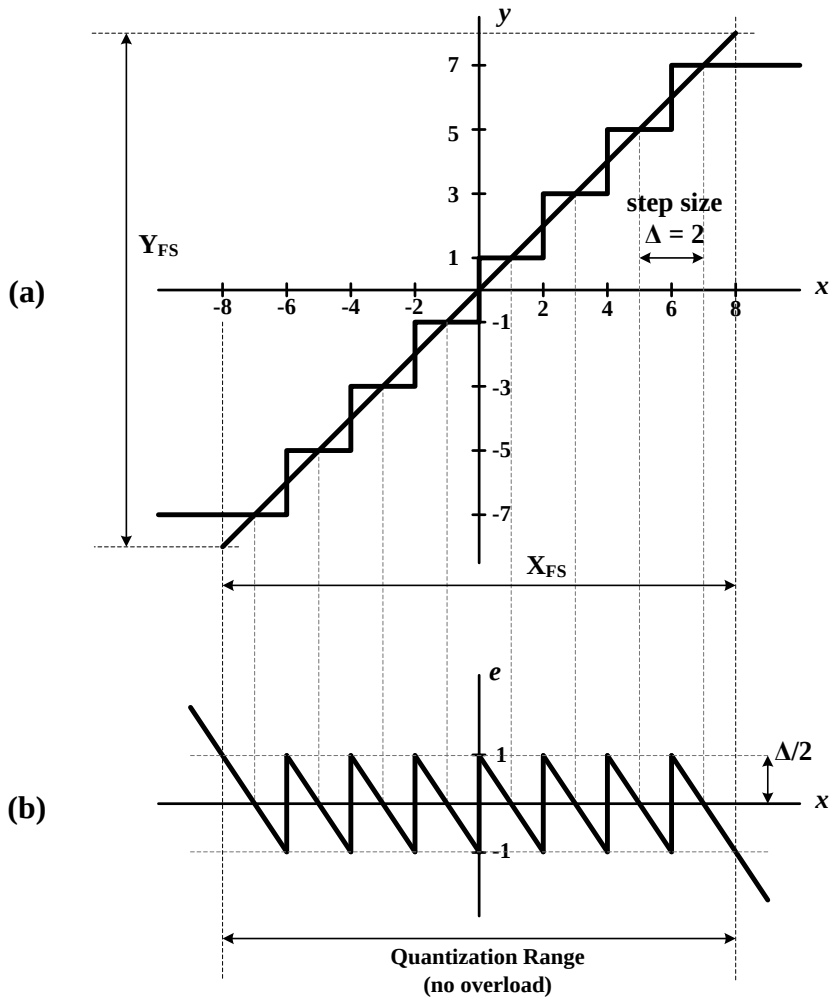

Fig.2.1 Transfer curve (a) and the quantization error of a uniform multi-level quantizer (b)

According to the above figure, the quantization step Δ can be defined as:

$$\Delta = \frac{X_{FS}}{N} \tag{2.1}$$

X_{FS} defines the dynamic range of the quantization and it is equal to 32 for the above figure and N is the total number of quantization intervals, and in the above figure it is equal to 8. Hence, the quantization step Δ is equal to 4 in the above figure. Multi-bit quantizer is the quantizer applied to carry out a multi-level quantization

result with $\log_2(N)$ represents the resolution of a multi-bit quantizer[13]. The quantizer gain C can be defined as the slope of the straight line passing through the center of two axes as shown in the above figure. The expression of quantized signal shown in Fig.2.1(a) is:

$$y = Cx + e \tag{2.2}$$

e is the *quantization error* as depicted in Fig.2.1 (b). The quantization error will be bounded within ±Δ/2 when the quantizer input does not go beyond the no-overload range. And for a particular case that is a binary quantization, and this type of quantization is performed by single-bit quantizer that has only two quantization levels. Since there is only two values of the quantization results in a binary quantizer, the quantization error will be larger than that in the multi-bit quantization. However, the quantization error will still be bounded within ±Δ/2. Different form multi-bit quantization, a single-bit quantizer has the variable gain since there are lots of lines just pass one single point. The arbitrary gain of single-bit quantizer will lead to the linearity problem in the quantization. According to the previous discussion, quantization error dependents on the input signal. Actually the input single can be erratically changed. If the signal amplitude changing over the quantization level spacing and not exceed the no-overload range, the quantization error can be basically sample to sample independent and has equal probability appearing in anywhere within ±Δ/2[14]. By further assuming the error has statistical properties, which are uncorrelated to input signal, hence, the quantization error can be considered as a white noise. This assumption is important for the establishment of modulator's properties which has been validated by many experiments.

On the other hand, the quantization error can be treated in the frequency domain since we have got that it is equivalent to the white noise can be distributed in the amplitude domain within the range of ±Δ/2. Then we can have the following equation which is the mean square value for the power of a quantization noise:

$$p_{quat} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.3}$$

After applying the one-sided representation of the frequencies with the assumption that all the noise power is in the positive frequency range, Power Spectral Density (PSD) for the quantization noise can be accomplished [14]. As an example, assume that the quantizer works with frequency $f = 1/T_S$ and the power are all within the frequency band from 0 to $f_S/2$, therefore, the quantization noise's PSD is:

$$p_{qnD}(f) = p_{quat}\left(\frac{2}{f_S}\right) = \frac{\Delta^2}{6 f_s} \tag{2.4}$$

In order to express the noise performance of a signal processing system, the Signal-to-Noise Ratio (SNR) is defined as below:

$$SNR\big|_{dB} = 10 \cdot \log\left(\frac{P_{signal}}{P_{noise}}\right) \tag{2.5}$$

With the in-band power of the input signal is marked as $p_{signal}$and the input signal noise is p_{noise}. Since for a sinusoidal-wave signal with maximum amplitude of $X_{FS}/2$, the mean square value of its power is

$$p_{\sin} = \frac{1}{T_S}\int_0^T \frac{X_{FS}^2}{4}\sin^2(2\pi ft)\,dt = \frac{X_{FS}^2}{8} = \frac{2^{2N}\cdot\Delta^2}{8} \tag{2.6}$$

With N is the number of quantization levels, as defined in (2.1). Hence, for an input sine wave signal, the SNR for a quantizer can be got as below according to (2.3) and (2.5):

$$SNR_{\sin}\big|_{dB} = 10 \cdot \log\left(\frac{3}{2}\cdot 2^{2N}\right) = 6.02N + 1.76 \tag{2.7}$$

The above (2.7) suggests the trend to increase the resolution of the quantizer: increasing the number of quantization steps. However, for every increasing of extra one bit, the SNR can be only improved by 6dB [14].

Until now, the discussion about the noise in the quantization are only for the Nyquist sampling quantization, which means that the frequency for the sampling are

twice of the frequency of signal band that is $f_S = 2f_B$. Different from the Nyquist sampling quantization, the oversampling frequency quantization distribute the quantization noise power in a frequency band that much larger than signal band, so that a large part of total noise power can be digitally filtered out from the band of interest as depicted in the following Fig.2.2[13][15]. And the ratio of sampling frequency to Nyquist frequency is defined as the OverSampling Ratio (OSR):

$$OSR = \frac{f_S}{2 f_B} \tag{2.8}$$

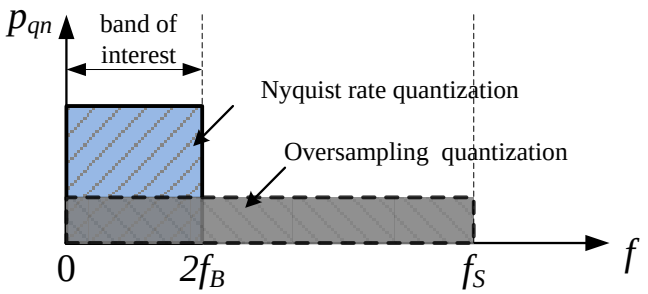

Fig.2.2 Quantization noise distribution in both Nyquist rate and oversampling quantization.

The power of the noise lying in the single band for an oversampling quantization can be got; hence, the SNR for oversampled quantization can be derived according to the above (2.5) and (2.6):

$$SNR_{ovs}\big|_{dB} = 6.02N + 1.76 + 10\log(OSR) \tag{2.9}$$

The above (2.9) gives that for the oversampling quantization with fixed quantizer resolution, the In-Band-Noise (IBN) power can be reduced by 3dB by doubling the OSR, improving the quantizer resolution by half bit which is significantly slow. However, the precision requirement for the quantizer can be reduced by applying oversampling technique. The anti-aliasing specifications of a sampled data converter can be relaxed by using oversampling.

2.3 ΔΣ MODULATION

Compare with the oversampling frequency quantization, the ΣΔ modulation can achieve higher efficient oversampling quantization [15]. A basic architecture for ΣΔ modulator and its linear model are depicted in the following Fig.2.3.

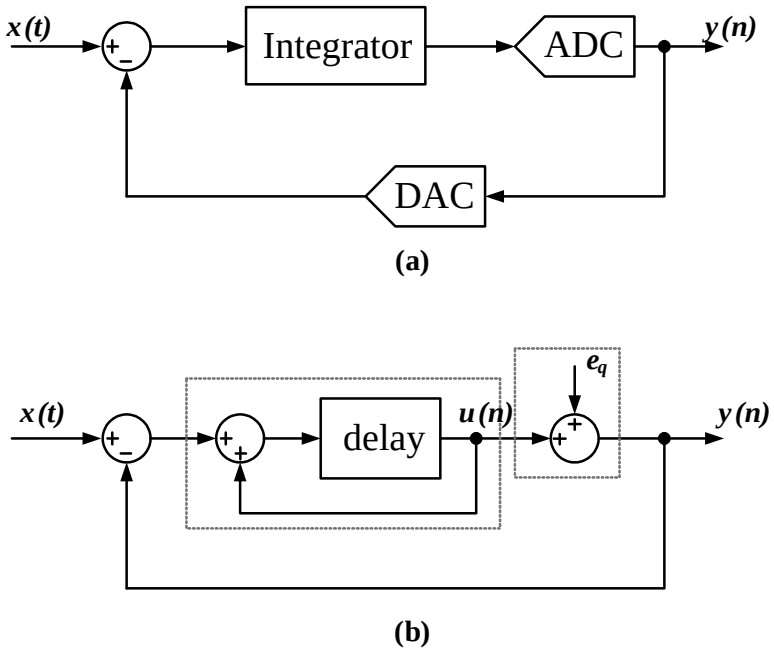

Fig.2.3 Basic architecture (a) and the corresponding linear model for the ΣΔ modulator (b).

e_q represents in the above Fig.2.3 (b) is the quantization error (noise); the output of the modulator is

$$y(n) = u(n) + e_q(n) \tag{2.10}$$

The output of the integrator *u(n)* can be derived and based on the aboveFig.2.3 (b),

$$u(n) = x(n-1) - y(n-1) + u(n-1) = x(n-1) - e_q(n-1) \tag{2.11}$$

Combining (2.10) and (2.11), the output of the modulator can be rewritten as

$$y(n) = x(n-1) + \left(e_q(n) - e_q(n-1)\right) \tag{2.12}$$

Hence, according to the above equation we can have that the expression for the quantization error in the output of a ΣΔ modulator is

$$n(n) = e_q(n) - e_q(n-1) \tag{2.13}$$

The delay block in the system shown in Fig.2.3 can be easily realized by using data sampling circuit. Hence the integrator, also called *loop filter*, in a ΣΔ modulator is conventionally implemented by employing Discrete-Time (DT) filtering circuit. The transfer function of a DT integrator is

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.14}$$

The linear model of the 1st order ΣΔ modulator shown in Fig.2.3 with the integrator whose expression is given in (2.14) is shown in the following figure.

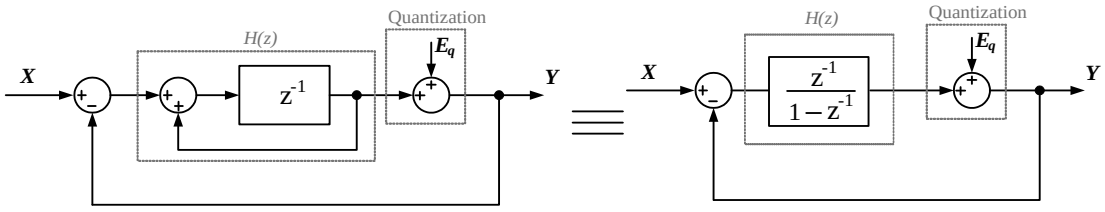

Fig.2.4 Linear model for a 1st order ΣΔ modulator employing DT integrator.

The transfer function describing the system shown in Fig.2.4 is

$$Y(z) = \frac{H(z)}{1 + H(z)} X(z) + \frac{1}{1 + H(z)} E_q(z) \tag{2.15}$$

The term multiplied to the signal expression is defined as *Signal Transfer Function* (STF), and similarly the term multiplied to the noise expression is defined as *Noise Transfer Function* (NTF). By substituting (2.14) into (2.15), it leads

$$Y(z) = X(z)\cdot \underbrace{z^{-1}}_{STF} + E_q(z)\cdot \underbrace{\left(1-z^{-1}\right)}_{NTF} \tag{2.16}$$

Equation (2.16) depicts that through a 1st order ΣΔ modulator, signal is just processed by one clock-period delay and the quantization noise is passed through a 1st order difference which contains high-pass characteristics in frequency domain. We can proof it by estimating it on the unity circle, let $z = e^{j\omega T}$ then we have

$$\begin{aligned} NTF(\omega) &= 1-e^{-j\omega T_S} = 2je^{-j\omega T_S/2}\frac{e^{j\omega T_S/2}-e^{-j\omega T_S/2}}{2j} \\ &= 2je^{-j\omega T_S/2}\sin(\omega T_S/2) \end{aligned} \tag{2.17}$$

$$\left|NTF(f)\right| = 2\sin\left(\frac{\pi f}{f_S}\right) \tag{2.18}$$

Based on (2.18), the gain for the power of quantization noise is

$$G_{Pn} = \left|NTF(f)\right|^2 = 4\sin^2\left(\frac{\pi f}{f_S}\right) \tag{2.19}$$

On the other hand, in frequency domain, the PSD for the noise expression above can be written as

$$P_{\Sigma\Delta 1,nD}(f) = P_{qnD}(f)\left(1-\exp(-j\omega T_s)\right)^2 = 4P_{quat}\left(\frac{2}{f_S}\right)\sin^2\left(\frac{\omega T_S}{2}\right) \tag{2.20}$$

With the above P_{qnd} and P_{quat} are defined in (2.3) and (2.4). Comparative of PSDs for the output quantization noise from an oversampling quantizer and a ΣΔ modulator are shown in Fig.2.5.

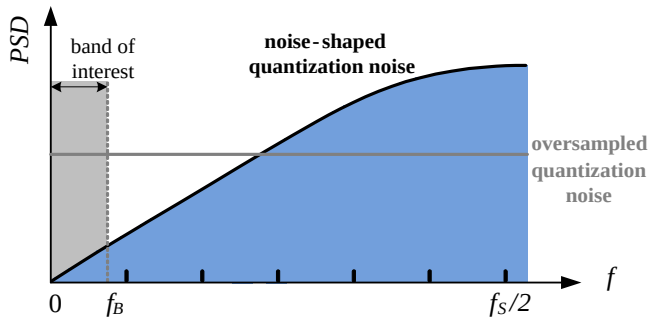

Fig.2.5 The PSDs for the quantization noise from an oversampling quantizer and a ΣΔ modulator.

According to the above result, assort a feedback loop to the quantizer as shown in Fig.2.3 can produce a noise reduction in low frequency band, this technique is called *noise shaping*. Since the quantization error is processed by 1st order difference, the noise shaping obtained is *1st order noise shaping*, and we called the ΣΔ modulator providing a 1st order noise shaping to the quantization noise *1st order ΣΔ modulator*. The total quantization noise power in the signal band of a 1st order ΣΔ modulator is

$$P_{\Sigma\Delta 1,n} = \int_0^{f_B} P_{\Sigma\Delta 1,nD}(f)\,df \approx \frac{\Delta^2}{12}\frac{\pi^2}{3}(2f_B T_s)^3 = \frac{\Delta^2}{12}\frac{\pi^2}{3}\left(\frac{1}{OSR}\right)^3 \tag{2.21}$$

Based on (2.5), (2.6) and (2.21), for sinusoidal input, the SNR of a 1st order ΣΔ modulator is

$$SNR_{\Sigma\Delta 1}\big|_{dB} = 6.02N - 3.41 + 9.03\log_2(OSR) \tag{2.22}$$

From (2.22), in a 1st order ΣΔ modulator with quantizer resolution fixed, by doubling the OSR the IBN power is reduced by 9dB, improving the ADC's resolution by 1.5-bit which is much higher than a oversampling ADC. Because of 1st order noise shaping, by using 1-bit quantizer, according to (2.22), 6-bit resolution can be easily achieved by choosing the *OSR* =16. Hence ΣΔ modulator is very good candidate for high resolution data conversion. On the other hand, from (2.19), the PSD of the quantization noise from a 1st order ΣΔ modulator is amplified by 4; however, it is significantly attenuated in low frequency range. This result corresponds with the descriptions of noise shaping given in (2.20) and Fig.2.5.

2.4 SECOND AND HIGHER ORDER MODULATION

According to the above discussion, for the first order ΣΔ modulator, we can increase the OSR to improve the resolution; however, the ADC's resolution can just be increased by 1.5-bit if we doubling the OSR. It is not an efficiency method to get the high resolution modulator by just increasing the OSR. Based on our knowledge, in order to get higher resolution of the ΣΔ modulator, the IBN of the modulator should be compressed as low as possible. And combine with the noise shaping knowledge as mentioned in the previous section, in order to get high resolution, the noise of the modulator should be shaped out of the signal band we interested in; hence, the higher order modulator is required. According to the structure of the ΣΔ modulator and the transfer function as written in (2.16), the output signal is related with the input signal and the NTF.

According to the 1st order ΣΔ modulator as in Fig.2.4, the second order ΣΔ modulator can be constructed by adding another integrator and feedback path. And the second order structure of the modulator is depicted as in Fig.2.6.

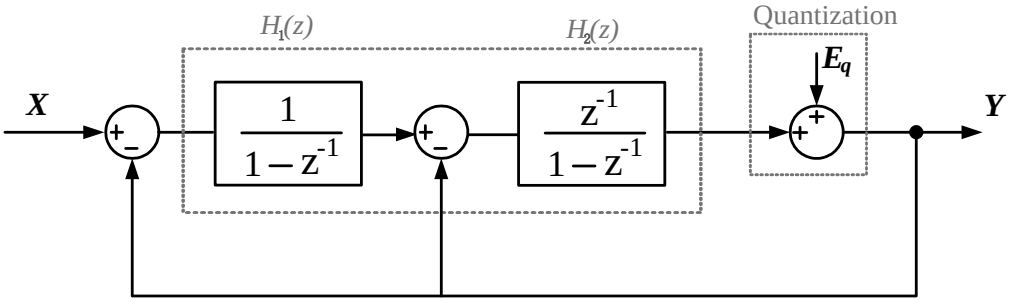

Fig.2.6 A second order ΣΔ modulator.

According to the above figure, we can get the transfer function of it as we got in the first order case.

$$Y(z)=\frac{H_1(z)H_2(z)}{1+H_1(z)H_2(z)+H_2(z)}X(z)+\frac{1}{1+H_1(z)H_2(z)+H_2(z)}E_q(z)$$
$$=z^{-1}X(z)+(1-z^{-1})^2E_q(z) \tag{2.23}$$

Compare the above equation with (2.16), we can find that the only difference is that the order of NTF has increased from one order to two, but there is one cycle delay of the input signal. In order to discuss the performance enhancement, let us focus on the SNR which describes the performance of the ΣΔ modulator. From the power point of view, we can achieve the PSD of the quantization error for the above Fig.2.6 as expressed below.

$$p_{\Sigma\Delta 2,nD}(f)=p_{qnD}(f)\left(1-\exp\left(-j\omega T_s\right)\right)^4=16p_{quat}\left(\frac{2}{f_S}\right)\sin^4\left(\frac{\omega T_S}{2}\right) \tag{2.24}$$

P_{qnd} and P_{quat} are the same as defined in (2.3) and (2.4). From the above equation we can easily observed that the quantization noise has been shaped by the higher order which is $sin^4(\omega T_S/2)$ compare with the first order case which is $sin^2(\omega T_S/2)$. And at the same time, it is attenuated to the low frequency and amplified 16 times. Therefore, in the band of signal, the quantization noise power for the second order case can be got

$$p_{\Sigma\Delta 2,n}=\int_0^{f_B}p_{\Sigma\Delta 2,nD}(f)df\approx\frac{\Delta^2}{12}\frac{\pi^4}{5}\left(2f_BT_s\right)^5=\frac{\Delta^2}{12}\frac{\pi^2}{5}\left(\frac{1}{OSR}\right)^5 \tag{2.25}$$

And when there is the sinusoidal input signal, the SNR can be achieved as well

$$SNR_{\Sigma\Delta 2}\big|_{dB}=6.02N-11.14+15.05\log_2(OSR) \tag{2.26}$$

Hence, it is obviously that for the second order ΣΔ modulator is more efficiency for increasing the resolution of the modulator compare with that in the first order case as in (2.22). Then we can have the assumption that increasing the order of the modulator will increase the performance and resolution significantly for doubling of

OSR. And based on the knowledge of first order and second order modulator, higher order modulator can be constructed by adding more integrators and feedback paths. And the structure of the *Mth* order modulator is shown in the following Fig. 2.7.

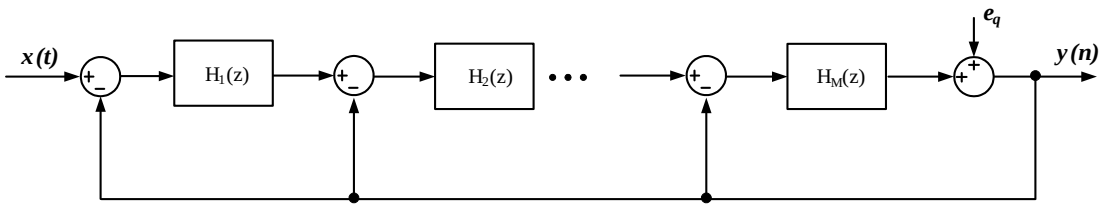

Fig.2.7 The *Mth* order ΣΔ modulator.

And for the above figure, they are the higher order modulator which will lead to higher resolution; however, there is one problem that the higher order of the integrator will lead to the unstable of the system. Until now, there is one solution to solve this unstable problem, that is an additional denominator are added in the NTF and STF and the zeros of the additional denominator should be inside the unity circle and usually close to the frequencies of signal band. However, the additional denominator will reduce the noise shaping function in certain extent. Hence, as the transfer function of the modulator got for the second order and first order case, the STF and NTF can be achieved take the stable problem under consideration,

$$STF = \frac{z^{-1}}{D(z)}$$
$$NTF = \frac{(1-z^{-1})^{M}}{D(z)} \tag{2.27}$$

After we got the NTF and STF of the higher order ΣΔ modulator and similar with the analysis method we used before, we can then get the performance expression SNR of the higher order case. And in order to discuss the higher order case, we start from power point of view. Hence, for *Mth* order ΣΔ modulator, the quantization noise's PSD and IBN power can be achieved

$$p_{\Sigma\Delta M,nD}(f) = p_{quat}\left(\frac{2}{f_S}\right)\left(2\sin\left(\frac{\omega T_S}{2}\right)\right)^{2M} \tag{2.28}$$

$$p_{\Sigma\Delta M,n} = \int_0^{f_B} p_{\Sigma\Delta M,nD}(f)\,df \approx p_{quat}\frac{\pi^{2M}}{2M+1}(OSR)^{-(2M+1)} \tag{2.29}$$

Thereafter, the SNR for the sinusoidal input signal is

$$SNR_{\Sigma\Delta M}\big|_{dB} = 6.02N + 1.76 + 10\log\left(\frac{2M+1}{\pi^{2M}}\right) + 10(2M+1)\log(OSR) \tag{2.30}$$

The above equation suggests the performance of the certain order ΣΔ modulator related with the order of it, the number of bit N used in DAC, and as well as the OSR used. And for the *Mth* order modulator, the performance SNR increases by (6M+3) dB and it is (M+0.5) bit by doubling the OSR. That is the noise shaping function is more effective by increasing the order than just increasing the OSR.

2.5 SINGLE-STAGE AND MULTI-STAGE ΔΣ TOPOLOGY

After the discussion about the order of ΣΔ modulator, this section will introduce two very commonly used topologies of it: single-stage or also called single-loop structure and the other is multi-stage also called as the cascade structure. And for these two different structures of ΣΔ modulator, the differences and advantages of them will be covered separately.

2.5.1 SINGLE-STAGE MODULATOR

As shown in the above Fig.2.7, it is the very classical single-stage ΣΔ modulator. The methodology to verify it is that in the whole structure there is only one quantizer no matter how accuracy of the modulator's resolution. And the single-stage modulator can be further ranked into the *Chain of Integrators with weighted FeedForward summation and local resonator feedbacks* (CIFF) and *Chain of Integrators with*

distributed FeedBack, distributed feedforward, and local resonator feedbacks (CIFB). Both of these two structures are shown in the following Fig.2.8.

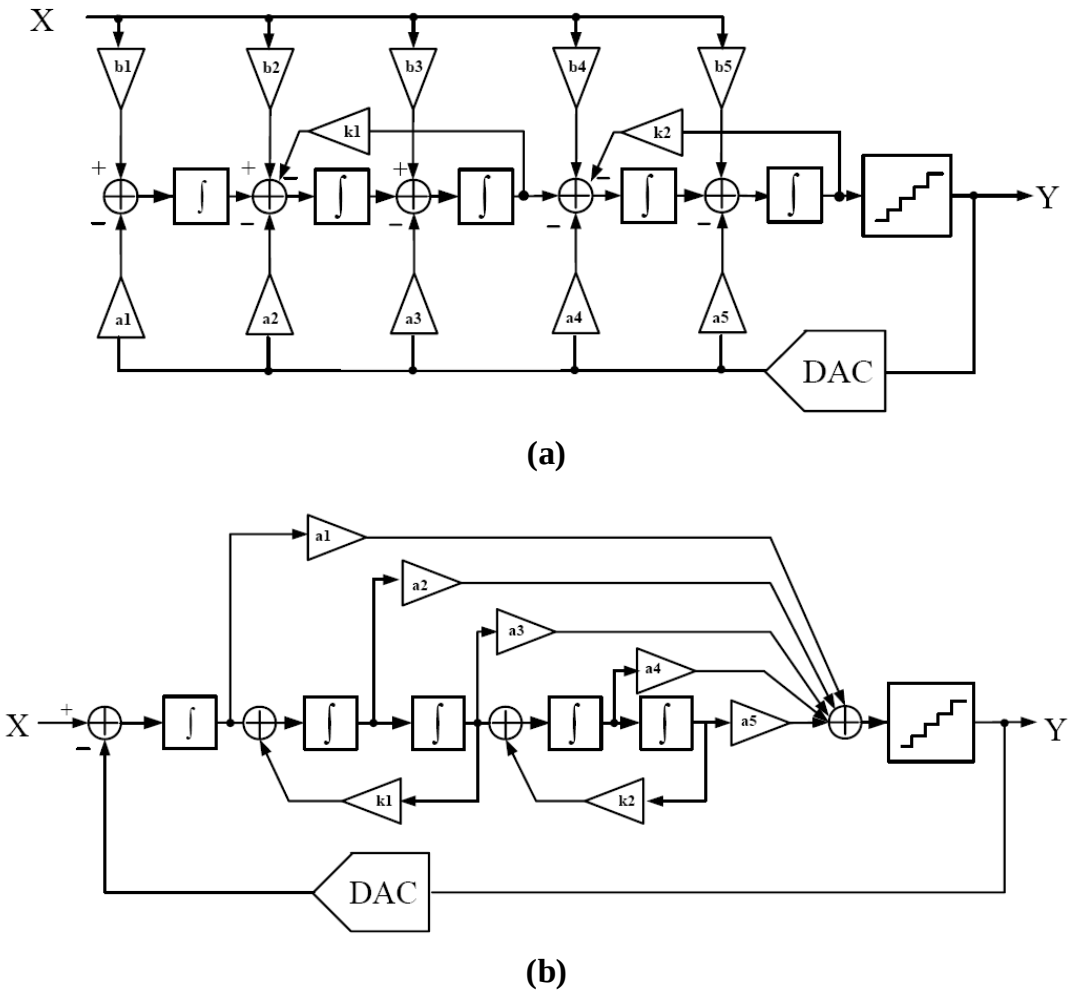

Fig.2.8 Structures of a 5th order (a) CIFB ΣΔ modulator and (b) CIFF ΣΔ modulator.

For the above CIFB single stage structure as shown in Fig.2.8 (a), we have that the feedforward paths are added from the modulator's input to each stage of integrator's input and there are input and feedback signals pass through different loop filters. And there are two local feedback paths as expressed in Fig.2.8 (a), it is employed to move the zeros of the NTF (the loop filter's poles) away from DC and to a frequency that is close to the signal band. Hence, the IBN power can be reduced and this topology is broadly used in wideband high resolution ΣΔ modulator. However, there are also drawbacks of using this kind of structure. Since there are feedforward

paths to the input of the loop integrators, as well as the filtered quantization noise; the output signal swing of each integrator will be large, the linearity problem of the quantizer will be taken consideration and the multi-bit feedback DAC will consume more power and silicon area.

On the other hand, for the CIFF single-stage topology as in Fig.2.8 (b), both of the input and feedback signals pass through same loop filters. Hence the STF of the modulator will be fixed if the loop filter has been designed for desired noise shaping performance. However, in this case, instability problem may be caused in some situation due to the possible STF peaking in high frequency range. And based on the same stability consideration, the local feedback is implemented the same as that in CIFB modulator.

Besides the 1st order ΣΔ modulator, the single-stage ΣΔ structure for higher order case has one commonly issue which is the stability of the system. And for the sake of making the modulator stable, lower forward loop gain should be chosen but which will lead to the reduction of the noise-shaping function. Another methodology is with the multi-bit quantizer, but it will lead to the linearity issued for multi-bit feedback DAC case.

2.5.2 MULTI-STAGE MODULATION

As discussed in the previous part, there are two types of the modulator structures, one is as introduced before the single-stage modulator and the other one is the opposite of the single-stage case which is the cascade modulator. The cascade modulator is also called MASH (Multi-stAge noise Shaping). The purpose to have this new structure is that for the single-stage case, the higher resolution of the modulator should have higher order but higher order will introduce the unstable problem. Hence, this MASH structure is widely used for high resolution case. And the following Fig.2.9 shows one 2-1 MASH ΣΔ modulator.

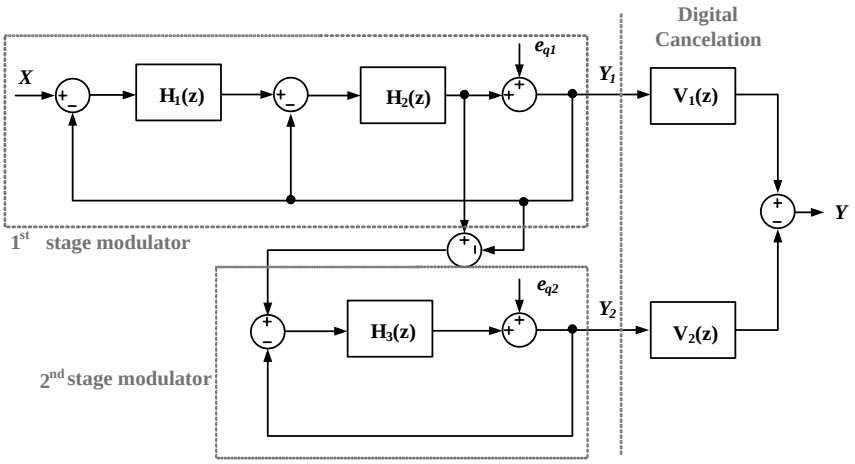

Fig.2.9 2-1 MASH ΣΔ modulator.

According to the above figure, the input signal of the second stage modulator is the first stage modulator's quantization error and we mark it as e_{q1}, and the same as e_{q2}; and then the transfer functions of the two modulators can be got as below:

$$Y_1(z) = STF_1(z)X(z) + NTF_1(z)e_{q1}(z) \tag{2.31}$$

$$Y_2(z) = STF_2(z)e_{q1}(z) + NTF_2(z)e_{q2}(z) \tag{2.32}$$

And then the final Y can be got as below:

$$Y(z) = Y_1(z)V_1(z) - Y_2(z)V_2(z) \tag{2.33}$$

After putting the (2.31) and (2.32) into the above (2.33), we can have the new expression of *Y(z)*.

$$\begin{aligned} Y(z) = &[STF_1(z)X(z) + NTF_1(z)e_{q1}(z)]V_1(z) \\ &-[STF_2(z)e_{q1}(z) + NTF_2(z)e_{q2}(z)]V_2(z) \end{aligned} \tag{2.34}$$

And in order to reduce the quantization error of the whole modulator, if the following equation can be satisfied then the totally output signal of the modulator is related with the input of the signal and the quantization error of the second order of the modulator.

$$NTF_1(z)V_1(z) - STF_2(z)V_2(z) = 0 \tag{2.35}$$

And then for the above equation, it can be easily satisfied: $V_1(z)=mSTF_2(z)$ and $V_2(z)=mNTF_1(z)$, with m is constant. And with the above condition satisfied, then the output signal is that

$$Y(z) = mSTF_1(z)STF_2(z)X(z) - mNTF_1(z)NTF_2(z)e_{q2}(z) \tag{2.36}$$

For the case shown in Fig.2.9, it is a 2-1 MASH ΣΔ modulator, the transfer function for each stage can be got and the constant value $m=1$ are used, then the above (2.36) becomes:

$$Y(z) = z^{-2}X(z) - (1-z^{-1})^3 e_{q2}(z) \tag{2.37}$$

Hence, the above equation shows that for a 2-1 MASH ΣΔ modulator shown in Fig.2.9 has the 3rd order noise shaping performance but just with the 2nd order stability consideration.

However, the above (2.37) establishes with the condition that the equation in (2.35) can be satisfied; if the left hand side of equation (2.35) does not equal to 0, there will be two more turns one the right hand side of the above (2.37) due to the mismatches. And the quantization error of the first stage will leak and the whole modulator's performance will be reduced. This difficulty is due to the hard setting of cancellation logic in analog domain especially for the nanometer-scaled process.

2.6 SUMMARY

In this chapter, elementary of ΣΔ modulator is introduced. The quantization and oversampling technique for the modulator are covered. And then in order to get higher resolution and fast processing speed, the structure of ΣΔ modulator is briefly recalled. And then second order and higher order ΣΔ modulator are introduced as well. Since for the higher order of modulator, the stability issue should be considered. And two

commonly used topologies single-stage modulator and multi-stage are described. In both stage, the advantages and draw backs are depicted.

CHAPTER 3

CONTINUOUS-TIME (CT) ΔΣ MODULATION

3.1 INTRODUCTION

In this chapter, the CT ΔΣ modulator will be introduced includes the advantages, the system and the conversion between a DT ΔΣ modulator and a CT ΔΣ modulator. The implicit anti-aliasing filtering function of CT ΔΣ modulator will be elaborated. And the some non-idealities of a practical CT ΔΣ modulator will be covered. In order to make our following discussion easily, the alternatives for CT filter implementation will be introduced.

3.2 ADVANTAGES OF CT ΔΣ MODULATION

. Compare with traditional DT ΔΣ modulator, CT ΔΣ modulator has been widely used due to its own special advantages. Hence, the five main advantages of it will be introduced in this section.

Anti-aliasing Filtering: compare with a CT ΔΣ modulator, the sample-data circuits are employed as the loop filter in DT ΔΣ modulator; hence, the realization of the in-band noise will be inflected by the aliasing effect of the modulator. Therefore, anti-aliasing elements are necessary in a DT ΔΣ Modulator. However, CT ΔΣ modulators have the implicit anti-aliasing function which will be elaborated in the later section.

Sampling Error Reduction: in a CT ΔΣ modulator, the continuous time signal is

sampled in front of the quantizer, therefore, the modulator loop will noise shape the sampling errors which make the sampling errors in a CT ΔΣ modulator less than that in a DT ΔΣ modulator.

Relax the bandwidth requirement of op-amp: different from the signals in CT ΔΣ modulator which are in continuous-time case, the switch capacitor technique is used in DT ΔΣ modulator to sample the signal. Therefore, the DT ΔΣ modulator should have a maximum clock rate to control the switch capacitors. The op-amp bandwidth will affect the maximum clock rate directly. Hence, the bandwidth requirement of the DT ΔΣ modulator is higher than CT case and at the same time the modulator requires several groups of time constant to settle the required accuracy.

Almost no glitch effect: because the employing of high speed switch capacitor pulses in DT ΔΣ modulator, at the virtual ground node there may be large glitches. On the other hand, in a CT ΔΣ modulator, the virtual ground node is always quite smooth because of the continuous changing signals. Due to this benefit, CT ΔΣ modulator is always being used in high speed resolution case.

Lower supply voltage: in a DT ΔΣ modulator, high voltage is required to drive the switch-on sampled-data path; however, for a CT ΔΣ modulator, pure resistive input impedance can be used, which can be more easily drove.

Even though a CT ΔΣ modulator has many benefits compare with a DT ΔΣ modulator, there are some its own drawbacks such as the clock jitter effect, variations of loop coefficients, excess loop delay and non-idealities of integrators. They will be detailedly discussed in the coming section and chapter.

3.3 CONVERSION OF A DT ΔΣ MODULATION

For designing a CT ΔΣ modulator, we always start from building a DT ΔΣ modulator, and then transfer it from DT to CT because the DT loop filter design is easier than that in CT. Hence the following figure gives the block diagrams for a CT

and DT ΔΣ modulator.

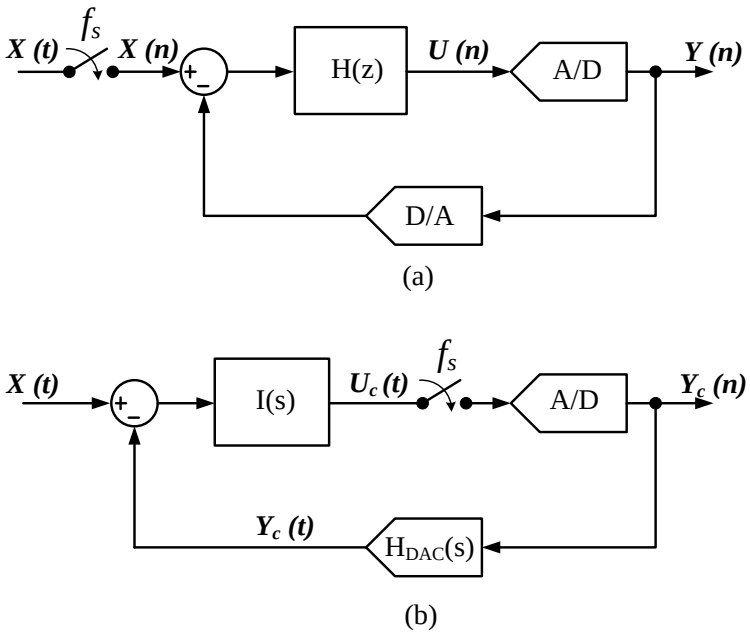

Fig.3.1 Block diagrams for (a) DT and (b) CT ΣΔ modulator.

The difference between a CT ΔΣ modulator and a DT ΔΣ modulator is that for a DT ΔΣ modulator, the signal is sampled in front of the integrator; however, in a CT ΔΣ modulator, the signal is sampled by the quantizer. Compare the CT ΔΣ modulator and DT ΔΣ modulator, if the input signal X(t) are the same, and then the output signal Y(n) are also the same at the same time instant, then we can say that the two modulators are the same no matter what is the signal style inside the modulator.

3.3.1 IMPULSE-INVARIANT TRANSFORM

And since the quantizer in CT case is the same that in DT case, the input of the quantizer should be the same in order to make sure that the DT are equivalent to CT one. Then our discussion about the equivalent of DT and CT ΔΣ modulator start from the point in front of the quantizer and then through the DAC and integrator and the end point is also in front of the quantizer. The feedback loop for the DT and CT ΔΣ

modulator are introduced in Fig.3.2.

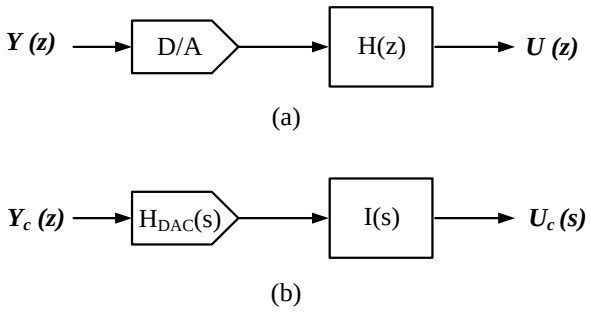

Fig.3.2 The feedback loop filters of (a) DT and (b) CT ΔΣ modulator.

From the above Fig.3.2 (a), the input signal Y(z) is in discrete-time domain and the output U(z) is also in discrete-time domain, compare with that in CT case, we have that the input is in discrete-time domain as well and the output of the integrator is in continuous-time domain. And the function of DAC in the CT ΔΣ modulator is transfer the signal in discrete-time domain to the continuous-time domain; hence, the transfer function of the DAC will affect the transfer function of the modulator directly. And in order to set the equivalent between these two block diagrams, the following equation should be got.

$$\mathcal{Z}^{-1}\left\{H(z)\right\} = \mathcal{L}^{-1}\left\{H_{DAC}(s)I(s)\right\}\Big|_{t=nT_S} \tag{3.1}$$

The above equation also depicts the truth that the waveform of DAC will affect the loop transfer function, and with $H_{DAC}(s)$ is the DAC feedback waveform in the frequency domain. And in order to make our discussion easily, we need to make the above equation from frequency domain to time domain. Hence, we have that

$$h(n) = \left[h_{DAC}(t)i(t)\right]\Big|_{t=nT_S} = \int_{-\infty}^{\infty} h_{DAC}(\tau)i(t-\tau)d\tau\Big|_{t=nT_S} \tag{3.2}$$

Where h_{DAC} depicts the impulse response of the DAC waveform, and the above equation describe that it is related with the different feedback waveforms of DAC. By using the above (3.1) and (3.2), DT and CT modulator can be transferred easily. The

impulse-invariant-transformation (IIT) is named by this methodology of transferring between CT and DT domain. And for this technique, at the sampling times, the open-loop impulse responses are equal.

3.3.2 MODIFIED Z-TRANSFORM

Except the previously discussed IIT method, there are many other techniques to get the transformation between DT and CT domain; this part will introduce another technique called Modified Z-Transform. This method is the extension of general Z-Transform. By using this technique, the signal at all-time instants can be calculated in the discrete time system. It is very efficiency and significant for mutilates sampled systems, sampled-data systems (delay exists) and mixed-signal. And for this modified Z-Transform method, the method to get the corresponding coefficients of the modulator is similar with the previous IIT technique: the DT loop transfer function for the corresponding CT loop filter with certain type of feedback DAC waveform should be got and should be identical to the original function of the ideal DT loop filter. And similar to the previous (3.2), the expression for the Modified Z-Transform can be got as below [14]:

$$H(z) = \sum_i Z_{m_i}\{H(s)R_{DAC}(s)\} \tag{3.3}$$

Where R_{DAC} is the impulse response of the DAC feedback. And the key point in above (3.3) which is different from the previous method is the value of m_i, it should be determined carefully. It is normalized to the sampling period and the value of it is between 0 and 1. The value of m_i equals to 0 means the previous sample instant and the value 1 means the next sample instant. For different types of DAC feedback, the values of m_i are different, since the time instants are different. Take the ideal Half-Return-to-Zero (HRZ) feedback pulse as an example as depicted in the following Fig.3.3.

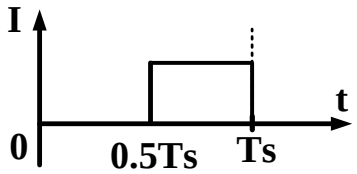

Fig.3.3 The HRZ feedback waveform

At the time t=0.5T_S, it is the first time instant for the starting point of DAC pulse, hence, m_1 equals to 1-0.5/T_S=0.5 and the second time instant is the ending point which is at t=T_S, leads to m_2 equals to 1-T_S/ T_S=0. For a first order modulator, the loop filter can be transferred according to the feedback waveform with corresponding m_i; for a second order or a higher order modulator, every loop filter term can be transferred according to all time instances m_i. After comparing the wanted CT loop filter function with the corresponding ideal DT loop filter, the corresponding new coefficients in CT loop filter can be got. The following will take a HRZ feedback waveform as an example to determine the corresponding new coefficients. And we take the first order CT ΔΣ modulator as an example.

For an NRZ feedback waveform as in previous Fig.3.3, the impulse response of it can be got.

$$R_{HRZ}(s) = \frac{e^{-0.5s}(1-e^{-s})}{s} \tag{3.4}$$

In order to do the further calculation, the following table gives the corresponding loop filter order with the modified Z-transform.

Table3. 1 THE CORRESPONDING LOOP FILTER ORDER WITH THE MODIFIED Z-TRANSFORM

s-domain	**Z_m-domain equivalent**
$\frac{1}{s}$	$\frac{1}{z-1}$
$\frac{1}{s+a}$	$\frac{e^{-amTs}}{z-e^{-aTs}}$
$\frac{1}{s^2}$	$\frac{mT_S}{z-1}+\frac{T_S}{(z-1)^2}$
$\frac{1}{s(s+a)}$	$\frac{1}{a}(\frac{1}{z-1}-\frac{e^{-amTs}}{z-e^{-aTs}})$
$\frac{1}{s^3}$	$\frac{T_S^2}{2}[\frac{m^2}{z-1}+\frac{2m+1}{(z-1)^2}+\frac{2}{(z-1)^3}]$
$\frac{1}{s^2(s+a)}$	$\frac{1}{a^2}[\frac{amT_S-1}{z-1}+\frac{aT_S}{(z-1)^2}+\frac{e^{-amTs}}{z-e^{-aTs}}]$

And as the previous discussion, the rising edge factor of the HRZ feedback pulse is m_1 =0.5 and m_2 =0. The loop filter transfer function of the first order CT ΔΣ modulator is

$$LF(s)=\frac{-k_1 f_s}{s} \tag{3.5}$$

Due to the theory of modified Z-transform, combine (3.5) and (3.4) together, the expression of (3.3) can be got as below:

$$LF(z)\big|_{CT-DT}=Z_{m1}\{\frac{\frac{-k_1 f_s}{s}}{s}\}-Z_{m2}\{\frac{\frac{-k_1 f_s}{s}}{s}\} \tag{3.6}$$

Then after calculation and simplification, the above equation can be simplified and after putting the value of m_1 and m_2 can lead to the below as

$$\begin{aligned} LF(z)\big|_{CT-DT} &= -k_1 f_s Z_{m1}\{\frac{1}{s^2}\} + k_1 f_s Z_{m2}\{\frac{1}{s^2}\} \\ &= -k_1 f_s[\frac{0.5T_S}{z-1} + \frac{T_S}{(z-1)^2}] + k_1 f_s \frac{T_S}{(z-1)^2} \\ &= \frac{-0.5k_1}{z-1} \end{aligned} \tag{3.7}$$

And then, the above (3.7) should be compared with the expression of ideal first order DT ΔΣ modulator, and then find out the corresponding value of k_1. And for different kind of DAC feedback pulse, the expression as shown in (3.4) is different and the value of rising edge m_1 and m_2 also should be recalculated according to the corresponding waveform.

3.4 IMPLICIT ANTI-ALIASING FILTERING

The aliasing effect is due to the alias of the high frequency images in the frequency band of interest in a data sampling ADC. Different from DT ΣΔ modulator, CT ΣΔ modulator has the implicit anti-aliasing filter function since at the multiples of the sampling frequency there is "Sinc" filtering function with zeros allocated which is comprised by the STF of CT ΣΔ modulators. Thus the high frequency images of the clock can be attenuated significantly from the input signal.

Fig.3.4 gives the equivalent form of the model in Fig.3.1. The transfer function F(s) and I(s) are always the same.

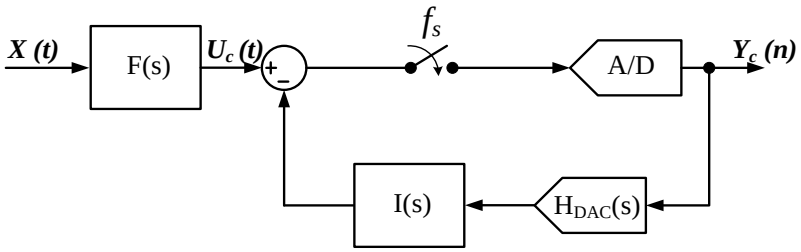

Fig.3.4 A modified representation for CT ΣΔ modulator.

Since the input signal of the CT ΣΔ modulator is in continuous time domain, its expression is related with s-domain. And the output signal of it is in discrete-time domain; hence, it is in z-domain. Due to the above reasons, the STF of the CT ΣΔ modulator cannot be described as a pure s-domain or z-domain equation. The STF for the CT modulator shown in Fig.3.4 can be written as

$$STF(\omega) = \frac{Y\left(e^{j\omega T_S}\right)}{X(j\omega)} \tag{3.8}$$

And in order to make our discussion more simply, we can rearrange the sampling position as shown in Fig.3.5, it is equivalent to that in Fig.3.4. [14]. According to the below Fig.3.5, the feedback loop can be realized equivalent with a DT filter H(z).

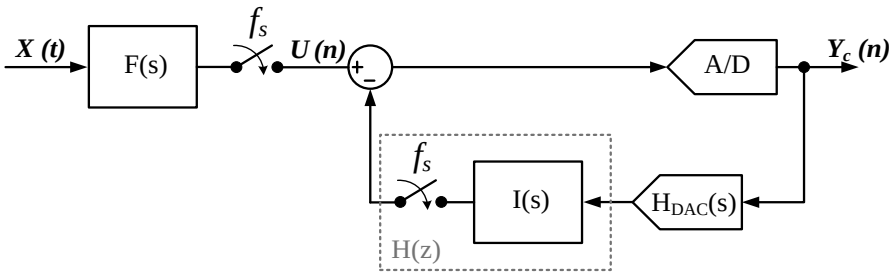

Fig.3.5 A representation for the ΣΔ modulator with CT input transfer function.

The transfer function for the signal from *U(n)* to $Y_c(n)$ can be derived as

$$\frac{Y_c(n)}{U(n)} = \frac{1}{1+H(z)} = NTF(z) \tag{3.9}$$

Therefore, (3.8) can be rewritten as

$$STF(\omega)=\frac{Y\left(e^{j\omega T_S}\right)}{U_c\left(e^{j\omega T_S}\right)}\frac{U_c\left(e^{j\omega T_S}\right)}{X(j\omega)}=\frac{1}{1+H\left(e^{j\omega T_S}\right)}F(j\omega)=F(j\omega)NTF\left(e^{j\omega T_S}\right) \tag{3.10}$$

Based on (3.10), the block diagram shown in Fig.3.1 can be re-depicted in Fig.3.6 [14].

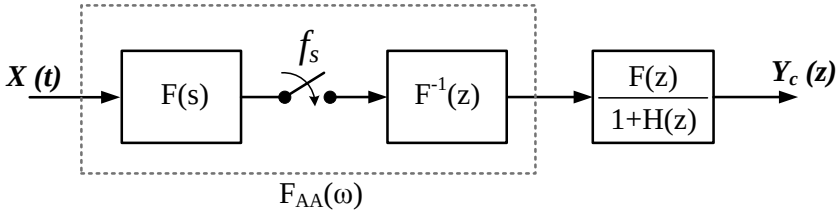

Fig.3.6 CT ΣΔ modulator with input anti-aliasing filtering.

The implicit anti-aliasing filtering function $F_{AA}(s)$ can be expressed as

$$F_{AA}(\omega)=\frac{F(j\omega)}{F\left(e^{j\omega T_S}\right)} \tag{3.11}$$

For F(z) = H(z) and F(s) = I(s), which are existed in most of ΣΔ modulator designs, (3.11) can be written as [16].

$$F_{AA}(\omega)=\frac{I(j\omega)}{H\left(e^{j\omega T_S}\right)} \tag{3.12}$$

The STF expressed in (3.10) can be written as

$$STF(\omega)=\frac{I(j\omega)}{1+H\left(e^{j\omega T_S}\right)} \tag{3.13}$$

Above (3.13) depicts the pole locations are at the multiples of the sampling frequency f_S. Hence, the expression of not only $F_{AA}(\omega)$ but also STF(ω) show that

there are zeros at the multiples of the f_S. Fig.3.7 shows the STF of a 2nd order CIFB CT ΣΔ modulator. The results depict that there are nulls at nf_S ($n \neq 0$) to the input signal for the CT ΣΔ modulator because of a "Sinc" function. The signal falling will attenuated because of implicit anti-aliasing filtering function within the aliasing frequency range which are $[nf_S - f_B, nf_S + f_B]$. Fig.3.7 also shows that the STF(ω) has high-pass function, which will cause the instability of the modulator if the in-band signals suffer the interfering with some out-band tones[17].

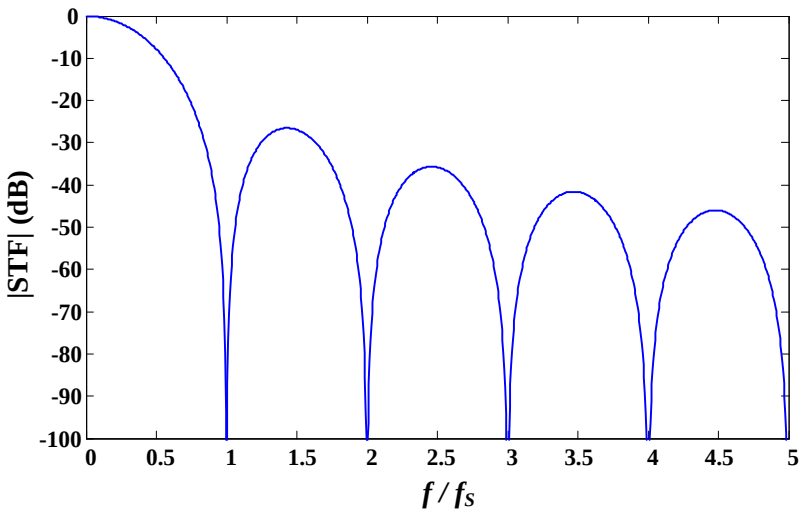

Fig.3.7 STF of a 2nd order CT ΔΣ modulator.

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3.5 ALTERNATIVES FOR CT FILTER IMPLEMENTATION

After discussing the properties of a CT ΔΣ modulator, this part will introduce the alternatives for the CT filter implementation, and will mainly focus on three most commonly used filters in the practical circuit: active RC integrator, Gm-C integrator and the passive RC integrator as well as the properties of them.

3.5.1 ACTIVE RC INTEGRATOR

One of the most commonly used structures of integrator is the active RC integrator, as the depicted in the following Fig.3.8.

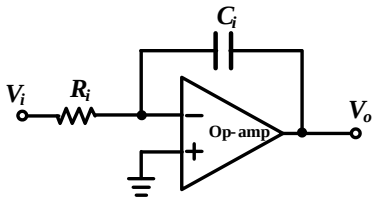

Fig.3.8 Structure of active RC integrator.

This active RC integrator consists of an op-amp, a resistor and a feedback capacitor. The transfer function this type of active RC integrator is shown in the following (3.14):

$$\frac{V_0}{V_i} = \frac{1}{sR_iC_i} \tag{3.14}$$

Because the usage of the active element op-amp, the input node of op-amp approximates to the ideal virtual ground; hence, there is a linear relation between two terminals of the input resistor. The limitation of the linearity depends on the value of the resistor. And the distorted of the above transfer function may also due to the non-idealities of the op-amp (such as the finite gain) and the value of the capacitor. However, the capacitor linearity is not as strict as the resistor (even though the limitation is also related with capacitor type we used); moreover, the capacitor is in the feedback path of the integrator. As a result of these reasons, the distorted of the capacitor can be reduced within a certain amount. The structure shown in above Fig.3.8 can be equivalent to the following transformation block.

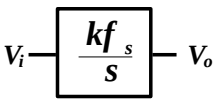

Fig.3.9 Transformation block of active RC integrator.

Hence, the above (3.14) can be rewritten as

$$\frac{1}{sR_iC_i} = kf_s\frac{1}{s} \tag{3.15}$$

With f_s is the sampling frequency of the integrator. Based on the above equation of the relation between the resistor, capacitor and sampling frequency, the integrator can be designed with the required specification by choosing suitable value of these three parameters. And in practical implementation, the fully differential active RC integrator is used to reduce the distortion.

As a result of the benefits of high resolution and high linearity, active RC integrator is a very commonly used type integrator in CT ΔΣ modulators. However, the usage of the active element op-amp will cause large power consumption. In order to reduce the power dissipation of the modulator, other types of the integrator will be introduced thereafter.

3.5.2 Gm-C INTEGRATOR

As the previous discussion about the implementation of the integrator, the active op-amp is used in active RC integrator which will increase the power consumption. Hence this and coming part will introduce the integrator structures which dissipate less power. Different from the active RC integrator will implement the active op-amp, Gm-C integrator employs the transconductance amplifier which transfer the input voltage to current and then to drive the capacitor as shown in Fig.3.10.

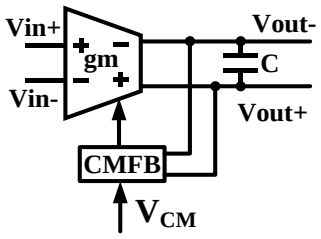

Fig.3.10 The Gm-C integrator structure.

And the transfer function of the above integrator is

$$\frac{V_o}{V_i} = \frac{g_m}{sC} = k\frac{f_s}{s} \tag{3.16}$$

Hence, this integrator is related with the value of transconductance and the capacitors. The benefits of the Gm-C integrator are very easily tunable, fully differential reduce even-order harmonics, small excess phase shift, and low current consumption. However, this structure need large signal swing, large output current source and the nonlinearity in voltage-to-current will limit the total harmonic distortion. And the sharp benefit is it low power consumption and easily implementation.

3.5.3 PASSIVE RC INTEGRATOR

Another alternative CT loop-filter configuration is passive RC filter whose circuit is illustrated in Fig.3.11.

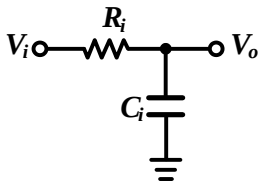

Fig.3.11 Structure of the passive RC filter.

And the transfer function of it is

$$\frac{V_0}{V_i} = \frac{1}{sR_iC_i + 1} \tag{3.17}$$

From the filter transfer function, the filter gain is dependent of RC time-constant and satisfies the relation in (3.15); its pole location is determined by also RC time-constant. Compared with active integrator, passive RC filter cannot achieve pole

location at DC. The mathematic model for passive RC filter is illustrated in Fig.3.12 which shows that to approximate the pole location as of an active RC integrator the filter gain must be minimized. Hence in order to acquire better low-pass characteristics, input signal attenuation will be the tradeoff.

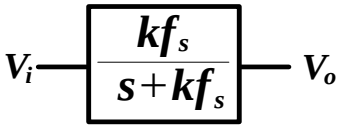

Fig.3.12 Transformation block of passive RC integrator.

Another important drawback of passive RC filter is that its gain at DC is 1 while for active integrator it's infinite; in ΔΣ modulator it requires a high loop gain to suppress In-Band-Noise (IBN), hence passive loop filter is difficult to achieve the loop function that active integrator can perform. In fact, this issue can be minimized by the optimization method presented hereinafter. Besides the DC gain difference, compared with passive structure, active-RC integrator can provide much better suppression to circuit noise and stable virtual ground node which is beneficial for accurate signal summation. In practice, due to the critical SNDR requirement to the input stage in a ΔΣ modulator, active-RC integrator is normally a preferred choice. Owing to the 1st order noise-shaping function achieved by the 1st stage, the loop-filter in the following stages can adopt an optimized passive structure for reducing system power. A mathematical system model for a CT ΔΣ modulator with hybrid AP loop-filter is shown in Fig.3.13.

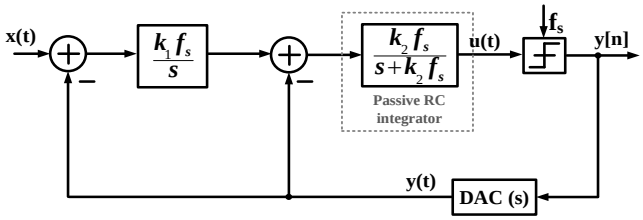

Fig.3.13 System architecture of hybrid AP CT ΔΣ modulator.

3.6 NON-IDEALITY ISSUES OF PRACTICAL CT ΔΣ MODULATOR

For a practical CT ΔΣ Modulator, there are non-idealities cause by two main components: the loop filter and the feedback DAC. The non-idealities caused by these two components may cause the reduction of the performance (SNDR) and the following part will discuss the main non-idealities caused by these two components separately.

3.6.1 TIME CONSTANT VARIATION

In contrast to a DT ΔΣ Modulator, the coefficients variation of a CT ΔΣ Modulator is due to the variation of the time constant which is the multiplication of the forward resistor and the feedback capacitor (for most commonly used active RC integrator as discussed in Sec.3.5.1). Hence, the time constant value cannot be a fixed accuracy value due to the change of the working temperature, the process variation of fabrication and so forth. And for the process variation, 10% to 20% variation is quite normal which will lead to up to 30% time constant variation. As discussed in Sec. 3.5.1, the transfer function of the ideal active RC integrator is introduced as in (3.14), if there is a time constant variation δ, and then the transfer function becomes:

$$\frac{V_0}{V_i} = \frac{1}{sR_iC_i(1+\delta)} = \frac{f_s}{s}\frac{k_i}{(1+\delta)} \tag{3.18}$$

Compare the above (3.18) with (3.14), we can find that the integrator coefficient has been changed due to the variation of time constant. And the feedback path of this active RC integrator is also implemented by the above (3.18), therefore the feedback coefficients variation is also caused by the time constant variation. And for multi-bit resolution modulator, in order to maintain the performance, the Dynamic Element Matching (DEM) or Data Weighted Averaging (DWA) should be employed. And for our discussion about the variation of time constant, we do not take the above DEM or

DWA into account.

In order to discuss the effect of time constant variation, a second order active RC integrator based CT ΔΣ Modulator will be taken as the example with the block diagram of the system is shown as below.

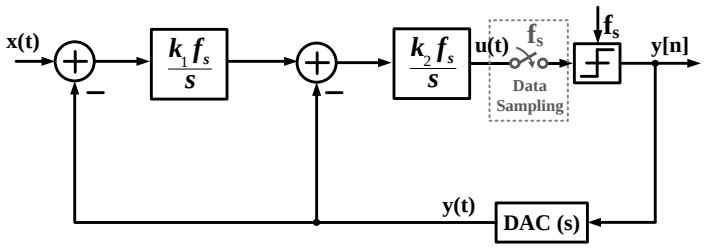

Fig.3.14 A 2nd order CT ΔΣ Modulator with active RC integrators and one-bit quantizer

For the structure shown above, in order to maintain the ideal NTF for the 2nd order CT ΔΣ Modulator, k_1 is equal to 2/3 and k_2 is 3/2. Then the following part will discuss the effect of time constant variation of these two coefficients. And simulation results will be depicted as well and the model to be used in MATLAB is based on that in (3.18). The ideal performance for the above structure gives the SNDR equals to 71.8dB with one-bit quantizer in MATLAB. The following Fig.3.15 is the system sensitive for the coefficient k_1 variation.

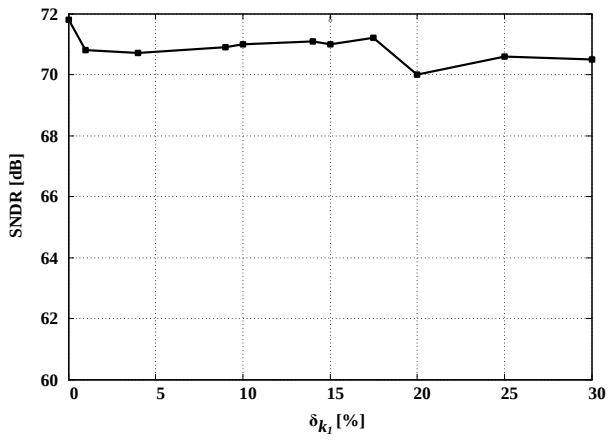

Fig.3.15 System sensitivity to the coefficient k_1 variation

The above figure appears that the coefficient k_1 variation will make the performance (SNDR) of the modulator vary, and the coefficient variation within certain range still make the performance quite stable. And the variation of the coefficient k_2 has also been modeled as depicted in Fig.3.16.

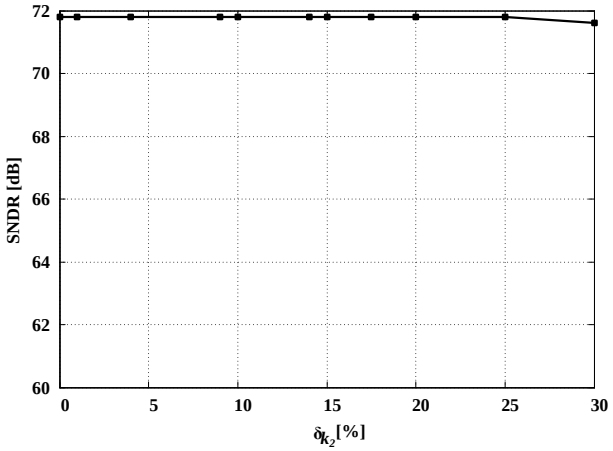

Fig.3.16 System sensitivity to the coefficient k_2 variation

Compare the above two figures we can find that in a 2nd order CT ΔΣ Modulator, the performance is strictly affected by the first order loop coefficient (k_1), but not so critically affected the coefficient higher than the first one (i.e. k_2 in our case).

Hence, for the variation of the time constant in the CT ΔΣ Modulator, the coefficient of the first stage has higher requirement compare with the coefficients thereafter. And the actual time constant variation tolerance also depends on the structure and the resolution of the modulator.

3.6.2 FINITE GAIN AND GBW FOR THE OP-AMP IN CT INTEGRATOR

After the discussion about the time constant variation in the CT ΔΣ Modulator, this part will focus on the non-idealities caused by the integrator. Finite gain of the integrator as well as the finite GBW which are caused by the non-idealities of the

integrator will be covered.

Same as the effect of finite gain to the DT ΔΣ Modulator, it will also reduce the performance of the modulator. For our discussion simplicity, we focus on the active RC integrator same as previous section. And then for the finite gain of the amplifier A_{dc} and refer to the structure in Fig.3.8 and the expression in (3.14), the transfer function due to it will be

$$\frac{V_0}{V_i}\Big|_{A_{dc}} = \frac{f_s k_i}{s(1+A_{dc}) + \frac{1}{A_{dc}} k_1 f_s} \approx \frac{f_s k_i}{s + \frac{1}{A_{dc}} k_1 f_s} \tag{3.19}$$

In contrast to the expression in (3.14), the above equation depicts that the pole location of the active RC integrator has changed from dc to the inner of unit circle. The change of the poles in transfer function will lead to the change of the zeros in NTF, this zeros' change direction directly affects the noise shaping type and increase the in-band-noise of the modulator.

After discussion about the finite gain effect of the op-amp to the modulator, the following part will discuss the finite GBW effect. It can be disassembled as the gain error and an additional pole in the transfer function [14]. For a simple single-input single-output active RC integrator, the transfer function is in (3.10).

In order to analyze the effect of finite GBW in the op-amp, the equivalent small signal model is as shown in Fig.3.17.

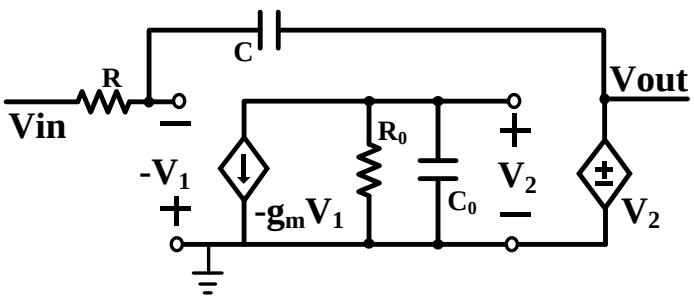

Fig.3.17 Equivalent small signal model of single-input single-output active RC integrator.

According to the equivalent structure, the real transfer function of the amplifier can be got as:

$$\frac{V_2}{V_1} = \frac{GBW \times A_{DC}}{s \times A_{DC} + GBW} \tag{3.20}$$

$A_{DC}=g_mR_0$ is the DC gain of the amplifier, $GBW=g_m/C_0$ is the gain bandwidth product of the amplifier. And then the transfer function of the structure shown in Fig.3.17 can be derived as:

$$\begin{aligned}\frac{V_{out}}{V_{in}} &= -\frac{GBW \times \frac{1}{R \cdot C}}{s^2 + s \times (\frac{1}{R \cdot C} + \frac{GBW}{A_{DC}} + GBW) + \frac{GBW}{R \cdot C \times A_{DC}}} \\ &\approx -\frac{GBW \times \frac{1}{R \cdot C}}{s^2 + s \times (\frac{1}{R \cdot C} + GBW)}\end{aligned} \tag{3.21}$$

And the approximation is due to the assumption of large DC gain of the amplifier. According to the above (3.20), the poles of the structure in Fig.3.17 are:

$$\begin{aligned} poles: \ s_1 &= 0 \\ s_2 &= -\frac{1}{RC} - GBW \end{aligned} \tag{3.22}$$

Compare (3.21) with the transfer function of an ideal active RC integrator as in (3.10), there is one additional pole. It is detected that the denominator order of transfer function is increased from one to two, as well as the numerator also changed.

3.6.3 CLOCK JITTER EFFECT

As mentioned before, the non-idealities of the modulator are mainly caused by two components: the integrator and the feedback DAC. The previous section

discusses the non-idealities caused by integrator such as the finite gain and finite GBW of it. This part will discuss the non-ideality which is caused by the feedback DAC. Clock jitter is one of dominant non-ideality, which reduces the performance due to the change of the feedback amount. And there is another non-ideality which is called the Excess Loop Delay (ELD), it is caused by the finite response time of the quantizer and DAC's switches. This ELD effect will be stress introduced in the following chapter. And this part will focus on the effect of clock jitter.

Clock source's purity controls the clock jitter effect, and it is the due to the sampling frequency's variation.

Different from the CT ΔΣ modulator, at the end of a clock cycle, the output of the switch capacitor integrator will settle to a stable value for a DT ΔΣ modulator. Sampling error will be introduced in the front end sample and hold stage due to the clock jitter, therefore, the performance of the modulator may be degraded. However, the clock jitter effect is not so significant since the IBN power which is introduced by clock jitter is proportional to OSR^{-3}[18][19][20]. However, for a CT ΔΣ modulator, the signal is sampled in front of the quantizer or sometime actually implemented by the quantizer. Hence the sampling error due to the clock jitter can be maximally suppressed by the modulator's loop in the band of interest. Nevertheless, clock jitter will influence the feedback of the DAC significantly since it will cause the variation of Pulse-Position (PP) and Pulse-Width (PW) as depicted in the following Fig.3.18. The effects of clock jitter to either PP or PW will make the random variation to the feedback waveform of the modulator and introduce the error which will increase the IBN floor of the modulator. Compare the effect of PP and PW, PW is more dominant since it will change the feedback result in the first stage loop filter in where the noise shaping function cannot available.

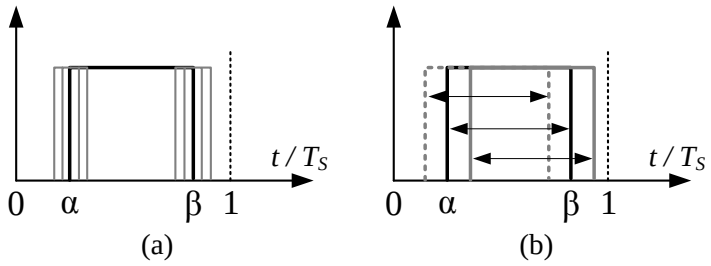

Fig.3.18 Clock-jitter induced (a) PW variation and (b) PP variation

As discussed in[21][22][23], the integrated area of the feedback waveform over a feedback cycle which is equivalent to the feedback charge quantity will directly influence the performance of the CT ΔΣ modulator significantly since the first stage loop filter is the most relative stage to the input signal over the after stages, and the and the feedback result in the 1st stage only depends on the feedback charge quantity.

Clock-jitter in CT ΔΣ modulators is due to the clock phase noise generated by the Voltage Controlled Oscillator (VCO) in the Phase Lock Loop (PLL) [23]. Hence the clock-jitter induced PW and PP variations are random, thus they can be considered as feedback noise. That is the reason why PW and PP variation can increase the IBN floor. Clock-jitter induced feedback noise is added to the input of loop filters increasing the noise power in the modulator's loop. As mentioned, in the first stage loop filter, the noise cannot be shaped, and also the feedback in the first stage only depends on the feedback charge quantity, thus the jitter induced feedback PW noise in the first stage can significantly influence the SNR of the whole modulator.

Besides the non-ideality caused by the clock jitter, there is another non-ideality which is also mainly due to the feedback DAC as mentioned before and named as the ELD, it will be mainly covered in the following chapter as well as the compensation method for this effect.

3.7 SUMMARY

In this chapter, the advantages of the CT ΔΣ Modulator compare with DT ΔΣ Modulator has been introduced, the methods to do the equivalent between the DT ΔΣ Modulator and CT ΔΣ Modulator such as the IIT and modified Z-Transform have been covered. And then some commonly used implementation of the CT filters (such as the active RC integrator, Gm-C integrator and passive RC integrator for different functions) has been discussed and finally the non-idealities of the CT ΔΣ Modulator has been briefly introduced and covered. Compare with DT ΔΣ Modulator, CT ΔΣ Modulator has its own benefits such as low power consumption, implicit anti-aliasing filtering, low supply voltage and so on. However, different from the DT ΔΣ Modulator, the CT ΔΣ Modulator has its own non-idealities which may reduce the performance significantly. And in order to maintain the high performance of the modulator, there are lots of compensation methods focus on different kind of non-idealities. The coming chapter will discuss the non-ideality named Excess Loop Delay (ELD) and the existed compensation techniques, and it is also my research field and direction.

CHAPTER 4

EXCESS-LOOP-DELAY (ELD) AND ITS COMPENSATION TECHNIQUES OF CT ΔΣ MODULATORS WITH ACTIVE RC INTEGRATOR

4.1 INTRODUCTION

As discussed in the previous chapter, there are lots of non-idealities in the practical CT ΔΣ Modulator. Except the non-idealities of the first integrator, the non-idealities caused by the Digital-to-Analog-Converter (DAC) are dominant which may also degrade the performance significantly since the feedback waveform depicts the feedback coefficients of the modulator. Hence, this chapter will mainly focus on the non-idealities which due to the finite switching response time of the DAC and quantizer in transistor level, which is named Excess-Loop-Delay (ELD)[15]. Compare with the response time of DAC, the finite response time of the transistors in quantizer is small; therefore, when we discuss the ELD effect of modulator we mainly focus on the ELD effect of DAC most of time [14]. And due to the degrees of ELD effect and the feedback pulse waveform, there are different performance degradation.

4.2 ELD EFFECT IN CT ΔΣ MODULATOR

Basically, ELD effect can be divided into two different categories: the order of the modulator may be increased, and the other one is there will be the coefficients mismatch. Both effects will be discussed separately in detail in this section combine

with different kind of feedback pulse.

4.2.1 DELAY AFFECTS THE RETURN-TO-ZERO (RZ) FEEDBACK

There are lots of types of feedback pulse in the existed literatures for different functions of the CT ΔΣ Modulator. According to the position of the feedback pulse in each clock cycle, they can mainly be divided into two groups: the Return-to-Zero (RZ) feedback pulse and Non-Return-to-Zero (NRZ) feedback, and take the ideal rectangular shape feedback pulse an example in our discussion, as shown in Fig.4.1 [14].

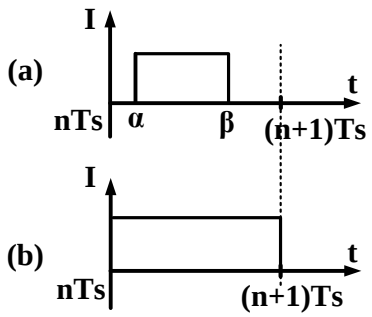

Fig.4.1 Rectangular waveforms of: (a) RZ feedback, (b) NRZ feedback.

RZ feedback means that the signal will be reset to original 0 for the coming next clock cycle, and with the starting feedback point is not limited. And as depicted in Fig.4.1 (a), the starting point is α and the return to zero point is β, in order to make sure that the feedback pulse is RZ feedback, the value of α and β should satisfied the following equation in a normalized time interval:

$$n \le \alpha < \beta < n+1 \tag{4.1}$$

And for a RZ feedback pulse in Fig.4.1 (a), if there is ELD effect τ_d, the feedback waveform is changed and as in Fig.4.2.

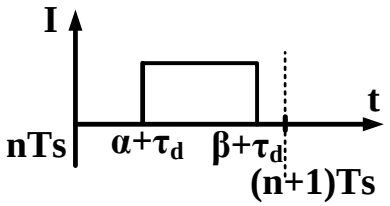

Fig.4.2 RZ feedback waveform with ELD τ_d.

From the above figure we can find that due to the delay amount τ_d, the feedback waveform has been shifted, the starting point is $\alpha+\tau_d$ and the return to zero point has become $\beta+\tau_d$. Hence, the time interval of the RZ feedback has changed from $[\alpha,\beta]$ to $[\alpha+\tau_d, \beta+\tau_d]$ due to ELD effect. According to the discussion about the conversion of a DT ΔΣ Modulator to a CT ΔΣ Modulator as in Sect. 3.3, the feedback coefficient is directly related with the time interval and shape area of the DAC feedback pulse [15].

In order to express the coefficients mismatch of the modulator, let us take the second order CT ΔΣ Modulator as an example [13] [24]. An ideal 2nd order ΔΣ Modulator are shown in the following Fig.4.3 [25].

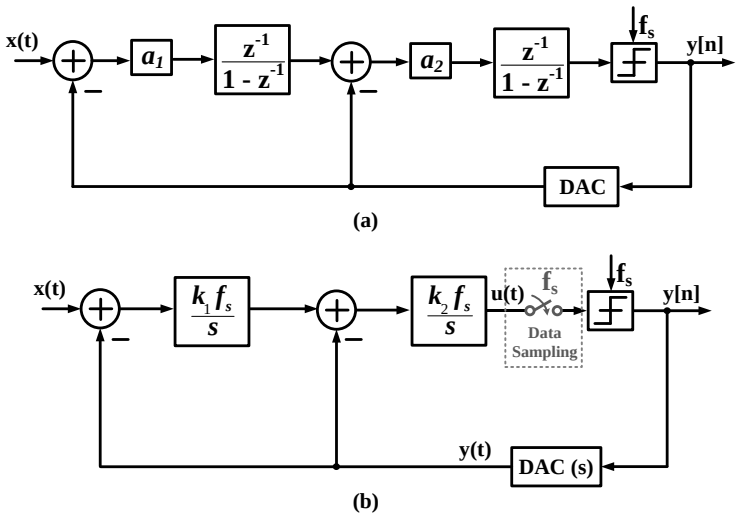

Fig.4.3 System architectures of a 2nd order (a) discrete-time and (b) active continuous-time ΔΣ modulator.

For a second order CT ΔΣ Modulator, the Loop Function (LF) can be got:

$$LF(s) = -a_2 \frac{\frac{f_S}{\beta-\alpha}}{s} - a_1 a_2 \frac{\frac{f_S(\beta+\alpha-2)}{2(\beta-\alpha)} s + \frac{f_S^2}{\beta-\alpha}}{s^2} \tag{4.2}$$

With a_1 a_2 are the coefficients in the DT ΔΣ Modulator in Fig.4.3 (a). From the above (4.2), the new value β-α is fixed when there is delay τ_d; however, the new value of α+β changes to α+β+2τ_d. Therefore, the coefficient to the first integrator is fixed with the coefficient to the second integrator is altered exactly. And then the in band noise has increased. However, the NTF of the modulator does not change.

According to the above (2), take a_1=0.125, a_2=0.5, [α, β] = [0, 0.4] as an example and then test the effect of τ_d (from 0 to 40%T_S) to the modulator.

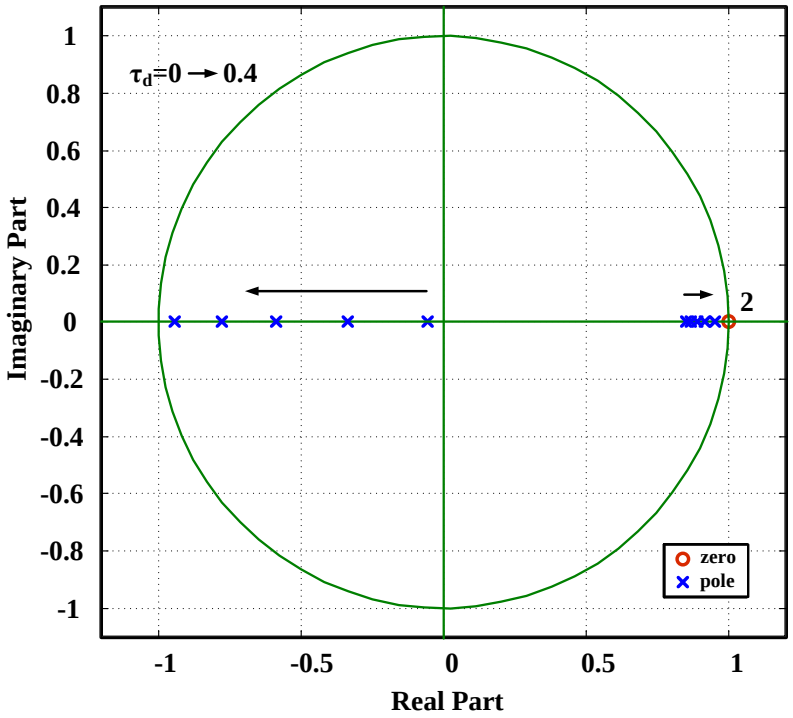

Fig.4.4 NTF pole-zero locations of RZ feedback with delay τ_d.

The pole-zero locations of the modulator are shown in the above figure and we can find that the zero of the modulator does not change when the delay amount changes from 0 to 40%T_S. After getting the pole and zero locations of the modulator,

the NTF can also be got.

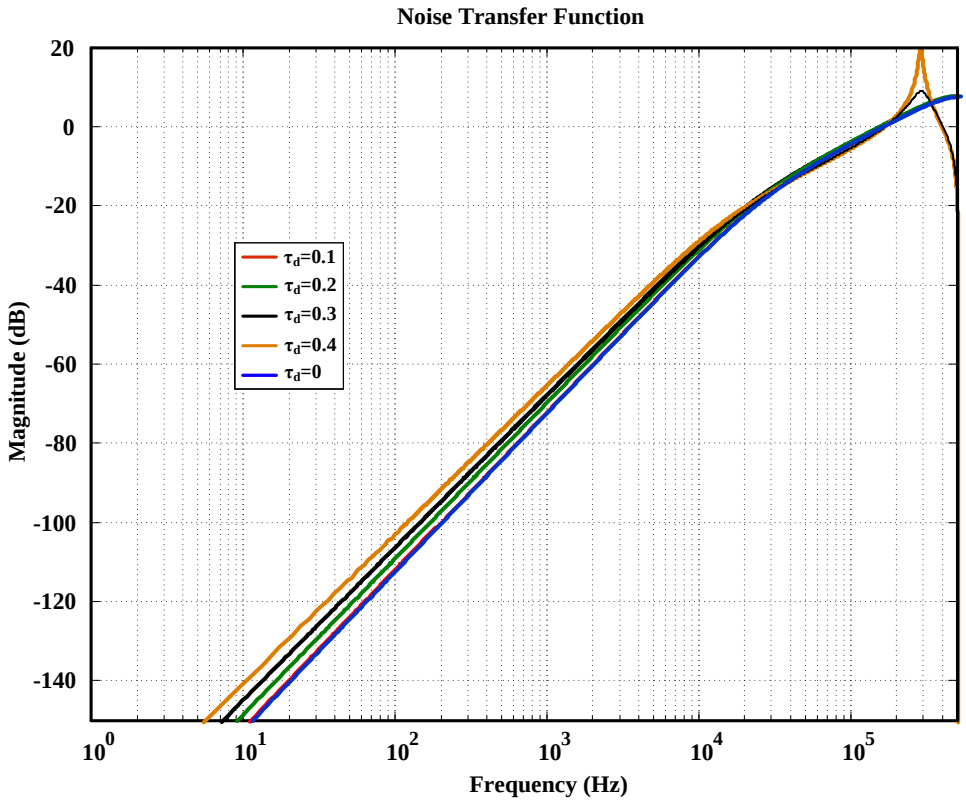

Fig.4.5 The NTF for RZ feedback with different values of delay τ_d

The above figure depict that with different values of delay, the noise shaping of the modulator is the same, however the in-band noise has been changed: large delay will increase the in-band noise which satisfied with the previous discussion. Hence, the altered time interval of feedback DAC pulse may lead to the change of the feedback coefficients of second and higher order modulator.

4.2.2 DELAY AFFECTS THE NON-RETURN-TO-ZERO (NRZ) FEEDBACK

After the discussion of ELD effect in RZ feedback pulse, and compare the waveforms (a) and (b) in Fig.4.1 and (1), we can find that NRZ feedback pulse is the extreme condition of the feedback pulse: RZ in one clock cycle: α=n and β=n+1. And

similar with the discussion of RZ feedback pulse, the ELD effect will shift the NRZ feedback pulse[14]. Since the time interval of ideal NRZ feedback is [n, n+1], the time interval due to delay τ_d will be [n+τ_d, n+1+τ_d], as shown in Fig.4.6.

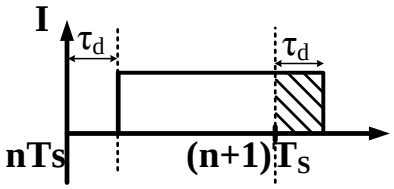

Fig.4.6 NRZ feedback pulse due to delay τ_d.

Hence, part of the feedback pulse has been shifted into the next coming period. The new feedback pulse can be divided into two part: during the first clock cycle, the time interval of feedback pulse is [n+τ_d, n+1]; and in the coming next clock cycle, the time interval is [n+1, n+1+τ_d]. And in order to discuss the effect of ELD to an ideal NRZ feedback, the LF also should be got.

$$LF(s) = -(a_2 - \frac{a_1 a_2}{2})\frac{f_S}{s} - a_1 a_2 \frac{{f_S}^2}{s^2} \tag{4.3}$$

From (4.3) we have that the LF just related with the value of feedback coefficients, it does not related with the starting point and return to zero point since it occupies each whole clock cycle. However, due to the effect of ELD, the pulse is shifted to the next clock cycle. In order to discuss the effect of ELD to NRZ feedback, the above (4.3) should be transferred into the discrete time domain. Take a 2nd order CT ΔΣ modulator as our discussion example again. Then we can have that LF with delay τ_d is

$$\begin{aligned} LF(s)\big|_{\tau_d} = -\Big\{&\Big[-a_1 a_2 {\tau_d}^2 + (2a_2 + a_1 a_2)\tau_d - 2a_2\Big] z^2 \\ &+ \Big[2a_1 a_2 {\tau_d}^2 - 4a_2\tau_d + 2a_2(1-a_1)\Big] z \\ &+ a_2(2-a_1)\tau_d - a_1 a_2 {\tau_d}^2\Big\} / (2z^3 - 4z^2 + 2z) \end{aligned} \tag{4.4}$$

With a_1 a_2 are the coefficients in the DT ΔΣ Modulator. Take a_1=0.125, and a_2=0.5 as an example and then test the effect of τ_d (from 0 to 30%T_S) to the modulator. After using the above (4.4), the LF can be got in discrete time domain; hence the pole and zeros of NTF can be got to analyze the stability and variation of pole and zero locations when there is delay exists.

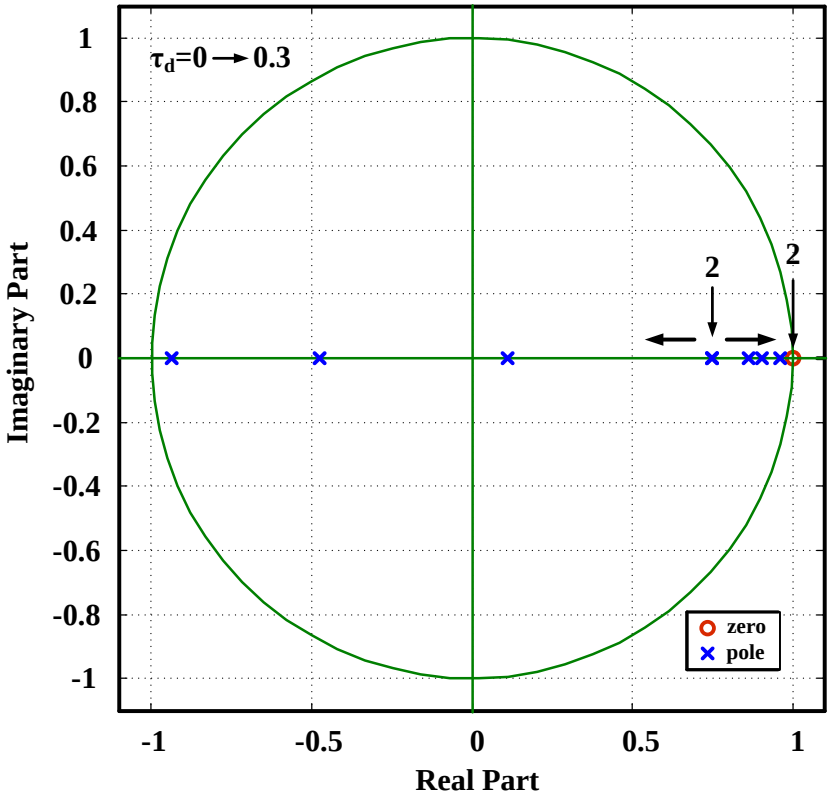

Fig.4.7 Pole and zero locations of NRZ feedback when there is delay τ_d

From the above figure, there are two same poles and two same zeros when there is no delay exists. Whenever there is delay exists, the pole and zero locations are changed: they are becoming more and more far away from each other. If the delay is large enough, then one pole of the modulator will be pushed out of the unit cycle, hence, lead to the un-stability of the modulator. However, the zeros of the modulator are unaltered. After the discussion about the poles and zeros of the modulator, the noise shaping shapes of the modulator are also needed. Therefore, the following

figure shows the NTF of the modulator when there are different values of the delay amount.

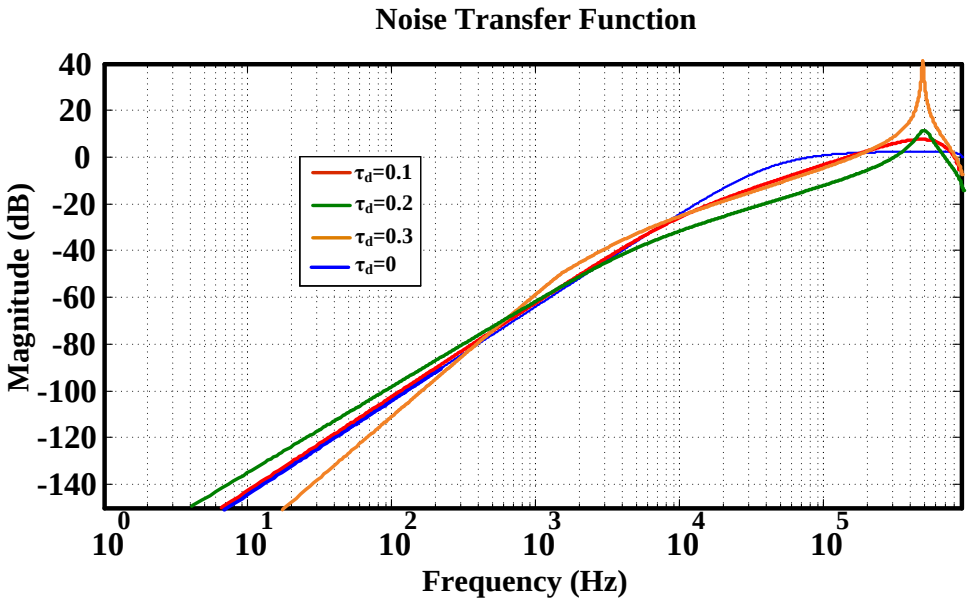

Fig.4.8 The NTF with different value of delay τ_d with NRZ feedback

From the above figure we can find that the noise shaping shape of the modulator is almost unaltered, the differences are that with different value of delay, there will be peak of the modulator that is the modulator may be unstable. This result matches with the previous pole zero location discussion: certain amount of delay will make the system unstable.

Since the effect of ELD is quite significant to a CT ΔΣ Modulator, the methods to compensate the effect of it is very necessary. Hence, the following part of the chapter will discuss the existed ELD compensation techniques.

4.3 EXISTED ELD COMPENSATION METHODS

As a result of the significant effect of ELD for a CT ΔΣ Modulator,

compensation method to compensate the performance of it is required. This section will discuss some of existed compensation method.

4.3.1 TRADITIONAL COMPENSATION TECHNIQUE WITH ADDITIONAL FEEDBACK PATH

In order to make our discussion more convenient, as in the previous discussion and refer to the figure in Fig.4.3, let us take the 2nd order CT ΔΣ Modulator as the example and since the previous discussion shows the modulator is more sensitive to NRZ feedback, it is also used in our discussion. Since the performance of the modulator will be reduced because of the variation of the NTF, our compensation methods are focused on the technique to make NTF equals to that in ideal case. For an ideal 2nd order DT ΔΣ Modulator,

$$NTF = (1 - z^{-1})^2 \tag{4.5}$$

The goal of the ELD compensation is to make sure that the NTF of the new modulator is identical with that of ideal one [26] [28].

The following figure gives the structure of the traditional compensation when there is half cycle delay. The loop delay is related with the real-time modulator. This traditional compensation method contains a constant delay placed before the feedback DAC which is half of a clock cycle and this constant half of a clock cycle delay can be employed by a D Flip-Flop (DFF). DFF can lock the delay of the signal within a certain time; therefore, it can tolerate smaller delay lengths. The NTF of the classical structure (Fig.4.9) is calculated to analyze the compensation of the ELD effect, in order to make the compensation method operate properly theoretically; it should be equal to (4.5). And, in the circuit level, one adder is needed as well as an extra DAC, which are the inside elements of red rectangular in the following Fig.4.9. Usually, the adder is employed by an amplifier; however, the power consumption of the modulator will be increased due to this active element. And as the structure shown in Fig.4.3 (b),

the LF can be got.

$$LF[z] = Z\left\{L^{-1}[(k_1k_2s^{-2} + k_2s^{-1})DAC(s)]_{t=n/f_S}\right\} \tag{4.6}$$

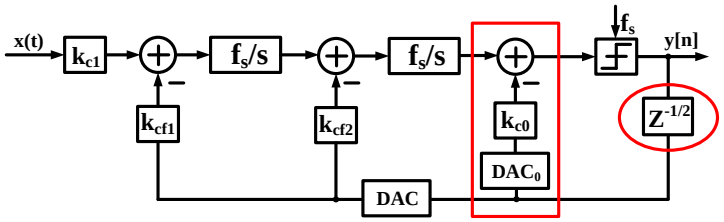

Fig.4.9 Traditional ELD compensation method.

And for the structure in Fig.4.9, we can have the LF of it

$$LF[z]\big|_{classical} = Z\left\{L^{-1}[(k_{cf1}k_{cf2}s^{-2} + k_{cf2}s^{-1} + k_{cf0})DAC(s)e^{-\frac{1}{2}s}]_{t=n/f_S}\right\} \tag{4.7}$$

In order to maintain the performance of the modulator, the above (4.7) should equal to (4.6). Hence, we can get the new group of the coefficients to make sure that the structure in Fig.4.9 matches with that in Fig.4.3 (b):

$$\begin{aligned} k_{cf0} &= \frac{1}{4}k_2(2+\frac{1}{2}k_1) \\ k_{cf1} &= \frac{k_1}{1+\frac{1}{2}k_1} \\ k_{cf2} &= k_2(1+\frac{1}{2}k_1) \end{aligned} \tag{4.8}$$

And the above discussion just take the delay amount equals to half of clock cycle as an example, the delay can be set to one clock cycle as well. And the compensation method is the same as that when there is one of clock cycle delay, and this method can compensate the delay amount up to one clock cycle. However, from figure we can find that in order to reach the goal to identical to the ideal case, there is one additional feedback path added to the quantizer, and this path always needs an additional adder,

it will consume more power.

4.3.2 ELD COMPENSATION METHOD WITH A DIGITAL DIFFERENTIATOR

Since from theFig.4.9 we can find that there is additional feedback path in front of quantizer and the adder is always be implemented by active elements which will consume more power, the technique which will combine the additional path with the input of the last integrator can be realized. The following Fig.4.10 gives the structure of ELD compensation using a digital differentiator [26].

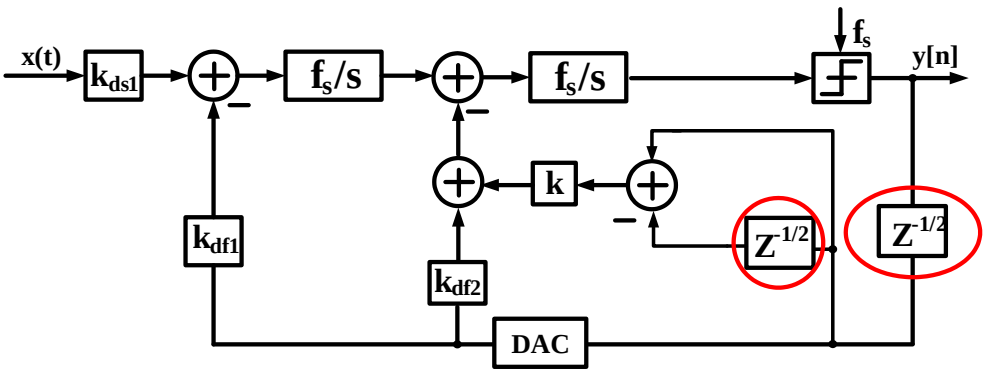

Fig.4.10 ELD compensation with a digital differentiator.

In this case, we also use the assumption of delay equals to half of clock cycle; the situation is similar with the case when delay amount is larger than half of clock cycle but less than one clock cycle. And from the above figure can observe that there is DAC output signal which is differentiated before the last integrator. However, the structure should satisfy the condition that the sum of delays which are rounded in the red cycle should less or equals to one clock cycle. Otherwise, the structure will increase the delay amount larger than one clock cycle in the system which cannot be compensated by the above structure in Fig.4.10. The method to make sure that the modulator in Fig.4.10 can compensate the delay amount is that the LF of it should be identical to (4.6). After solving the equations we can get the new coefficients of

Fig.4.10 for the low frequency case.

$$k_{df0} = \frac{1}{4}k_2(2+\frac{1}{2}k_1)$$
$$k_{df1} = \frac{k_1}{1+\frac{1}{2}k_1}$$
$$k_{df2} = k_2(1+\frac{1}{2}k_1)$$
$$k = \frac{k_{df0}}{2k_{df2}} \tag{4.9}$$

Compare the structure of Fig.4.10 and Fig.4.9, there is no additional adder before the quantizer and the structure of Fig.4.10 can be further simplified actually: the feedback path added to k can be combined to one signal path which is the sum of 1 and k. And the summation function in Fig.4.10 is realized by the summing of feedback current.

4.3.3 ELD COMPENSATION WITH PI-ELEMENT

Fig.4.10 is a simple method to compensate the ELD effect compare with the traditional technique; however, there are also additional DACs and some digital elements to realize it. Hence, another topology which is called Proportional-Integrating-element (PI-element) structure, as depicted in the following Fig.4.11 [26][27]. This structure has simplified the structure by combining the inner two loops together. And similar as previous discussion, the NTF of this structure also should identical to (4.6).

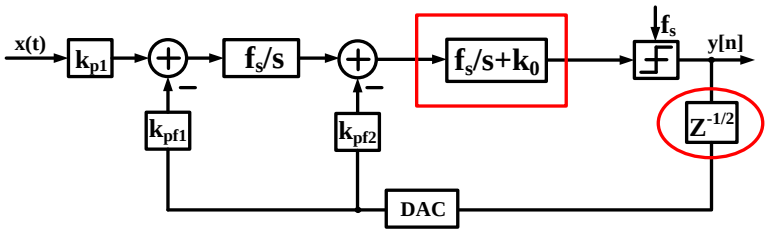

Fig.4.11 The PI-element ELD compensation method.

After setting the NTF of this PI-element structure equal to (4.6), the new coefficients in terms of k_{f1}, k_{f2} (Fig.4.3 (b)) in Fig.4.11 can be got, and they are given by (4.10).

$$
\begin{aligned}
k_{p1} &= k_{pf1} = k_1 \\
k_{pf2} &= \frac{1}{2}k_{f2}\left(1+\frac{1}{2}\frac{k_1}{k_{f2}} \pm \sqrt{1-\frac{k_1}{k_{f2}}-\frac{1}{4}\frac{k_1^2}{k_{f2}^2}}\right) \\
k_0 &= \frac{\frac{1}{4}k_{f2}\left(2+\frac{1}{2}\frac{k_1}{k_{f2}}\right)}{k_{pf2}}
\end{aligned}
\tag{4.11}
$$

Compare the technique in Fig.4.9 and Fig.4.11, the additional feedback path inside the red rectangular in Fig.4.9 has been compressed and expressed as an additional constant in Fig.4.11. However, during the progress we solve the equation to make sure the PI-elements compensation method works and the equations in (4.11), there is root square value exists. In order to make sure that the coefficients of Fig.4.11 make sense, i.e. the value under the root square should be real number. Hence, we can get the limitation of the PI-element technique:

$$
1-\frac{k_1}{k_{f2}}-\frac{1}{4}\frac{k_1^2}{k_{f2}^2} \geq 0 \tag{4.12}
$$

And of course, this limitation is under the condition that the delay amount is equals to half of clock cycle. And for the delay amount is not the exactly half of clock cycle, we have that

$$\tau_d \le \frac{\sqrt{2}-1}{k_1} \tag{4.13}$$

Here τ_d is the delay of the modulator; it should be less than one of clock cycle. And of course it also should satisfy the above (4.13). Except the condition that the delay amount should satisfy (4.13), the PI-element compensation method is low power consumption and easily circuit implementation compare with other existed compensation method.

As the discussion of alternative integrators in previous section, there are lots of structures to implement the integrators. For the active RC integrator, in order to implement the constant k_0, the following Fig.4.12 shows the realization of PI-element block in Fig.4.11 [27].

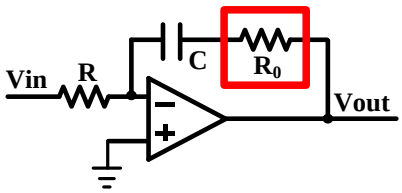

Fig.4.12 Realization of a PI-element for ELD compensation for an active RC integrator

The transfer function of the above Fig.4.12 is

$$\frac{V_{out}}{V_{in}} = -\left(\frac{1}{sCR} + \frac{R_0}{R}\right) = -(kf_S + k_0) \tag{4.14}$$

The extreme interesting point of the above PI-element compensation method is that whenever there is an additional resistor R_0 in series of the capacitor C, the constant can be implemented by the ratio of two resistors. This constant can be easily controlled accurately since the matching of resistors can be easily realized by layout position.

4.4 SUMMARY

This chapter introduces the ELD effect of a CT ΔΣ Modulator, it is discussed in two different feedback types: RZ feedback and NRZ feedback. For the RZ feedback pulse, there is coefficients mismatch of the modulator and the ELD will increase the order of modulator when NRZ feedback is used. The ELD may make the modulator unstable when it is large enough to push the poles of the modulator out of the unit cycle. Since the ELD will decrease the performance of the modulator significantly, the compensation method is necessary. There are lots of compensation method exist, this chapter introduce the traditional compensation method, the compensation method with a digital differentiator and the PI-element method. The traditional compensation method can compensate the delay amount up to one clock cycle, however, it need one additional feedback path in front of the quantizer and the active element which will consume more power to realize the additional adder. And in order to reduce the power consumption and make the compensation structure easily, a digital differentiator is introduced. This differentiator makes the summation in front of the input of last integrator. This technique is simpler compare with the traditional compensation method. And there is one simpler method existed, PI-element method which just introduces the constant to realize the compensation method is introduced. In the active RC integrator, the method can be implemented by introduce one resistor in series of the capacitor. However, this simpler method has its own limitation, the delay amount of the modulator should satisfy with certain condition. And the last integrator should be well designed with high slew rate and large bandwidth.

CHAPTER 5

AN ELD TRACKING COMPENSATION TECHNIQUE FOR ACTIVE-RC CT ΣΔ MODULATORS

5.1 INTRODUCTION

Because CT ΔΣ modulators have the benefits of low power consumption, small silicon area, and large signal bandwidth, it is very commonly implemented in the wideband telecommunication system. Besides, it has the inherent anti-aliasing function with low power dissipation and oversampling techniques. The performance of the modulator will be influenced by the core component: integrator dramatically [15]. Active RC, gm-C and MOSFET-C are mainly three types of architectures, to implement the integrators in CT ΣΔ modulators Although the active RC integrator consumes more power, it is usually the most commonly used one compared with the other two structures as its higher linearity [14]. Besides, it can provide a wider range of signal swing with deep-submicron technologies. On the other hand, compare with the corresponding DT case, ELD will affect the performance of the CT ΣΔ modulator significantly [14][15][29]. When there is NRZ feedback pulse implemented, then a part of it will be extended into the coming next period, hence, the transfer function will increase order due to this extension of the signal theoretically. The Noise Transfer Function (NTF) will be altered and even worse may cause the modulator to be unstable.

Excess Loop Delay (ELD) induced feedback DAC nonideality is a dominant factor causing error in the transfer function of CT ΣΔ modulators and eventually leading to instability. And as discussed in the previous chapter, there are lots of

compensation techniques for the ELD effect. This paper will propose a novel compensation scheme to track ELD when NRZ feedback is used, by comparing with the existing compensation methods, and then the delay amount will be compensated correspondingly by an RC feedback network and using digital logic elements. There are two advantages of using this technique: 1) compensation amount of ELD is tracked synchronously on a real-time modulator; 2) simple implementation of digital logic elements.

A 2nd order CT ΣΔ modulator with 1-bit DAC was built at transistor-level in 65nm CMOS to demonstrate the efficiency of the method. By using the proposed technique, the Cadence simulation results depict that the modulator can track the ELD up to 50% of the clock period duration and compensate it, leading to 69.2dB SNDR when compared with the ideal value of 70dB SNDR

5.2 ELD TRACKING COMPENSATION METHOD

As discussed in the previous chapter, ELD effect is more dramatically when the feedback pulse is NRZ shape. The proposed novel compensation method is with the NRZ feedback. And in order to make our discussion simpler, the single-bit quantizer case is also used. Fig.5.1 shows the single-bit NRZ DAC pulse in different cases: a) with a certain amount of delay τ_d, b) ideal case.

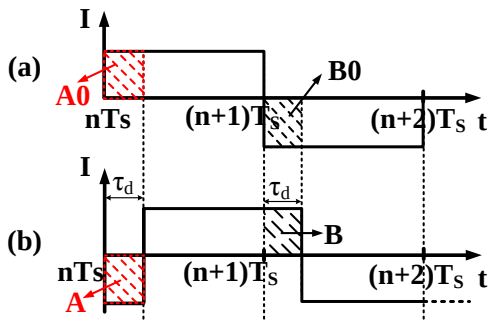

Fig.5.1 NRZ DAC pulse with: a) ideal case, b) with a certain amount of delay τ_d

When we compare the ideal waveform and that in Fig.5.1 (b), the ideal case is with positive area A0, but the real circuit is with the negative area A, hence there is the error of the feedback path; on the other hand, there is a redundant positive area B in the subsequent clock cycle. Since 1-Bit DAC is used, as well as B0 and B, A0 and A are equal. In order to compensate the delay effect, the lacked area A0 should be added back and the redundant area B should be subtracted in the subsequent clock cycle. Compare these two waveforms, if the area in the first clock cycle can equal to that in the ideal case, then the compensation method works. One possible solution is that, the lacked area can be added back during the time interval after the delay τ_d and before the coming next clock cycle, and similar compensation idea can be used for the coming next clock cycle. Hence, the waveform of the proposed method is realized and as appeared in Fig.5.2.

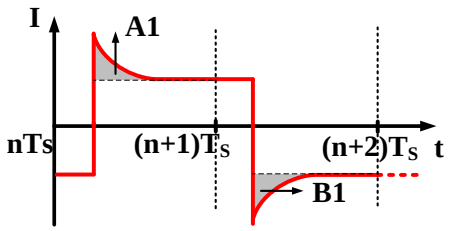

Fig.5.2 Waveform of the proposed compensation technique.

In the above Fig.5.2, grey areas A1 and B1 should be the double of A0 and B0, respectively. The working principle of the proposed ELD tracking compensation technique implies the determination of the delay amount, and after that the lacking/redundant area is added /subtracted by A1/B1.[28][30]also utilize the similar principle, but this technique can reflect the real-time ELD value with simple implementation. [31] which introduces the method to get the coefficient of the compensation path with the time domain equivalent theory is implemented in our case.

5.2.1 WORKING PRINCIPLE OF COMPENSATION COMPONENT

Fig.5.3 illustrates the block diagram of the proposed compensation technique. Compare with a traditional ideal 2nd order CT ΣΔ modulator, it has an additional Compensation Component (CC). It contains the RC feedback network. and the CLG Control Logic Generator (CLG)controls the PMOS/NMOS switches SP/SN in the RC feedback network to charge/discharge capacitor CC, that is the capacitor CC contains the lacking/redundant feedback amount due to delay.

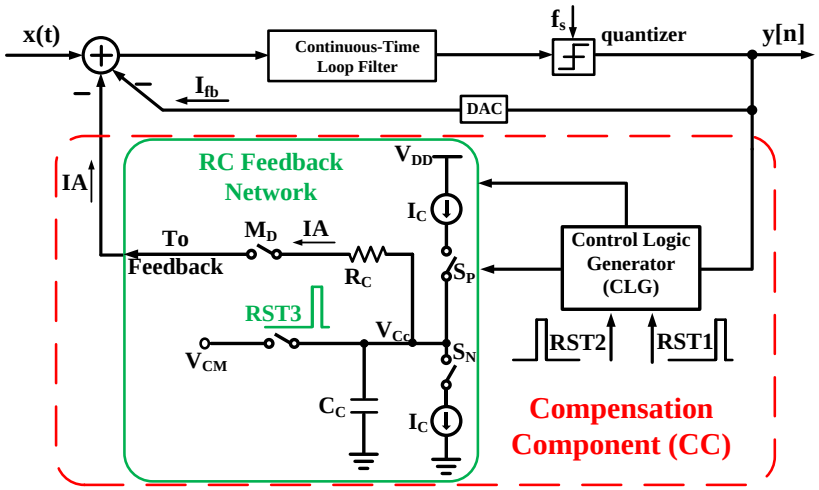

Fig.5.3 Block diagram of the proposed ELD tracking compensation technique

The switch MD controls the compensation amount, which will be added back to the main circuit, and this MD signal is controlled by CLG. The waveforms of reset signals and the clock in compensation component are depicted in following Fig.5.4.

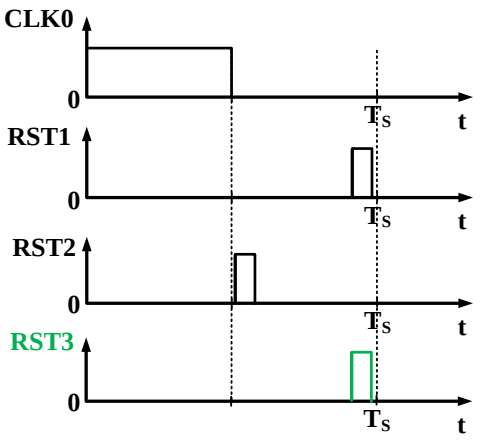

Fig.5.4 Clock and reset signals for Compensation Component (CC).

The quantizer sampling clock signal is CLK0, the switches SP and SN are reset by RST2, and the charge restored in capacitor CC is reset by RST3. The implementation of the CLG is exhibited in Fig.5.5 and the overall working principle of the proposed ELD compensation technique is illustrated in Fig.5.6.

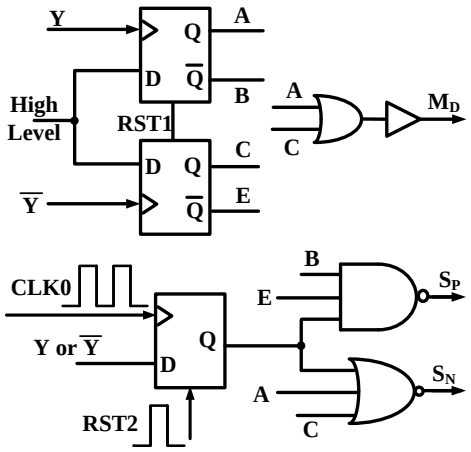

Fig.5.5 Implementation of the Control Logic Generator (CLG) with digital logic.

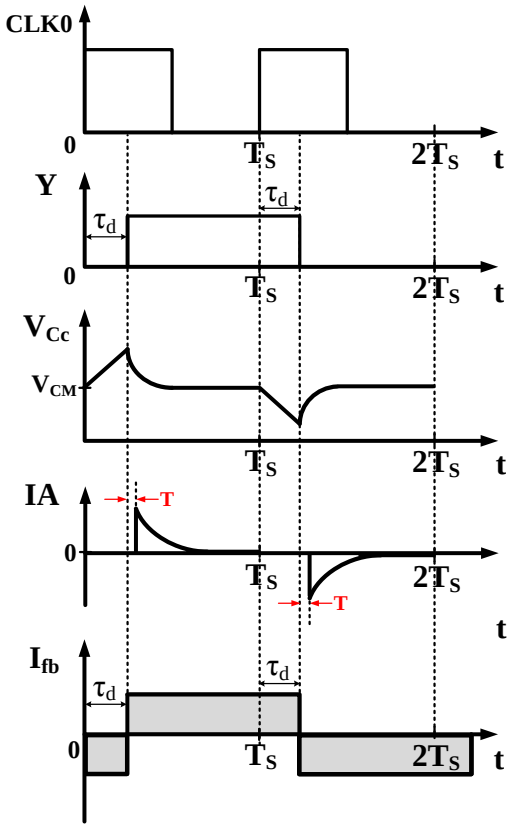

Fig.5.6 Illustration of the proposed ELD tracking compensation technique.

I_{fb} is the current of the traditional CT ΣΔ modulator feedback path (as in Fig.5.3) in Fig.5.5. In order to make our discussion simplicity, the value of Y is assumed to be with initial value 0, which is the input signal to Cc. And the operation principle of the proposed technique will be analyzed in the following several conditions:

There is delay τ_d in the quantizer output Y and the I_{fb} which is the feedback current compare with the CLK0 waveforms of Fig.5.6. Then the subsequent period contains a redundant amount and a lack amount within the period $[0,T_S]$. Our task is to subtract the redundant amount and add back the lack amount in each period to the original circuit. Based on Fig.5.5, both the NMOS and the M_D switches will be turned off and the PMOS switch (S_P in Fig.5.3) will be turned on according to CLG component. In addition, as shown in Fig.5.6, the voltage V_{Cc} will increase linearly and Cc contains the lacked charge of the feedback current which is due to ELD effect.

At time instant τ_d, both PMOS and NMOS switches turn off because the signal Y is rising from 0 to 1. However, the lack amount due to the ELD effect will be compensated because of the turn on of switch M_D,.

At time instant T_S, based on the assumption from Fig.5.6 that Y is maintained the same, the NMOS switch turns on and the PMOS switch turns off. The voltage V_{Cc} drops from VCM to a lower level according to the current direction through the capacitor C_C.

At $T_S + \tau_d$ time instant, the signal Y changes from high to low but with delay and both NMOS and PMOS switches turn off. Because V_{CM} is larger than the voltage V_{Cc}, the voltage differences between these two. Therefore, the redundant current amount is subtracted from the main circuit through the capacitor.

Besides, there is condition that in two consecutive periods nT_S and $(n+1)T_S$ there are no signal changes. If so, either NMOS or PMOS (i.e. one CMOS switch) is opened from time nT_S to $(0.5+n)T_S$ to discharge/charge the capacitor C_C. Therefore, there is changing of the voltage V_C. The only difference is that the signal in the PMOS or NMOS switches will be reset by RST2 signal at the time instant $(0.5 + n)T_S$. Furthermore, the switch M_D turned off because of the unaltered Y; as in Fig.5.4 and in order to allow the compensation component to work properly, V_{Cc} equals to VCM for the forthcoming period is set by RST3.

5.2.2 DELAY ISSUES OF COMPENSATION COMPONENT

Fig.5.5 shows that the performance of the modulator may be dramatically reduced by the extra delay which is caused by the logic elements, in high speed CT ΣΔ modulators condition maybe especially worse. The position of RC feedback pulse IA may be varied and the amount of charge Q stored in capacitor C_C may also be changed, both of them are due to this delay. Both of these two effects will be analyzed in detail separately.

Let's firstly focus on the charge amount issue. Based on the previous introduction, capacitor C_C is charged/discharged according to the current I_C which is controlled by the switch S_P/S_N during the delay $\tau_{d,}$. The time interval (that starts with the turning on of the switch S_P/S_N, to charge C_C, and the time when the switch turns off) controls the charge amount Q in the capacitor. The response time for the trigger signal to turn on switch S_P/S_N (as depicted in Fig.5.7) can be marked as delay T1, and the delay caused by switch S_P/S_N to turn off is T2.

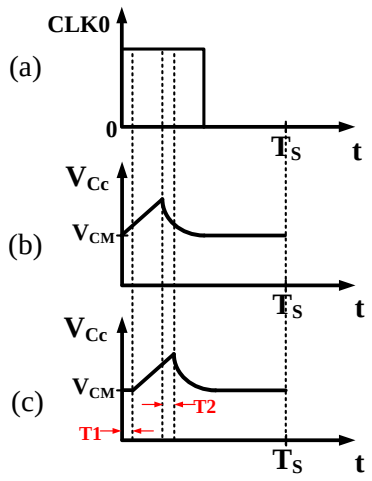

Fig.5.7 Waveforms of a) CLK0 b) theoretical V_{Cc} c) V_{Cc} with delay considered

The theoretical value can be achieved by the charge Q if T1 and T2 are equal; otherwise, an offset appears and leads to the failure of compensation technique. Fig.5.5 shows that a D Flip-Flop and a NAND/NOR gate with 3 inputs' response time produces T1. T1 is produced by the same reason as T2, that is T1 and T2 are definitely equivalent. Hence, in CLG, the theoretical charge value can be achieved easily the in capacitor C_C (considering the delays T1 and T2), and the modulator's performance does not be affected by both the delays T1 and T2.

Secondly, response time of the switch controller MD will produce a delay T. Fig.5.6 shows that the delay T will shift the feedback current waveform. With different values of the time constant τ, the behavior of the current IA of the RC feedback network is depicted in Fig.5.8, which leads to different capacitor discharge times.

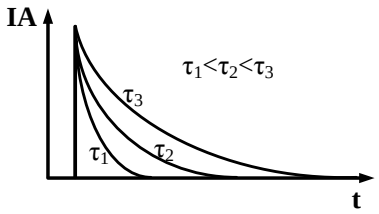

Fig.5.8 Current IA of the RC feedback network for different values of the time constant τ.

The charges are released at a quicker pace if the value of the time constant is smaller. According to this knowledge, , the performance will not change even though there is the delay T if the charge in capacitor C_C can be released almost completely. The time constant τ of the RC network should be carefully picked to maintain the performance since: 1) the charge on capacitor C_C may not be released completely if RC is too large. 2) It may imply a very large peak value of the current even though the charge on capacitor C_C can be released completely if RC is too small. Next section will illustrate a design example with adequate choices of C_C and RC in detail.

5.3 DESIGN EXAMPLE AND SIMULATION VERIFICATION

A low-pass 2nd order single-bit CT ΣΔ modulator was modeled and further tested the workable of the technique based on the proposed architecture of Fig.5.3 in 65nm CMOS with Cadence design tools. The sampling rate of the designed modulator is 250MS/s, the OSR is 64 and the input bandwidth is 2MHz to match with the standard of 3G WCDMA receivers. The input signal is set with amplitude P_{in}= –4.43dBFS. The coefficients of the CT ΔΣ modulator are scaled down to avoid the signal swings saturating to the loop filter. In addition, based on the time equivalent theory from [28] [31], the shape of the waveform of the CT outputs within the [0, 1] period is irrelevant; the value at the sampling time t=nT mattered. According to the calculation results, a proposed compensation path to the second integrator is needed, and the compensation current I_C should be 3 I_{fb2} (feedback current of the second integrator in an ideal second order CT ΣΔ modulator) [31][32]. The time constant value τ which is

composed by C_C and RC should be determined according to the figure in Fig.5.3 and Fig.5.6. From the definition of RC feedback network (whose expression is an exponential one) and Fig.5.8, the charge in the capacitor C_C cannot be completely released. Hence, based on the knowledge of probability statistics, the settle error tolerance can be achieved. The settle error tolerance can be defined by the following expression to get the suitable time constant τ:

$$N = \frac{T_S - \tau_d}{\tau} \tag{5.1}$$

Equation (5.1) gives that smaller N leads to larger τ. The delay τ_d up to half clock cycle is supposed to track and compensate in our case. When τ_d=0, that is there is no delay existed which is one of the extreme case and the other one is with the largest delay amount up to half of clock cycle, then τ_d =0.5T_S. Therefore, for a modulator that contains half cycle delay and there is an RC network (which can release the charge almost completely), then the delay amount is less than half cycle case is also acceptable. Fig.5.9 gives the settle error tolerance of the RC feedback network.

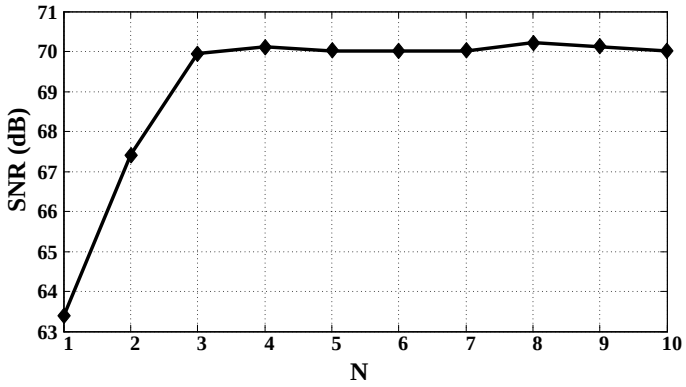

Fig.5.9 Settle error tolerance of the RC feedback network.

The modulator with stable performance when the value of N is bigger than 3, the performance almost reach the ideal case. According to the knowledge of N and τ (smaller N leads to larger τ), fixed C_C with small RC will lead to good performance (when the effect of high peak current is excluded). This results matches with the simulation outputs. N=4 is picked according to the above discussion and the above

Fig.5.9. Hence, with C_C is selected as 1fF, RC equals to 500Ω. Simulation result gives a 69.2dB SNDR, compare with 70dB of ideal 2nd order one. Fig.5.10 gives the power spectrum density (PSD) of two different cases.

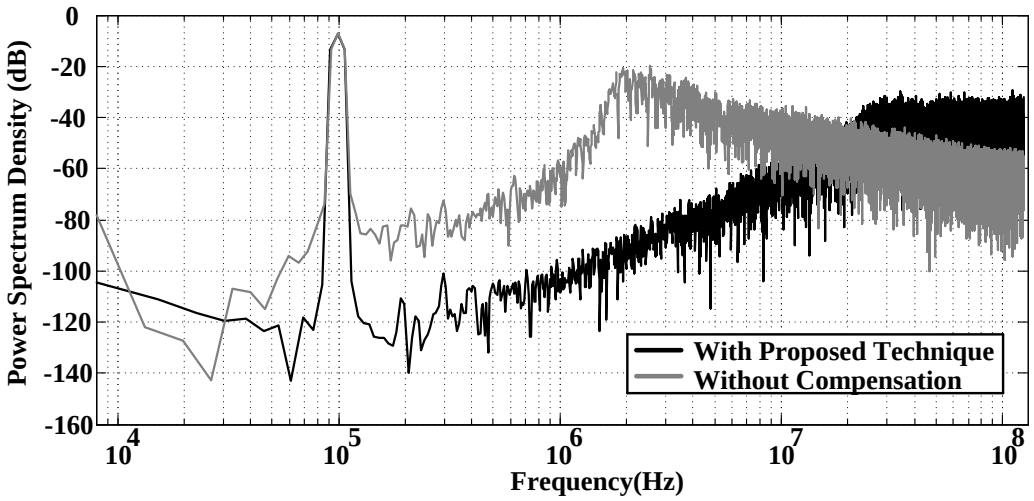

Fig.5.10 Comparison of simulation results for 2 different cases when there is 50% Ts delay in the quantizer.

The proposed technique in a 2nd order CT ΣΔ modulator with the ELD sensitivity of system is presented in Fig.5.11. The system can tolerate the delay amount up to half of clock cycle.

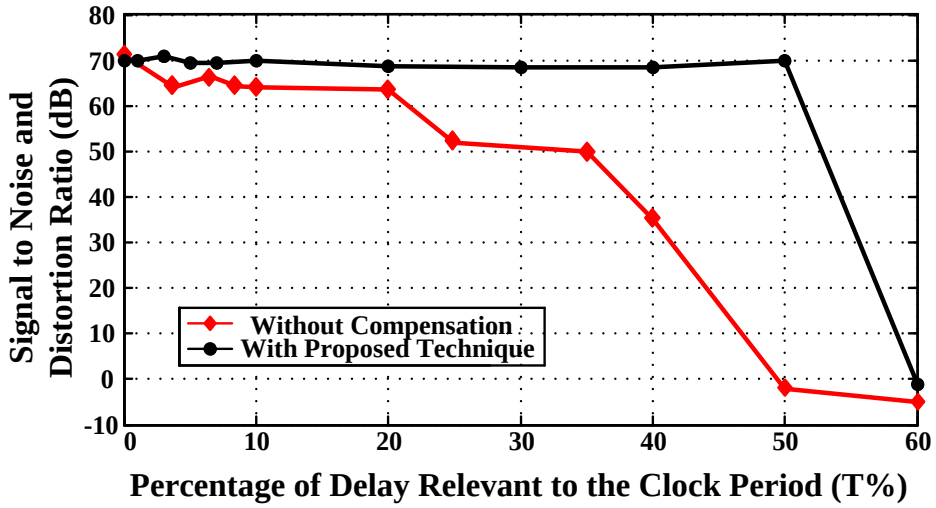

Fig.5.11 Simulation results for system sensitivity to ELD in a 2nd order CT ΣΔ modulator with or without the proposed compensation technique.

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After getting the above simulation results, the comparison between this work and the existed traditional compensation technique is shown in the following table.

Table5. 1 THE COMPARISON BETWEEN THIS WORK AND EXISTED ONES

	SNDR (dB)	Power (mW)	Can Compensate Delay (T_S)	Added Element
With delay no compensation	Unstable	/	/	/
With delay with proposed compensation	69.2	5.45	50%	Digital Elements, RC Feedback Network
Ideal Case	70	5.3	/	/
Traditional compensation	69	6.5	Up to 100%	An Adder, An extra feedback path

5.4 SUMMARY

A novel technique to compensate the effect of ELD in CT ΣΔ modulators is illustrated in this chapter. In order to track the ELD, there is only a few digital logic elements utilized, and then an RC feedback network is implemented to either subtracts the redundant charge or compensate the lacking charge back. NRZ feedback pulse and delay amount up to half of clock cycle is used in a 2^{nd} order CT ΣΔ modulator to verify the technique. Simulation results in 65nm CMOS proves that up to half of clock cycle loop delay can be recorded and then completely compensated, the final 69.2dB SNDR is close to the ideal 70dB. In comparison, if there is no compensation technique used with the same condition, the modulator is unstable, which further prove the workable of the technique.

CHAPTER 6

A PASSIVE ELD COMPENSATION TECHNIQUE FOR GM-C BASED CT ΔΣ MODULATORS

6.1 INTRODUCTION

The CT ΣΔ modulator is very sensitive to clock jitter and ELD, which can degrade the system performance very seriously [15]. An effective option to reduce the clock jitter influence is the utilization of NRZ feedback in the CT ΣΔ modulator. But, NRZ feedback is more sensitive to the ELD effect. Therefore, tradeoffs must be made between choosing feedback modes in the DAC topology and its performances.

As mentioned in Chapter 4, ELD is normally induced by the nonzero switching time of the transistors in the quantizer and the DAC. It will shift a part of the feedback pulse into the next clock cycle. A certain amount shift of the feedback pulse will increase, mathematically, the order of the modulator, hence the loop stability may not be guaranteed under the ELD effect. Due to the serious effect of ELD in the CT ΣΔ modulator with NRZ feedback, several compensation methods have been proposed. However, most of them focus on CT ΣΔ modulators using an active RC loop filter. As one of the other most widely used integrators in the CT ΣΔ modulator, the Gm-C filter exhibits the benefits of inherent simplicity of the active elements with their open loop operation, which results in a high-speed potential and generally a small excess phase and power dissipation [14]. Thus, in this chapter, a technique to compensate the ELD in CT ΣΔ modulators using Gm-C loop filter is presented. The proposed circuit architecture uses a resistor in series with the integration capacitor to obtain a feed-forward adder in the Gm-C integrator. The proposed ELD compensation is based on

the PI - element method for low power dissipation and simple implementation, and it is verified through the design of a 2nd order CT ΣΔ modulator which uses a Gm-C integrator as the 2nd stage of the loop filter. To further demonstrate the efficiency of the technique a NRZ feedback is utilized due to its larger sensitivity to ELD. Simulation results show that a 68.9dB SNDR can be achieved with an ELD close to half clock period, while the system will be unstable without compensation for such an amount of the loop delay. These results confirm the effectiveness of the proposed ELD compensation method in Gm-C filter based CT ΣΔ modulators. Hence, the following of this chapter will introduce the technique in detail.

6.2 PROPOSED TECHNIQUE WITH GM-C INTEGRATOR

Since ELD can significantly reduce the SNDR of a CT ΣΔ modulator its effect will be analyzed in detail in a 2nd order CT ΣΔ modulator. Fig.6.1 shows the diagram of an ideal 2nd order CT ΣΔ modulator composed by a Cascade of Integrators in Feedback (CIFB)[29]. CIFB topology has advantages over the Cascade of Integrators in Feedforward (CIFF) due to better intrinsic antialiasing and lower susceptibility to the peaking of signal transfer function (STF) [29].

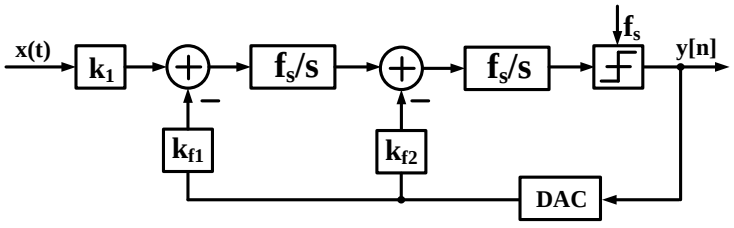

Fig.6.1An ideal 2nd order CT ΣΔ modulator with CIFB topology.

The 2nd order modulator enjoys better stability when compared to higher order systems and its coefficients (shown in Fig.6.1) can be obtained by transferring the corresponding DT coefficients into the z-domain. Besides, the standard form of its NTF is the following:

$$NTF = (1 - z^{-1})^2 \tag{6.1}$$

And as mentioned in the Chapter 4, there are lots of compensation methods. Compare with classical technique, another structure designated by Proportional-Integrating element (PI-element) has been introduced, illustrated in Fig.4.11, which combines together the two inner loops of the previous topology [27]. Similarly, the NTF should be equal to (6.1). By matching the NTFs, the new coefficients of the system in Fig.4.11 can be expressed in terms of kf1, kf2 (Fig.4.3), and they are given by (4.11).

Most previous works focus on the implementation of the ELD compensation in CT ΣΔ modulators with RC integrators, but, here, the proposed technique will concentrate in the design of an ELD compensation structure with PI-element utilizing Gm-C loop filters, due to the advantages previously mentioned and that will be further analyzed next.

The proposed technique is based on the compensation theory shown in Fig.4.11 and utilizes at its core the Gm-C integrator. The general structure of such integrator is illustrated in Fig.6.2, where the input voltage is transferred by the transconductor Gm to the output current which is integrated in the capacitor producing a voltage drop. This operation principle can be described as here below:

$$\frac{V_o}{V_i} = \frac{g_m}{sC} = k\frac{f_s}{s} \tag{6.2}$$

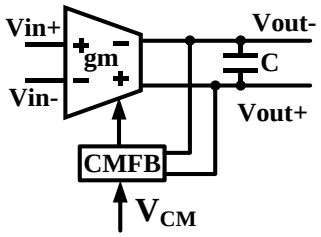

Fig.6.2 Fully differential Gm-C loop filter with CMFB

Comparing this equation with the function presented in the red rectangular block shown in Fig.4.11 it can be found that the constant item k0 should be generated in order to implement the PI-element with a Gm-C integrator. And, due to the definition of transconductance, if gm is multiplied by R then a constant will arise, which in circuit terms, to match with the theoretical diagram of Fig.4.11, can be achieved by the structure of Fig.6.3. Where, the corresponding voltage transfer function can be derived as:

$$\frac{V_o}{V_i} = \frac{g_{m1}}{sC} g_{m2} R + g_{m3} R \tag{6.3}$$

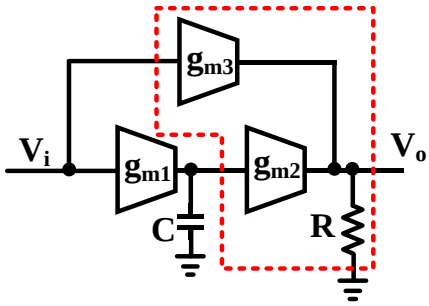

Fig.6.3 Basic concept for ELD compensation with PI-element using Gm-C integrator

After applying the structure shown in Fig.6.3, the equation (6.3) can be realized, hence, the PI-element compensation technique is implemented. However, it is also obviously that in order to implement the feedforward path, two extra transconductors are needed, which will lead to additional power consumption due to its active circuit implementation. Hence, with this disadvantage, the circuit from Fig.6.3 is not the preferred choice to obtain the function fs/s+k0 from Fig.4.11 at circuit level, and a passive solution must be sought.

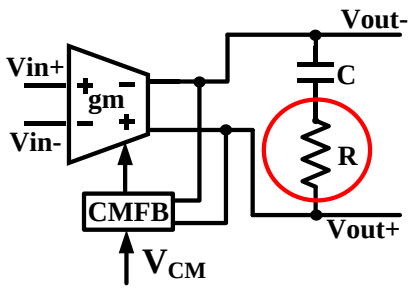

Fig.6.4 Proposed ELD compensation with PI-element using Gm-C integrator with passive implementation

One possibility is illustrated in Fig.6.4 where the voltage transfer function is given by:

$$\frac{V_o}{V_i} = \frac{g_m}{sC} + g_m \times R = k\frac{f_s}{s} + k_0 \tag{6.4}$$

and it requires only one additional resistor to obtain the same NTF as in the classical structure, significantly reducing the circuit complexity. Traditionally, at least one adder and one extra DAC should be used (Fig.4.9) which will complicate the circuit and increase the power consumption. Here, instead, the additional resistor R is used to realize the feedforward function and finally to have NTF equal to (6.1). Another benefit of this structure is the smaller loading at the output of the Gm-C integrator when compared with the original circuit from Fig.6.3, which can enhance the transconductor's speed and reduce the lower power consumption[14][33]. However, a drawback of this passive structure is related with the parasitic capacitance C_P that exists on the 2 terminals of the integrating capacitor, as depicted in Fig.6.5.

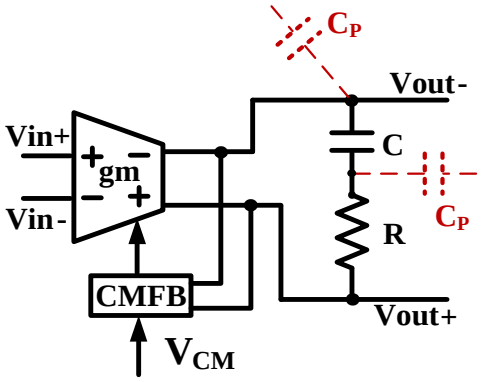

Fig.6.5 Proposed PI-element ELD compensation with parasitic capacitor C_P

The figure shows above is with parasitic capacitor C_P, it will directly inflect the transfer function of the integrator. Hence, if there are parasitic capacitors C_P, (6.4) cannot be maintained.

To overcome this, a modified improved structure is given in Fig.6.6. Here, the original C and R are separated into two identical branch elements connected in series between the 2 differential outputs of the transconductor and the ground

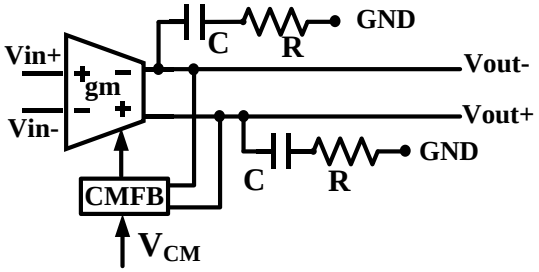

Fig.6.6 Modified improved ELD compensation with PI-element using Gm-C integrator structure.

This new modified Gm scheme, when introduced in a classical ELD compensation with Gm-C integrator (Fig.6.7) [34], allows the removal of the transconductor Gm that operates as the adder and the additional feedback path, simplifying the whole circuit structure and reducing power consumption.

Furthermore, extra elements can be realized by using only additional resistors.

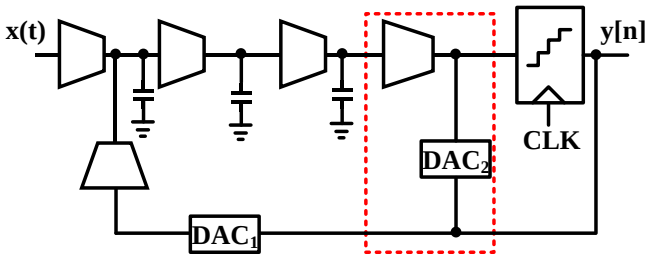

Fig.6.7 Traditional ELD compensation with Gm-C integrator in CT ΣΔ modulator.

6.3 DESIGN EXAMPLE OF CT ΔΣ MODULATOR

In order to verify the proposed technique shown in Fig.6.6, a 2nd order, single-bit, low-pass CT ΣΔ modulator was designed based on the system diagram of Fig. 4.3 (b), with a sampling rate of 250MS/s. The input bandwidth is 2MHz corresponding to the standard of 3G WCDMA receivers and the OSR is 64. NRZ feedback was chosen. The transformed CT coefficients were scaled down to guarantee that the signal swing will not reach the saturation level of the loop filter.

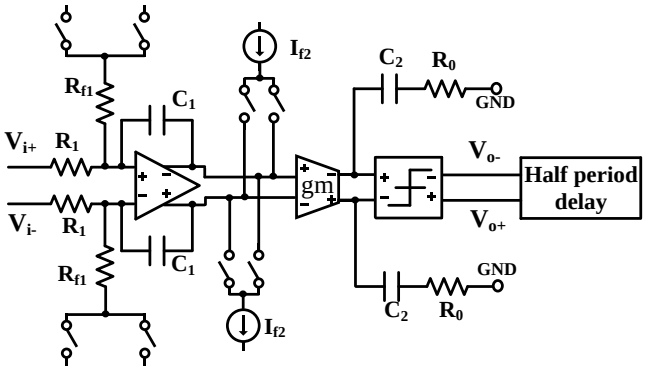

Fig.6.8 Circuit schematic of the proposed ELD compensation structure with Gm-C integrator in a 2nd order, 1-bit, CT sigma-delta modulator with NRZ DAC.

The overall circuit schematic of the modulator is given in Fig.6.8, which was implemented in 65nm CMOS with 1V supplied voltage. And, since the requirement of

the second loop filter is released, a Gm-C loop filter can be used to save power, enhance the speed and simplify the circuit. Then, the circuit of Fig.6.6 was employed in the second loop filter to obtain the compensation with PI-element of Fig.4.11.

The calculation of the system coefficients with ELD compensation leads to: kp1= 0.125, kpf1= 0.125, kpf2= 0.1692 and k0= 0.646. Then, based on (5) and the working principle of RC integrator, the parameters of all the circuit elements in Fig.6.8 can be obtained. Moreover, some considerations to get the value of resistors and capacitors can be made: the resistors can generate thermal noise; hence their values should not be too large. One the other hand, if the classical compensation method was used, the corresponding coefficients will be: kc1= 0.125, kcf1= 0.125, kcf2= 0.25 and kc0= 0.11. The values of the feedback coefficients are related to the power consumed by the feedback DAC. And, by comparing the feedback coefficients in the two structures, it can be found that by using the proposed method the value of the feedback coefficients in the first stage is reduced from 0.25 to 0.1692, which will imply a power reduction of close to 32%.

6.4 SIMULATION VERIFICATION

The proposed compensation technique was implemented in a CT ΣΔ modulator and verified by transistor-level simulations. Fig.6.9 shows the simulation results of the same modulator in two different cases, with and without ELD compensation.

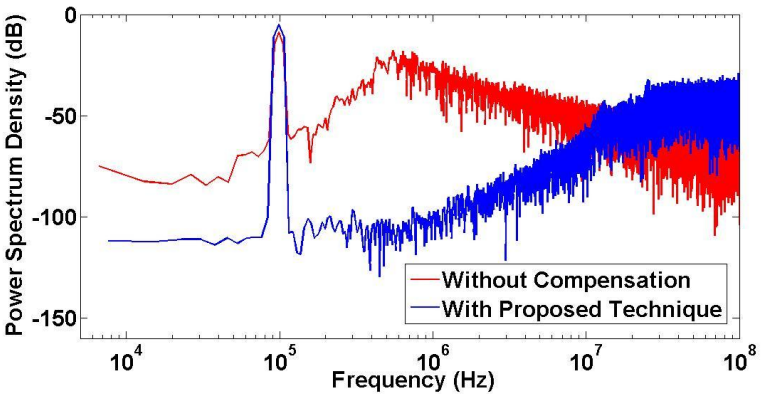

Fig.6.9 Comparison of simulation results for 2 different cases when there is 50% Ts delay in the quantizer

A value of 50% of TS was added as delay in the system loop. The result exhibited by the red line shows the simulated PSD of the modulator without ELD compensation. It can be seen that its noise floor is much higher than that of the compensated system employing the proposed ELD technique (blue line); and also the noise shaping function has been distorted due to the change of the NTF. Basically, the system cannot work normally under 50% TS loop delay without ELD compensation, in particular also because of the NRZ feedback. Then, the new circuit structure can achieve 68.9 dB SNDR which is close to an ideal case. The performance difference is mainly due to the differences between the noise-shaping curves. From the simulation results, for a general CT ΣΔ modulator, 50% Ts loop delay is large enough to imply the failure of the noise shaping function and destabilize the system. By contrast, after applying the proposed technique, the ELD effect can be compensated and the SNDR increases close to the ideal case. Theoretically, the proposed new scheme can compensate the loop delay if not larger than half clock period, as it can be seen in Fig.6.10, where the ELD tolerant ranges for the designed 2nd order CT ΣΔ modulator with and without the proposed ELD are provided.

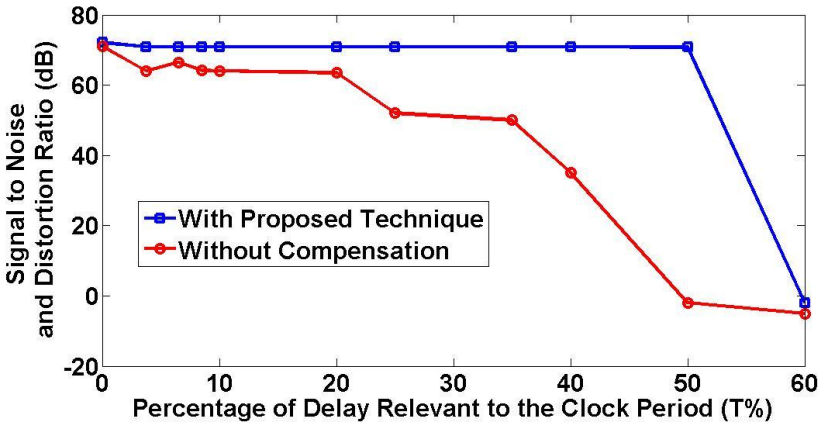

Fig.6.10 Simulation results for system sensitive to ELD in a 2nd order CT ΣΔ modulator with proposed compensation technique and without compensation

Similar with the previous condition, the comparison between this technique and the previous existed structures are presented in the following table. From the table we can find that besides the benefit of low power dissipation in Gm-C integrator, the power was reduced up to 32% with the help of this proposed technique.

Table6. 1 COMPARISON BETWEEN PROPOSED TECHNIQUE AND THE EXISTED STRUCTURES

	SNDR (dB)	k_{f2}	k_0	Can Compensate Delay (T_S)	Added Element
With delay no compensation	Unstable	/	/	/	/
With delay with proposed passive Gm-C compensation	68.9	0.1692	0.646	50%	Resistors
Ideal Case	70	/	/	/	/
Traditional compensation structure [34]	69	0.25	0.11	Up to 100%	Additional Transconductors, An extra feedback path

6.5 SUMMARY

This chapter has proposed a novel compensation technique and its corresponding circuit scheme to the ELD effect in Gm-C integrator based CT ΣΔ modulators. The new structure uses a resistor, in series with the integration capacitor, which works as the adder creating a feedforward function. Half clock period of loop delay could be tolerated after employing the proposed compensation. Comparing it with existing solutions, this new method is simpler in terms of circuit implementation and consumes less power. Its behavior was verified through the design of a 2nd order CT ΣΔ modulator with NRZ feedback and a 2nd stage Gm-C integrator. Simulation results show that with a loop delay of 50% of Ts the CT ΣΔ modulator without ELD compensation was unstable; by contrast, the proposed modulator achieved 68.9dB SNDR which is close to the ideal case, further demonstrating the effectiveness of the new scheme.

CHAPTER 7

AN ELD COMPENSATION TECHNIQUE FOR CT ΔΣ MODULATORS WITH HYBRID ACTIVE-PASSIVE (AP) LOOP-FILTERS

7.1 INTRODUCTION

Because of the merits that the dissipation power is low, silicon area is small, signal bandwidth is large, and the anti-aliasing function is inherent as well, the CT ΔΣ modulator has been extensively used in wideband telecommunication systems. Three main elements: integrator, quantizer and feedback DAC constitute a CT ΔΣ modulator. Integrator is the core component of the modulator and there are two categories: active integrator and passive one. Many structures can be implemented as the active integrators [27]. Active RC integrator is the most commonly used one since it produces higher linearity compare with other structures, though it consumes more power. However, power dissipation is an important consideration factor for telecommunication system [27]. Hence, CT ΔΣ modulator with hybrid Active-Passive (AP) integrators plays a more and more important role.

Though the CT ΔΣ modulator with hybrid AP integrators has the benefit of low power consumption, it is still sensitive to the effect of ELD, which is due to the non-idealities of the DAC and quantizer. Since in transistor level, the response time of the switches in DAC quantizer is not ideally zero, there should be the finite response time [15][28]. Due to ELD effect, when NRZ feedback is used, the feedback pulse will be shifted and a part of it will be extended into the consequent clock cycle which may lead to the un-stability of the system [25][35][36][37]. Since the ELD effect in the CT ΔΣ modulator will reduce the performance significantly, lots of compensation

methods have been proposed [25][27][33][35][36][37][38], and[26][39] even show the compensation for delay amount is more than one clock period. However, they are only applicable in full-active modulator due to the lack of the isolation in passive integrator [14] [40]. Because of the benefits of hybrid AP CT ΔΣ modulator, ELD compensation for hybrid case is also necessary. A design of ELD compensation technique for CT ΔΣ modulators with hybrid Active-Passive (AP) loop-filters is presented in this chapter. The design and optimization methodology for hybrid CT loop-filter is discussed. By appropriately scaling the passive filter gain and cooperating with single-bit quantizer, hybrid AP loop filtering can achieve approximated noise-shaping function as a fully active ΔΣ modulator. As a result of passive loop-filter cannot perform proportional feedback signal summation, classical ELD compensation technique cannot be practically applied in hybrid AP CT ΔΣ modulator. This work proposes an ELD compensation technique applied in the passive loop-stage in a hybrid CT ΔΣ modulator. A resistor added in the passive loop-filter is the only additional circuit component adopted to implement the proposed technique. The proposed ELD compensation technique achieves advantages of no active power consumption and easy circuit implementation. By applying the technique, the maximum quantizer delay tolerance can be a full clock period. The technique was applied in a designed 2nd order CT ΔΣ modulator with active-RC integrator as the 1st stage and passive RC filter as the 2nd stage. Its effectiveness was verified by transistor-level simulation in 65nm CMOS, and both one clock period and half clock period conditions have been corroborated. Simulation results show a 67.3dB SNDR under half clock period ELD effect and 65.3dB SNDR under one clock period ELD effect; by contrast, without compensation, the system is unstable in both half clock period and one clock period ELD effect. The designed hybrid CT ΔΣ modulator achieves 2MHz signal bandwidth and consumes 2.54mW power.

7.2 LOOP FUNCTION OPTIMIZATION WITH SINGLE-BIT QUANTIZER FOR HYBRID AP CT ΔΣ MODULATOR

To achieve faster rate of signal processing, CT loop-filters are more suitable candidates in the implementation of ΔΣ loop-filtering. A general procedure of CT ΔΣ loop-filter design starts on its Discrete-Time (DT) counterpart. A 2nd order DT ΔΣ modulator with CIFB loop architecture is shown in Fig.4.3 (a). By knowing the DT loop-filter coefficients, a1 and a2, and the impulse response of selected proper CT feedback DAC pulse, the corresponding CT loop coefficients can be obtained through Impulse-Invariant Transform (IIT).

The Loop transfer Function (LF) of the active CT ΔΣ modulator shown in Fig.4.3 is derived in (7.1).

$$LF_a(s) = -\frac{k_2 f_s (s + k_1 f_s)}{s^2}$$
$$k_1 = \frac{2a_1}{2 - a_1}$$
$$k_2 = a_2\left(1 - \frac{1}{2}a_1\right) \tag{7.1}$$

The expressions of k1 and k2 are for NRZ rectangular feedback case where a1 and a2 are the integrator gain of the corresponding DT counterpart. Because the output is quantized signal which is in DT domain, the CT LF is for the signal transferred from DAC output y(t) to the front of the quantizer u(t). The CT DAC response is involved into the calculation of loop-filter gain. Hence, a 2nd order hybrid AP CT ΔΣ modulator structure is shown in the Fig.7.1.

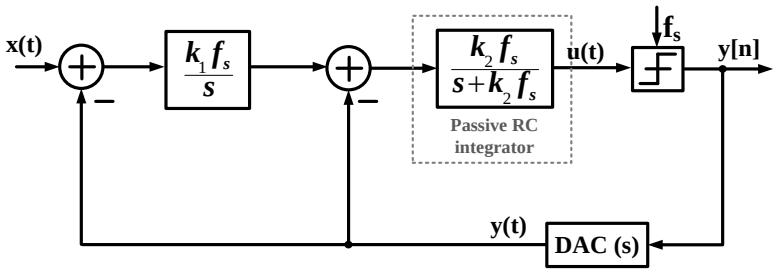

Fig.7.1 System architecture of hybrid AP CT ΔΣ modulator.

The *LF* for the hybrid AP CT ΔΣ modulator shown in Fig.7.2 is

$$LF_{ap}(s) = -\frac{k_2 f_s (s + k_1 f_s)}{s(s + k_2 f_s)} \tag{7.2}$$

where k1 and k2 are determined same as in (7.1). To observe the relocated pole-zero of the NTF for the hybrid AP CT ΔΣ modulator, the CT LF should be transformed into Z-domain since both of the quantization error and output signal are in DT. The equations given in (7.3) can be applied to determine the corresponding NTF. In this chapter, all the discussed feedback DAC pulses are rectangular.

$$\begin{aligned} NTF(z) &= \frac{1}{1 - LF(z)} \\ LF(z) &= Z\left\{ L^{-1}\left\{ LF(s)\, DAC(s) \right\}_{t=nT_S} \right\} \\ DAC_{NRZ}(s) &= \frac{1 - e^{-T_s s}}{s} \end{aligned} \tag{7.3}$$

By adopting NRZ feedback mode and applying (7.3), the pole-zero locations for the NTF of the active and the hybrid CT ΔΣ modulator are shown in Fig.7.2. Without loss generality, the sampling frequency is normalized to 1. The DT integrator coefficients are a_1 =0.5, a_2 =2 to achieve standard 2nd order differentiation to quantization noise.

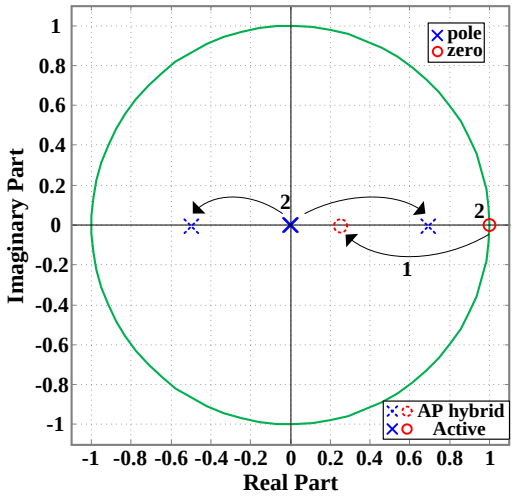

Fig.7.2 NTF pole-zero locations for the 2nd order active CT ΔΣ modulator and the hybrid AP modulator without optimization.

In Fig.7.2, for active CT ΔΣ modulator, the pole-zero locations conform to ideal 2nd order NTF, $(1-z^{-1})^2$. By contrast, for the hybrid AP CT ΔΣ modulator, one zero moves within unit-circle, it indicates that the NTF is only 1st order differentiation in a certain low frequency band. The separated poles affect the out-band response of the NTF. The analytical NTFs over frequency for the active and the hybrid AP CT ΔΣ modulator are shown in Fig.7.3. Because one zero moves to high frequency, the hybrid AP modulator achieves only 1st order in-band noise-shaping function.

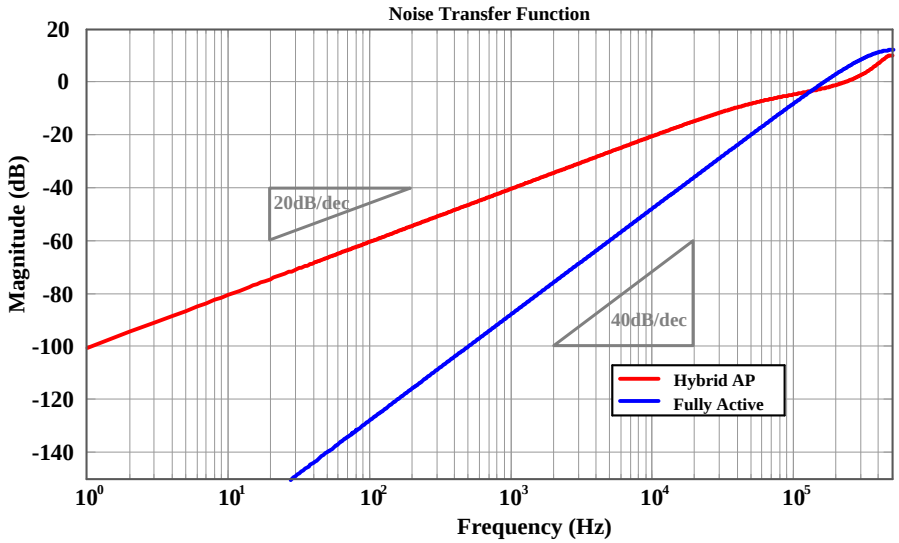

Fig.7.3 Calculated NTF for the un-optimized hybrid AP and the active CT ΔΣ modulator

To approximate the *LF* for the hybrid AP modulator to the ideal active form given in (7.1), a feasible way is to move the non-DC pole in (7.2) to as low frequency as possible. However, scaling down k_2 also decreases the filter gain which will increase IBN floor. In general case, this issue should be compensated by increasing the quantizer gain so that the total loop gain can be fixed; for using multi-bit quantizer, this solution requires to compress the conversion reference range which significantly increases the precision requirement. However, in the modulator employing single-bit quantizer, the loop gain scaling issue can be automatically compensated by the arbitrary gain characteristics of the quantizer itself. Hence single-bit quantizer is more reasonable for the ΔΣ modulator employing passive loop stage.

The analytical model for loop function optimization of hybrid AP CT ΔΣ modulator is shown in Fig.7.4 where the scaled passive filter gain is described as k_2'.

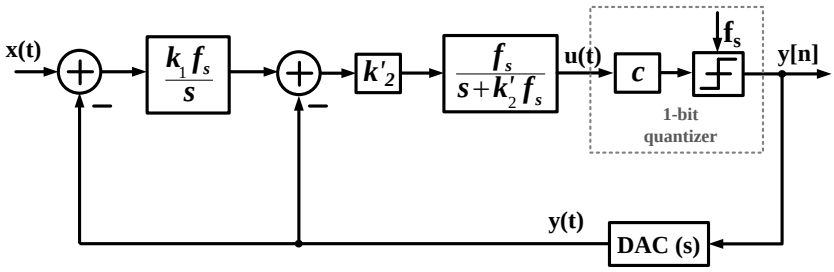

Fig.7.4 Analytical model for loop function optimization of AP CT ΔΣ modulator

Gain *c* describes the inherent gain of the single-bit quantizer, which can be arbitrary within zero to one. In practical operation, *c* can automatically satisfy the following relation to compensate loop gain.

$$\left.\begin{aligned} k_2^{'} &= a \cdot k_2 \\ k_2^{'} \cdot c &= k_2 \end{aligned}\right\} \rightarrow a \cdot c = 1 \tag{7.4}$$

Where *a* is the scaling factor of passive filter gain. The NTFs plotted in Fig.7.5represent the effect under different values of *a*.

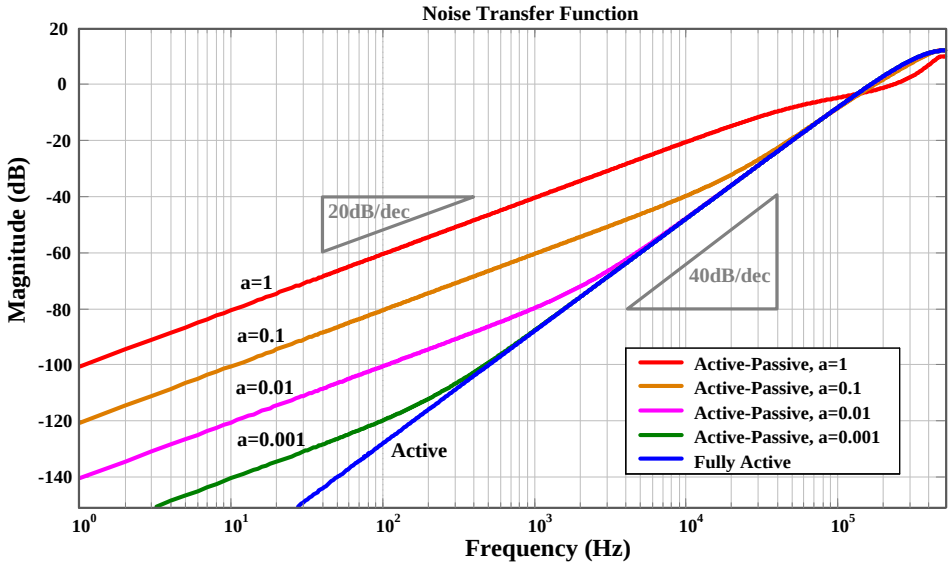

Fig.7.5 Calculated NTFs for the hybrid AP CT ΔΣ modulator with different passive loop filter gain scaling values.

It can be observed that the smaller the value of *a* is, the closer the NTF is to an ideal modulator. However, from the expression of passive RC integrator, for extremely small value of *a*, the RC time-constant should be very large which increases circuit area or thermal noise power. Moreover, if the loop-filter gain is scaled down too much, from (7.4), the equivalent quantizer gain *c* will be quite high which means the quantizer is processing a terribly small input and further increases the accuracy requirement to the comparator of the single-bit quantizer. Scaling factor *a* should be determined based on the desired signal band. The NTF's zero and pole locations variation as the deceasing of *a* are shown in Fig.7.6.

From the discussion above, to optimize a hybrid AP CT ΔΣ modulator as an approximate standard active modulator, the system is preferred to be with single-bit quantizer for its arbitrary conversion gain. Suitable scaling value for the passive filter gain can be determined based on the designed signal bandwidth.

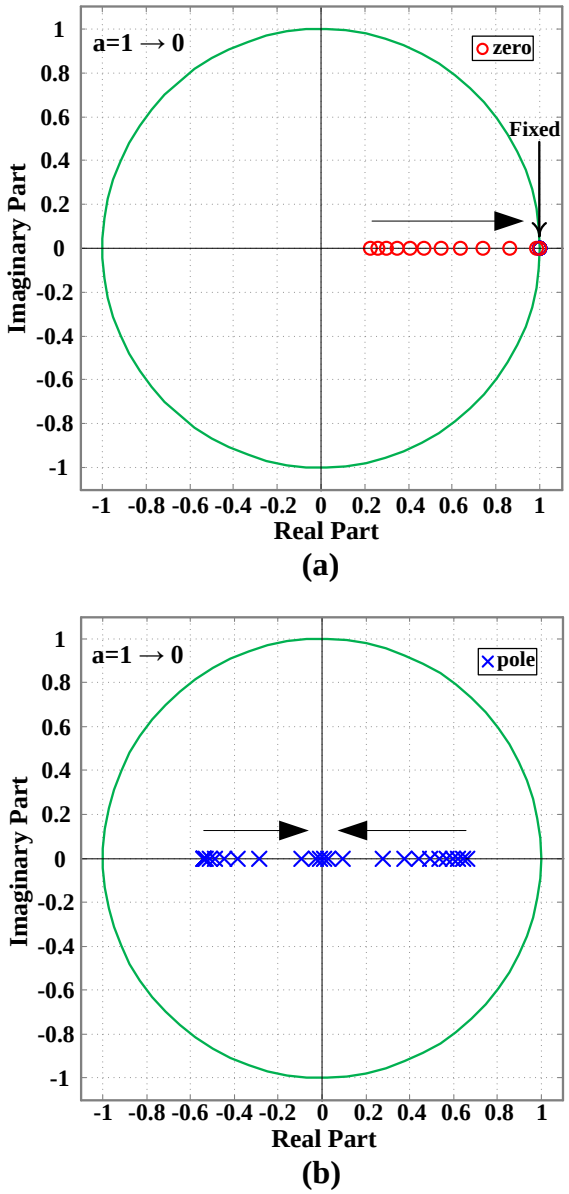

Fig.7.6 NTF pole-zero location variation for the AP CT ΔΣ modulator with the passive loop filter gain scaling from 1 to 0.

7.3 ELD COMPENSATION FOR A CT ΔΣ MODULATOR WITH HYBRID ACTIVE-PASSIVE LOOP-FILTERS

Due to the effect of ELD, the Signal to Noise and Distortion Ratio (SNDR) of the modulator may drop significantly in the CT ΔΣ modulator with hybrid AP integrators. Hence, the coming section will analyze the effect of ELD and the classical

compensation method in detail in a 2nd order CT ΔΣ modulator with hybrid AP integrators: the 1st stage of the loop filter is implemented by an active RC integrator, and a passive RC network as the 2nd stage.

7.3.1 ELD EFFECT IN THE HYBRID AP CT ΔΣ MODULATOR

Fig.7.1 and (7.2) depict the model and transfer function of a 2nd order hybrid AP CT ΔΣ modulator, and they are in the continuous-time domain. As mentioned in the previous section, all of the continuous-time transfer functions (with/without delay) should be transferred into Z-domain. Hence, a standard *LF* of hybrid AP CT ΔΣ modulator should be achieved firstly. As mentioned, NRZ rectangular feedback DAC is used in this chapter for our discussion since it is more sensitive to ELD effect. Since the Laplace Transform of an ideal rectangular feedback waveform is got as depicted in (7.3), with the modified Z-transformation method [40], *LF* in Z-domain of Fig.7.1 is:

$$\begin{aligned} LF_{ap}[z]\big|_{CT-DT} &= Z\left\{L^{-1}\left[LF(s)DAC_{NRZ}(s)\right]_{\,t=nT_S}\right\} \\ &= -\frac{k_1}{z-1}+\frac{k_2-k_1}{k_2}(e^{-k_2}-1)\frac{1}{z-e^{-k_2}} \end{aligned} \tag{7.5}$$

Compare the above (7.5) with the *LF* of the ideal 2nd order fully active modulator (which has two identical poles with values $z_1=z_2=1$), noticed that one pole of (6) has been shifted from 1 to e^{-k2}. Different k_2 will lead to different pole locations of NTF, as the previous Fig.7.6 depicted.

Meanwhile, the ELD effect will shift the NRZ feedback waveform from the current period to the subsequent period [27], as in Fig.7.7.

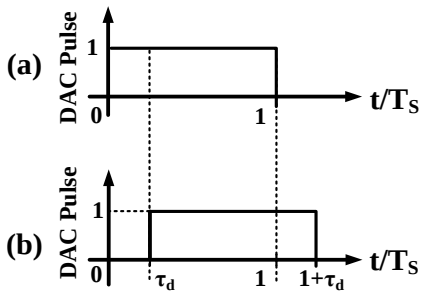

Fig.7.7 NRZ DAC feedback pulse: a) Ideal case, b) With delayed τ_d.

According to the equation of the ideal NRZ DAC feedback pulse in (4) and [29], the expression for NRZ DAC with delay τ_d ($0 \le \tau_d \le 1$) is:

$$DAC_{NRZ\_\tau_d}(s) = \frac{e^{-\tau_d sT_S} - e^{-(1+\tau_d)sT_S}}{s} \tag{7.6}$$

Based on above (7.6) and the equation (7.3) which states the methodology to achieve the *LF* in Z-domain, the *LF* due to the ELD effect can be got as below and the new *LF* is obviously dominated by the shifted delayed DAC pulse.

$$\begin{aligned} LF[z]_{ap\_\tau_d}\big|_{CT-DT} &= Z\left\{L^{-1}\left[LF(s)DAC_{NRZ\_\tau_d}(s)\right]_{t=nT_S}\right\} \\ &= Z\left\{L^{-1}\left[-\frac{k_2 f_s\left(s+k_1 f_s\right)}{s\left(s+k_2 f_s\right)}\frac{e^{-\tau_d sT_S} - e^{-(1+\tau_d)sT_S}}{s}\right]_{t=nT_S}\right\} \end{aligned} \tag{7.7}$$

With the help of second shift theorem and [29], the *LF* with delay τ_d can be got

$$\begin{aligned} &LF[z]_{ap\_\tau_d}\big|_{CT-DT} \\ &= z^{-1}Z\left\{L^{-1}\left[-\frac{k_2 f_s\left(s+k_1 f_s\right)}{s\left(s+k_2 f_s\right)}\frac{1}{s}\right]_{t=(n+1-\tau_d)T_S}\right\} \\ &-z^{-2}Z\left\{L^{-1}\left[-\frac{k_2 f_s\left(s+k_1 f_s\right)}{s\left(s+k_2 f_s\right)}\frac{1}{s}\right]_{t=(n+1-\tau_d)T_S}\right\} \end{aligned} \tag{7.8}$$

From the above (7.8) we have that the ELD increases the order of *LF* and amount τ_d affects the expressions of *LF*, this matches with the statements of ELD effect in [15][27][28][29][40].

For instance, discuss the delay effect with amount $\tau_d=1T_S$. According to the above (7.8), the *LF* when $\tau_d=1T_S$ is

$$\begin{aligned} &LF[z]_{ap\_\tau_d=1T_S} \\ &= \frac{-k_1}{z-1} + \frac{1}{z}(k_1 - 1 + \frac{k_1}{k_2} - \frac{k_1}{k_2}e^{k_2} + e^{k_2}) \\ &+ \frac{1}{z-e^{-k_2}}(-\frac{k_1}{k_2} + 1 + \frac{k_1}{k_2}e^{k_2} - e^{k_2}) \end{aligned} \tag{7.9}$$

The following Fig.7.8 describes the comparisons of NTF for a hybrid AP modulator example with a=0.25 as in (7.4) has and does not have one clock cycle ELD effect. When there is no ELD effect, the noise shaping is quite smooth; however, whenever there is one clock cycle delay in the modulator, the peak is created which describes the unstable of the system. The figure also suggests the importance of ELD compensation and the trends to compensate the ELD effect: set the suitable zero of NTF to compensate the peak in NTF.

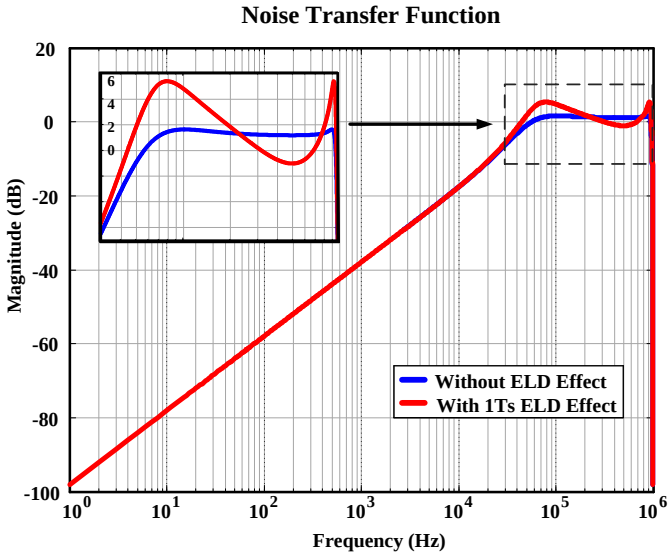

Fig.7.8 The NTF when the hybrid AP modulator contains and does not contains one clock cycle delay effect with a=0.25.

7.3.2 TRADITIONAL ELD COMPENSATION METHOD

Because of the significant effect of ELD in CT ΔΣ modulators, there are many methods proposed [26] [27] [40] [41] to compensate it. The traditional technique with one additional feedback path to compensate the ELD effect can also be used in the hybrid AP case, as represented in Fig.7.9.

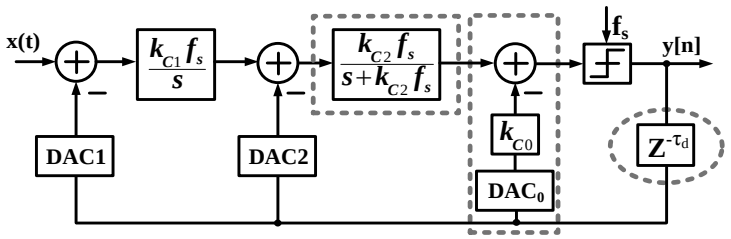

Fig.7.9 Traditional ELD compensation method for a 2nd order CT ΔΣ modulator with hybrid AP integrators.

It consists of a delay τ_d, and in practical, it is usually set to be half or one sampling period. This delay is always implemented by a D Flip-Flop and before the feedback DAC. DFF can lock the delay of the signal within a certain time; therefore, it can tolerate smaller delay lengths.

According to the classical compensated structure in Fig.7.9, the corresponding *LF* with delay can be got using (7.7). And for our discussion simplicity, one clock cycle delay is set as the example. With one clock cycle delay and based on (7.6), the Laplace Transform of the rectangular NRZ feedback can be achieved. Hence, combine the equations which states the *LF* with one clock cycle delay effect and delayed DAC together, the *LF* with $\tau_d=1T_S$ of Fig.7.9 is

$$\begin{aligned} LF[z]\Big|_{ClassicalComp\_\tau_d=1T_S} &= -\frac{k_{C1}(z-1)}{(z-1)^2} \\ &+\frac{1}{z}\left(k_{C1}-k_{C0}+1-\frac{k_{C1}}{k_{C2}}+\frac{k_{C1}}{k_{C2}}e^{-k_{C2}}-e^{-k_{C2}}\right) \\ &+\frac{1}{z-e^{-k_{C2}}}\left(\frac{k_{C1}}{k_{C2}}-1-\frac{k_{C1}}{k_{C2}}e^{-k_{C2}}+e^{-k_{C2}}\right) \end{aligned} \tag{7.10}$$

In order to compensate the effect of ELD, (7.10) should equal to (6). Then the coefficients of Fig.7.9 with $\tau_d=1T_S$ match with Fig.7.1 are:

$$\begin{aligned} k_{C0} &= k_1 + \frac{k_2 - k_1}{k_2}(1 - e^{-k_2}) \\ k_{C1} &= k_1 \\ k_{C2} &= k_2 \end{aligned} \tag{7.11}$$

As shown in Fig.7.10 that one clock cycle delay will bring the peak of NTF leads to the unstable of the modulator, in order to verify the efficiency of the compensation coefficients in (7.11), the comparison of NTF are depicted in Fig.7.12. And the same as the case in Fig.7.10, the value of *a* is also 0.25.

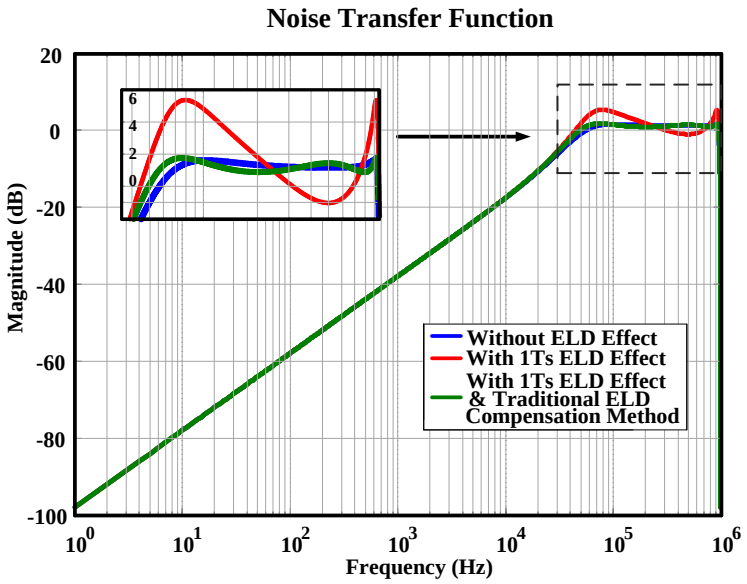

Fig.7.10 The ideal NTF (without ELD effect), the NTF for the modulator contains one clock cycle delay effect and the NTF with delay after traditional compensation with *a*=0.25.

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7.3.3 SIMPLE RESISTOR ADDER METHOD

Usually, an analog adder can accomplish such a function. In order to reduce power dissipation the analog adder can be implemented with passive elements in a general active CT ΔΣ modulator similar with the technique in [43]. As shown in Fig.7.11, the feedback current flows through the adder resistor and produces a voltage

drop; the final output is equal to the integrator output added to the voltage drop on the resistor. The feedback current will not affect the original integrator output due to the op-amp's low output impedance.

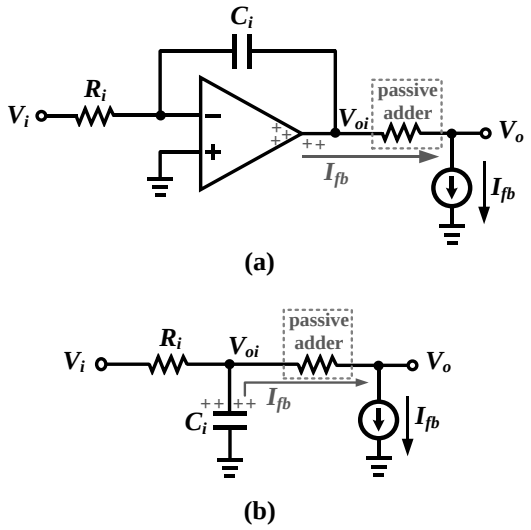

Fig.7.11 Passive analog adder current feedback in (a) active and (b) passive loop-filters.

By contrast, if the same method as in [43] is applied to a passive RC filter, as shown in Fig.7.11 (b), the only source of charges is the energy storage element, i.e. the integrating capacitor C_i. The charges forming the feedback current come from capacitor C_i (equivalent to the integration of the feedback current), and, consequently, the final output includes the integration of the sum of the input and the feedback simultaneously, and the constant k_{C0} feedback cannot be realized. Then, the passive simple resistor adder compensation method as illustrated in Fig.7.11 (a) cannot be implemented when the passive loop-filter is in the last stage. On the other hand, if an active adder is employed to implement the compensation, the low power benefit of the hybrid AP loops filtering will be lost. Therefore, low power compensation and highly efficient techniques for ELD compensation are required for the hybrid AP CT ΔΣ modulator.

7.3.4 PASSIVE ELD COMPENSATION TECHNIQUE FOR HYBRID ACTIVE-PASSIVE INTEGRATORS

Comparing the model of the traditional ELD compensation method in Fig.7.14 with the ideal active-passive model in Fig.7.1, the additional path with constant k_{C0} (as depicted in Fig.7.9) is introduced to compensate the delay. Thus, the effect of the ELD can be equivalently compensated by additional feedback with a constant in front of the quantizer and in the eyes of the *LF*. In order to reduce the additional constant path (Fig.7.9) and save power consumption, combining the constant term with the preceding passive integrator similar with the technique in [27] will be implemented, as shown in the following Fig.7.12.

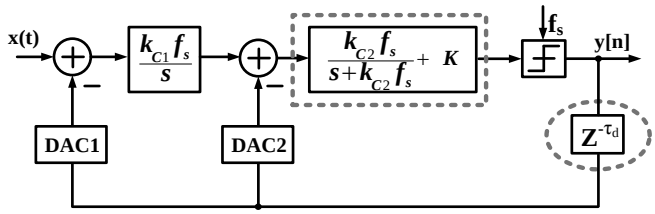

Fig.7.12 The model of the passive technique to compensate the ELD effect in the hybrid AP modulator.

According to Fig.7.12, and with the passive integrator of Fig.3.11 and Fig.3.12, the ELD effect in the hybrid AP CT ΔΣ modulator can be compensated if the constant *K* (Fig.7.12) is obtained by a ratio of resistors or capacitors, leading to the implementation of the technique. This is based on the structure of a passive RC integrator and similar with that from [27] and [33].

To compensate the ELD effect the *LF* of the passive compensation structure should match with that of the ideal hybrid AP CT ΔΣ modulator, as expressed by (5). The passive technique imposes the additional resistor R_0 in series with C_2, as shown in Fig.7.13. For this structure, after simplification, the constant *K* (Fig.7.12) can be determined by the ratio of resistors. The whole 2nd loop-stage (highlighted as the gray dashed block in Fig.7.12) can be implemented by the structure in Fig.7.13, with the transfer function given by,

$$\frac{V_{out}}{V_{in}} = \frac{sR_0C_2 + 1}{sC_2(R_0 + R_2) + 1} = \frac{k_{P2}s + k_{P0}k_{P2}f_s}{s(k_{P0} + k_{P2}) + k_{P0}k_{P2}f_s} \tag{7.12}$$

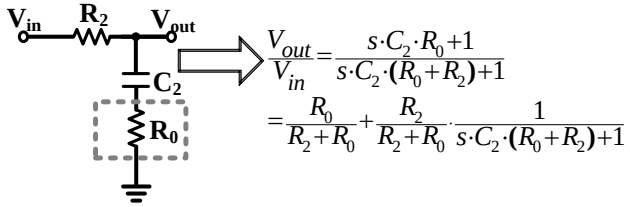

Fig.7.13 Circuit implementation of the passive ELD compensation technique for a passive RC integrator

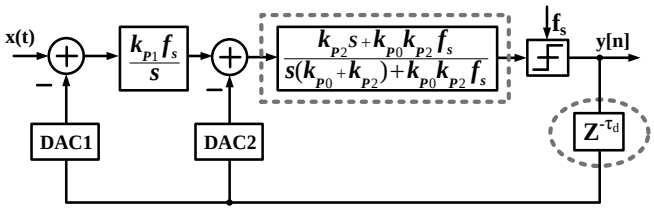

Fig.7.14 Passive ELD compensation technique with hybrid AP integrators.

Fig.7.14 represents the structure of the proposed technique for a 2nd order CT ΔΣ modulator with hybrid AP integrators and excess loop delay τ_d. (as before, τ_d is set to be 1 clock cycle). The corresponding *LF* should be equal to that of Fig.7.1, to compensate the ELD effect. Since the *LF* with ELD effect of Fig.7.9 is also identical to that of Fig.7.1, the equivalence of the *LF* between Fig.7.9 and Fig.7.14 implies that the compensation is achievable. After some calculation, the new coefficients that turn equivalent the structures of Fig.7.14 and Fig.7.9 are,

$$\begin{aligned} k_{P0} &= \frac{k_{C2}}{k_{C0}} \\ k_{P2} &= \frac{k_{C2}}{1 - k_{C0}} \\ k_{P1} &= k_{C1} \end{aligned} \tag{7.13}$$

And for the figure about NTF as demonstrated in Fig.7.10, since this

methodology is identical to that of the traditional compensation technique, the same condition will lead to the same curve as illustrated in Fig.7.10 (green line).

When comparing both structures (from Fig.7.9 and Fig.7.14), the modified passive RC integrator (Fig.7.13) operates as an adder plus an additional feedback path, simplifying the whole circuit structure and reducing power dissipation. Furthermore, the extra elements in Fig.7.9 can be implemented by only one additional resistor. Plus, when compared with the method from [27], [33] and [41], this passive technique can compensate the delay up to 1 clock cycle.

Although the compensation method presented in [41] (as illustrated in its Fig.7.6) also did not contain an additional feedback path in front of the quantizer (traditional compensation technique), that additional path was efficiently added together with the input of the last stage integrator which was implemented by an G_m-C integrator so that summation could be accomplished more easily (as depicted in Fig.7.7 of [41]). In addition, also from [41], the feedback shapes of DAC1 and DAC2 are different: DAC1 was Non-Return-to-Zero (NRZ) feedback but DAC2 was Return-to-Zero (RZ) feedback. In contrast, the last integrator here is the passive RC integrator which consumes no power and the feedback shapes of DAC1 and DAC2 are the same, which are NRZ.

7.4 DESIGN EXAMPLE OF HYBRID AP CT ΔΣ MODULATOR

In order to verify the passive ELD compensation technique, shown in Fig.7.13, a 2^{nd} order, single-bit, low-pass CT ΔΣ modulator with hybrid AP integrators was designed based on the system diagram of Fig.7.14, with a sampling rate of 250MS/s. The input bandwidth is 2MHz corresponding to the standard of 3G WCDMA receivers and the OSR is 64. The input amplitude of the signal is P_{in}= -2dBFS and NRZ feedback was chosen. The transformed CT coefficients were scaled down to guarantee that the signal swing will not reach the saturation level of the loop filter.

However, since the second integrator is passive, which will reduce the signal swing, the input swing of the second integrator should not be too small (small input swing will increase the requirement of the quantizer). The overall circuit schematic of the modulator is given in Fig.7.15, which was implemented in 65nm CMOS with 1V supply voltage. The circuit of Fig.7.13 was employed in the second loop filter to obtain the compensation.

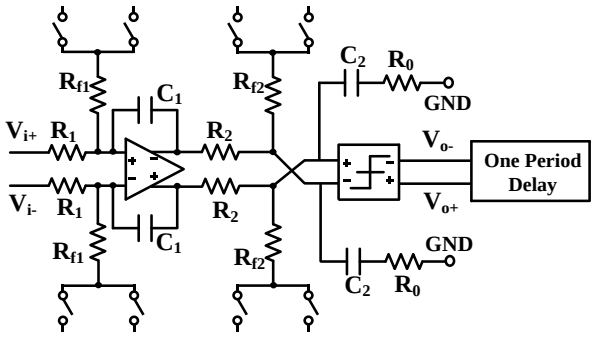

Fig.7.15 Circuit schematic of the passive ELD compensation structure in a 2nd order, 1-bit, CT ΔΣ modulator with hybrid AP integrators and NRZ DAC.

Based on Fig.7.1 and previous analysis, the performance (SNDR) of a hybrid AP CT ΔΣ modulator can approximate that of an active structure whenever the coefficient of the passive integrator is properly selected. If the structure of Fig.7.1 is taken as an example, in order to get the expected performance, a suitable value of k_2 is required.

In this design and to match with Fig.7.1, taking the swing reduction of the second passive integrator into account, for a hybrid AP 2nd order CT ΔΣ modulator without delay, $k_1 = 0.25$ is selected. Since the coefficient of the 2nd integrator affects the performance of the system it should be carefully chosen, leading here to $k_2 = 0.01$. Then, after calculation, the system coefficients with ELD compensation (as in Fig.7.14) can be obtained. Additionally, based on (7.12) and the working principle of the active and passive RC integrator, the values of all circuit elements in Fig.7.15 can be determined: $R_1 = R_{f1} = 16k\Omega$, $C_1 = 1pF$, $R_2 = R_{f2} = 400k\Omega$, $C_2 = 1pF$ and $R_0 = 2k\Omega$. Comparing this passive ELD compensation method with the traditional compensation

technique which needs active circuit elements, clearly this will reduce the power consumption of the overall system.

Fig.7.16 shows the simulation results (when 1 clock cycle delay is added) of the same modulator in two different cases, with and without the passive ELD compensation. The red curve is with input amplitude Pin=-20dBFS and blue one is Pin=-2dBFS. Since without compensation, the input amplitude Pin=-2dBFS leads to un-stability as well, here it is shown the low input amplitude to allow a comparison. The results demonstrate that the in-band noise floor of the red curve (without ELD compensation) is much higher than that of the system employing the passive ELD compensated technique (blue curve); and also the noise shaping function has been distorted due to the change of the NTF. Obviously, the system is unstable and cannot work normally under $1T_S$ loop delay without ELD compensation, in particular also because of the NRZ feedback. The dynamic range of the system is 77dB, and Fig.7.17 depicts the SNDR versus the input signal amplitude. The variation of R0 versus SNDR is also depicted in Fig.7.18, showing that the technique is not sensitive to process variations. The efficiency and delay tolerance of the passive technique is plotted and compared with the structure without compensation, as described in Fig.7.19. By contrast, after applying the proposed technique, if there is 1/2 clock period delay, the SNDR is 67.3dB; on the other hand, with 1 clock period ELD effect compensated the SNDR is 65.3dB; both of them close to the ideal 69dB case. Theoretically, the passive scheme can compensate the loop delay if not larger than 1 clock period. The comparison of the performance of the different structures analyzed is shown in Table7. 1. And in addition, the traditional simple adder technique as in [43] cannot be implemented in our hybrid AP case.

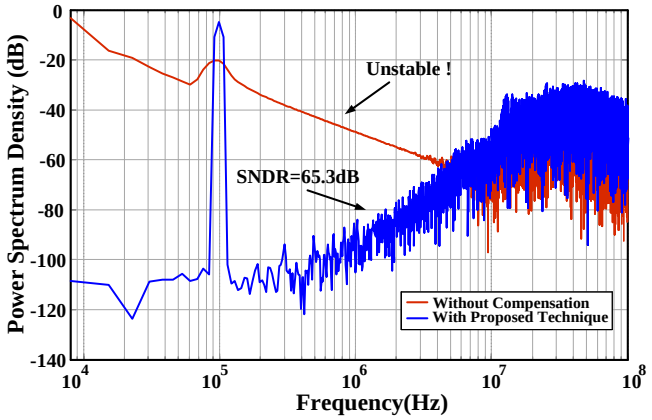

Fig.7.16 Comparison of simulation results for 2 different cases (Pin_red=-20dBFS, Pin_blue=-2dBFS) when there is 1Ts delay in the quantizer.

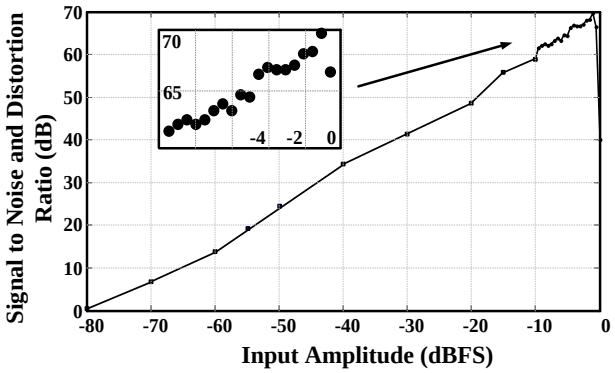

Fig.7.17 SNDR versus input signal amplitude.

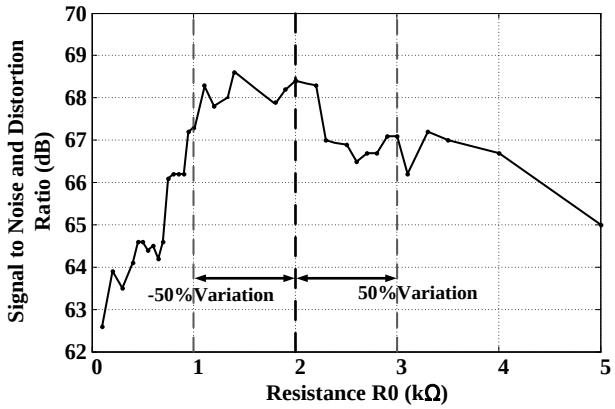

Fig.7.18 The value of R0 vesus SNDR of the system.

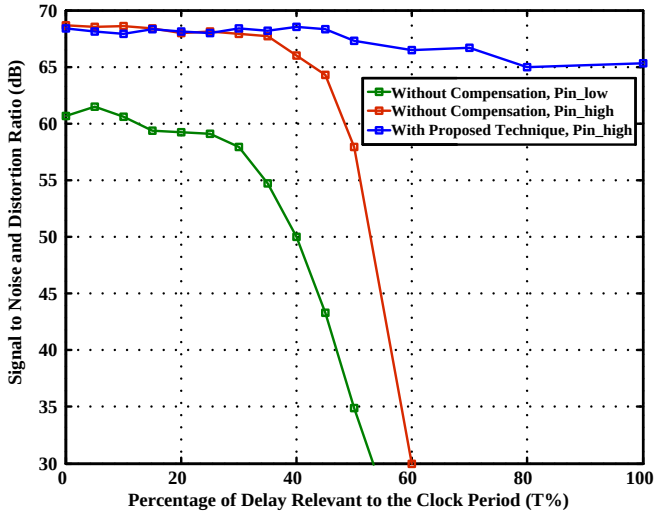

Fig.7.19 Simulation results for system sensitivity to ELD in a 2nd order Hybrid AP CT ΔΣ modulator with and w/o the proposed compensation technique, with Pin_low= -20dBFS and Pin_high= -2dBFS.

Table7. 1 COMPARISON OF PERFORMANCE OF DIFFERENT STRUCTURES

CT ΔΣ modulator	***OSR***	***SNDR (dB)***	***Power (mW)***	***Delay (%T_S)***	***Additional Components***
A	256	69.6	6	/	/
B	64	70	5.3	/	/
	64	30	5.3	50	/
	64	unstable	/	100	/
C	64	69.4	6.1	50	Adders &
	64	67.1	6.1	100	Feedback Path
D	64	68.7	2.5	/	/
	64	57.9	2.5	50	/
	64	unstable	/	100	/
E	64	67.3	2.54	50	Resistors
	64	65.3	2.54	100	Resistors

- A: 1st Order CT ΔΣ modulator with active RC integrator
- B: 2nd Order CT ΔΣ modulator where both stages are active RC integrators
- C: 2nd Order CT ΔΣ modulator where both stages are active RC

integrators and with traditional ELD compensation

- D: Hybrid AP with 1st stage as an active RC integrator and 2nd stage as a passive RC integrator

- E: Hybrid AP with 1st stage as an active RC integrator and 2nd stage as a passive RC integrator with the **passive ELD compensation technique**

7.5 SUMMARY

This chapter discussed the ELD effect in hybrid AP CT ΔΣ modulators and the feasibility of implementing different compensation techniques which commonly used full-active integrators. The passive ELD effect compensation technique and its corresponding circuit scheme, to be used in hybrid AP CT ΔΣ modulators, was verified as exhibiting very high efficiency and low power consumption. Its application allows the tolerance of up to 1 clock period of loop delay. This passive method is simpler in terms of circuit implementation and does not consume active power. Its behavior was verified both mathematically and through the design of a 2nd order CT ΔΣ modulator with hybrid AP integrators and NRZ feedback. Simulation results show that with 1/2 of clock period delay the performance of the hybrid AP CT ΔΣ modulator without ELD compensation was poor (57.9dB); by contrast, the proposed modulator achieved 67.3dB SNDR; when there is 1 clock period delay, the structure without compensation is unstable; after using the compensation method, the SNDR is 65.3dB, which is close to the ideal active case, further demonstrating the effectiveness of this passive scheme.

CHAPTER 8

CONCLUSION

8.1 SUMMARY OF THE THESIS

In this thesis, ΣΔ modulator is introduced and it is also been broadly used in the telecommunication system since the property that it can provide wide bandwidth but small silicon area and low power dissipation. Furthermore, the CT ΣΔ modulator has the benefit of anti-aliasing function compare with DT ΣΔ modulator. These are the motivations of the research background. However, compare with DT ΣΔ modulator, CT ΣΔ modulator has its own non-idealities which may reduce the performance of the modulator sharply. Hence, the compensations for these non-idealities are essential. This thesis focus on the non-ideality named Excess-Loop-Delay (ELD); therefore, the compensation methods for this non-ideality are introduced. And based on the knowledge of the effect of ELD, the thesis covers the proposed three novel different compensation techniques for CT ΣΔ modulator.

As the summary of this thesis, Chapter 1 covers the research background and motivation. The telecommunication development is been taken a glanced at, and then the suitable modulator structure for the telecommunication system for nowadays' speed and resolution is indicated.

And then Chapter 2 discusses the working principle and the properties of ΣΔ modulator. And the topologies of single-bit and multi-bit modulator are introduced and the properties of these two topologies are compared, as well as the structures of single-stage and multi-stage modulators.

Compare with the DT ΣΔ modulator, the following Chapter 3 introduces the merits of CT ΣΔ modulator. And then the transformation methods (such as the

Impulse-Invariant Transform, modified Z-Transform) between the DT ΣΔ modulator and CT ΣΔ modulator are introduced. And the alternatives for CT filter implementations (for example the active RC integrator, Gm-C integrator) are indicated. However, there are non-idealities in CT ΣΔ modulator which may affect and reduce the performance sharply same as their effects to the performance of the DT ΣΔ modulator, such as the loop gain coefficients variation, finite gain of the integrator. Compare with the DT ΣΔ modulator, there are non-ideality (such as clock jitter) in the CT ΣΔ modulator which affects the performance of CT ΣΔ modulator but does not influence the DT ΣΔ modulator are also discussed in this chapter.

Similar with the non-ideality of clock jitter, the non-ideality ELD does not seriously affect the performance of the DT ΣΔ modulator, but it is an important non-ideality in CT ΣΔ modulator. Hence, this Chapter 4 mainly focuses on the effect of ELD and the traditional existed compensation techniques. Due to the effect of ELD, the CT ΣΔ modulator may be unstable since the pole of the NTF may be changed and pushed out of the unit circle. The ELD effect is verified in this chapter not only from the mathematical point of view, but also the simulation in MATLAB. And for different kinds of feedback waveform, the effect of ELD are different, this chapter discussed the effect of it for Non-Return-to-Zero (NRZ) feedback waveform as well as the Return-to-Zero (RZ) feedback waveform type. The effect of ELD discussed in this chapter is introduced for the active RC based integrator, and the existed compensation techniques are also depicted. Based on the existed compensation techniques and the knowledge of ELD effect discussed in this chapter, three novel proposed topologies to compensate the ELD effect are indicated in the following chapters.

Chapter 5 introduces an ELD tracking compensation technique for active RC loop filter CT ΣΔ modulator. For this proposed technique, the active RC integrator is used because of the merits of its high linearity and high resolution. The delay amount of the modulator can be tracked by the simple digital logic circuit synchronously according to the real-time circuit. At the same time the lacked/redundant feedback amount due to the real-time delay is tracked and then stored in the RC network. If there is delay due to ELD, these lacked/redundant amounts are then added back to/ subtracted from the original waveform. Hence the feedback amounts after the

compensation in each sampling period are identical to that of ideal case. The technique is verified in the second order CT ΣΔ modulator with 1-bit quantizer.

Chapter 6 expresses a passive ELD compensation technique for Gm-C loop filter based CT ΔΣ modulators. Gm-C loop filters are also one kind of commonly used loop filter since it operates in open loop condition and the circuit level of it is simple. Hence, the Gm-C loop filter has the small excess phase, high-speed potential and low power consumption. Because of the benefits of the Gm-C integrator, this chapter introduces a novel compensation methodology based on Gm-C loop filter. The novel methodology introduces a feed-forward adder by implementing a resistor in series with the integration capacitor. And this novel methodology has the function of simple realization and low power dissipation because of the usage of the PI-element technique. The delay amount in the modulator equals to half of clock circle can be compensated. The technique is also verified in the second order CT ΣΔ modulator with 1-bit quantizer.

Chapter 7 introduces an ELD compensation technique for CT ΔΣ modulators with hybrid Active-Passive (AP) loop-filters. Since low power consumption has been one dominant consideration factor in the telecommunication equipment, passive loop filter with low power dissipation receives more and more recognition. And also because of the benefits of high resolution and high linearity of active loop filter, the structure called hybrid Active-Passive (AP) loop filter becomes more and more popular. This chapter covers the design and optimization methodology for hybrid CT loop-filter. From the discussion in this chapter, by appropriately scaling the passive filter gain and cooperating with a single-bit quantizer, the hybrid AP loop filtering can achieve an approximated noise-shaping function as a fully active ΔΣ modulator with the same order. The ELD effect in the hybrid AP CT ΔΣ modulator which affects the poles and zeros locations of Noise Transfer Function (NTF) in the modulator is depicted. This chapter also discusses the feasibility of applying the classical ELD compensation techniques in the hybrid AP CT ΔΣ modulator; however, it cannot be practically applied since the passive loop-filter cannot perform proportional feedback signal summation. This chapter proposes an ELD compensation technique applied in the passive loop-stage of a hybrid CT ΔΣ modulator. The technique can be easily

implemented in the circuit level and after applying it, there is one additional zero to compensate the peak in the NTF. With the help of proposed technique, the maximum quantizer delay tolerance can be a full clock period. The proposed ELD compensation technique was applied in a 2^{nd} order CT ΔΣ modulator with an active-RC integrator as the 1^{st} stage and a passive RC filter as the 2^{nd} stage.

8.2 CONCLUSION OF THE THESIS

In the proposed compensation technique I: for Active-RC integrator, it implemented the digital elements and the RC feedback network to reduce the power consumption compare with the traditional technique which needed the additional adder and the extra feedback path. After the verification in 65nm CMOS processing technology, the power consumption of the proposed technique was 5.45mW and delay amount up to half of clock cycle can be tracked and compensated compare with the traditional compensation technique consumed 6.5mW. Hence the compensation technique is quite efficiency and low power consumption compare with the traditional technique.

The proposed technique II: for Gm-C integrator, it reduced the second feedback path coefficient which reflected the power consumption from 0.25 to 0.1692 for our verification circuit. Hence, this coefficient reduction leaded to up to 32% power reduction. Besides, the low power consumption integrator Gm-C integrator would give more power reduction. This technique is also low power dissipation and effective to compensate delay amount up to half of clock cycle.

The proposed technique III is implemented in the hybrid Active-Passive (AP) CT ΔΣ modulators. It introduced the passive resistors to compensate the delay amount up to one of clock cycle, but the power consumption was just 41.6% of the traditional technique. And in addition, the traditional simple resistor adder technique cannot be utilized in our hybrid AP modulator case. Therefore, this technique is efficiency and low power dissipation technique.

8.3 THE FUTURE WORK

From the proposed three techniques in the previous chapters, the resolutions of them mainly focus around 10 bit, and in order to match with the standard of 3G WCDMA receivers, the input bandwidth is 2MHz, the sampling rate of the designed modulator is 250MS/s and the OSR is 64. These are the standards for 3G WCDMA, and for the future work we can focus on the higher speed (for example 4G) and higher resolution (>12bit) with lower power consumption (for example with the implementation of hybrid AP loop filters). For the higher sampling frequency, the ELD effect will be more significant and the compensation technique is more essential. The hybrid AP loop filter will be the research trends for the implementation of integrator in CT ΔΣ modulator.

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