A 1-V Transient-Free and DC-Offset-Canceled PGA with a 17.1-MHz Constant Bandwidth over 52-dB Control Range in 0.35-µm CMOS

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***Abstract*-Two circuit techniques, namely *switched-current-resistor (SCR)* and *switchable DC-offset canceler (S-OC) inside OpAmp*, are proposed to realize a low-voltage, transient-free and constant-bandwidth programmable-gain amplifier (PGA) with also adaptive stage-DC-offset cancellation. Fabricated in 0.35-µm CMOS, the PGA dissipates 7.4mW from 1V. The mean and standard deviation of the bandwidth over 52-dB gain range are 17.1MHz and 8.3%, respectively, The SFDR is 56.2dB. The transient in a 52-dB-gain step settles within 0.2µs.**

I. Introduction

As the supply voltages have been continuously reduced with the technology scaling, low-voltage analog blocks will be increasingly demanded for the future full integration of analog and digital blocks in nano-CMOS. Programmable-gain amplifier (PGA) is the fundamental block for many systems such as wireless transceivers. Without any supply-voltage constraint, an excellent linearity with small transient can be achieved by applying the switched-resistor technique in an inverting amplifier [1]. However, in low-voltage operation the responses will be degraded, as explained next:

Switched-Resistor Technique – Shown in Fig. 1 is a low-voltage inverting amplifier with a two-stage OpAmp [2]. No input swing is required from the OpAmp while rail-to-rail output swing is deliverable. Two common-mode feedback circuits, input (I-CMFB) and output (O-CMFB), are employed to bias the DC-levels of the virtual ground (V_{vg+} and V_{vg-}) and output, to one-overdrive voltage (V_{OD}) and half of the supply (V_{dd}), respectively. Thus, NMOS switch is workable at the virtual ground and thereby allows gain programmability through the replacement of either the forward (R_{ff}) or feedback (R_{fb}) resistor by a switched-resistor bank. Such a gain-control method has two main drawbacks. First, independent to the V_{dd}, the bandwidth will vary gain-dependently due to the variation of the feedback factor [$\beta=R_{ff}/(R_{ff}+R_{fb})$]. Second, since changing the resistance of resistor R_{ff} is equivalent to alter the overall input impedance of the PGA, tuning is more commonly done on resistor R_{fb}. But the unmatched DC-levels of the virtual ground and output will produce an unstable DC current [$I_{fb,dc}=(V_{dd}/2 - V_{OD})/R_{fb}$] in the feedback loop, disturbing the DC operating points of the OpAmp and I/O-CMFBs, thereby resulting large and long transient in gain change.

This paper proposes two techniques to realize a low-voltage high-performance PGA for an IEEE-802.11a/b/g/-compliant receiver IF-to-baseband chip [3]. The first one is the *switched-current-resistor (SCR)* technique, which compensates the drawbacks of switched-resistor one to obtain transient-free-gain adjustment and constant bandwidth, by maintaining all the DC operating points and feedback factor unaltered with gain. Another technique is the *switchable DC-offset canceler (S-OC) inside OpAmp*. It takes advantages of negative feedback to obtain a highpass pole with low-corner frequency and high DC attenuation, which conventionally occupies lots of chip area. The gained area-efficiency, together with the use of current-mode feedback at low-impedance node, improves the speed, noise and switchability of the S-OC in performing adaptive stage-DC-offset cancellation.

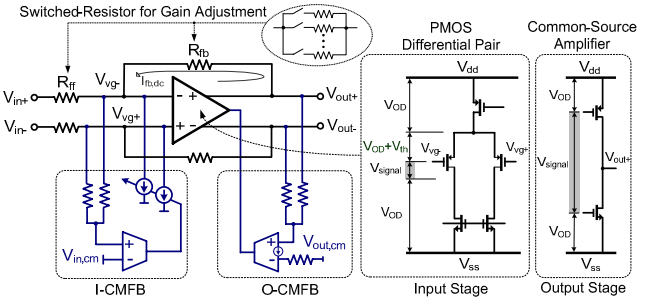


Fig. 1 Low-voltage inverting amplifier with a two-stage OpAmp.

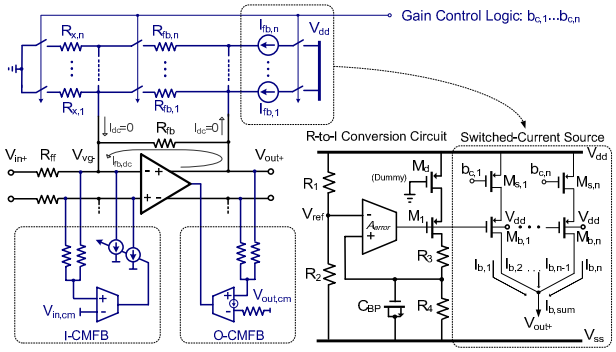


Fig. 2 The SCR technique (negative terminal is omitted for clearness).

II. Switched-Current-Resistor Technique

Illustrated in Fig. 2 is the SCR technique for maintaining the DC-operating points of the OpAmp and I/O-CMFBs unaffected by gain change. As mentioned, gain tuning by resistor R_{fb} can keep the input impedance (R_{ff}, ideally) constant, which is highly desired for cascade use of multiple PGAs. When the resistors [R_{fb}, $R_{fb,1}\cdots R_{fb,n}$] are programmed by the gain control logic [$b_{c,1}\cdots b_{c,n}$], a set of current sources [$I_{fb,1}\cdots I_{fb,n}$] and resistors [$R_{x,1}\cdots R_{x,n}$] are switched correspondingly, such that the [$I_{fb,1}\cdots I_{fb,n}$] can replace the OpAmp for delivering the transient current, while the [$R_{x,1}\cdots R_{x,n}$] can sink out the same amount of current from the virtual ground (V_{vg-}) to ground (V_{ss}). Hence, the whole operation requires no change of the $I_{fb,dc}$ and consumes no extra power. The resistors are matched by using identical unit elements in the circuit layout, whereas the current sources are derived from a linear resistor-to-current (R-to-I) conversion circuit [Fig. 2, right]. The error amplifier (A_{error}) tracks the resistance value of resistor R_4, and then mirrors it to the current sources [$I_{fb,1}\cdots I_{fb,n}$] through transistor M_1. Hence, the operation is insusceptible to thermal and process variations. The sum of the switched-current sources, $I_{b,sum}$, is given by,

$$I_{b,sum} = \sum_{i=1}^{n} I_{b,i} b_{c,i} = \frac{V_{dd}}{R_4\left(\frac{R_1}{R_2}+1\right)\frac{W_{M_1}}{L_{M_1}}} \sum_{i=1}^{n}\left(\frac{W_{M_{b,i}}}{L_{M_{b,i}}} b_{c,i}\right) \qquad (1)$$

where W_1/L_1 and $W_{Mb,i}/L_{1Mb,i}$ are the dimensions of the current-

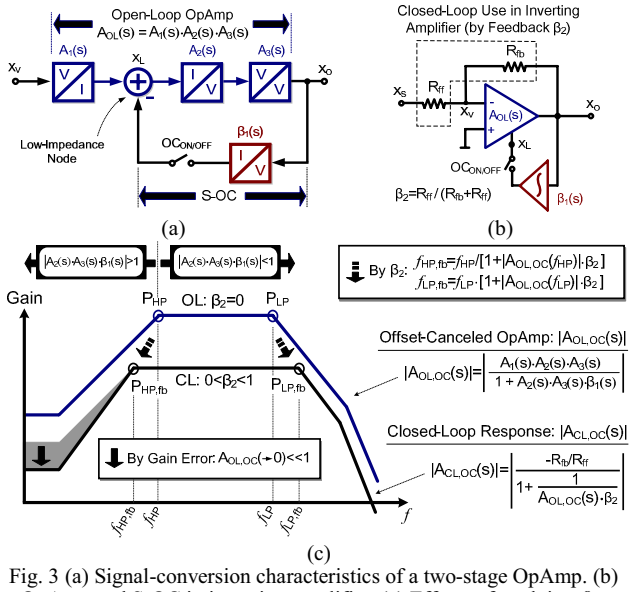


Fig. 3 (a) Signal-conversion characteristics of a two-stage OpAmp. (b) OpAmp and S-OC in inverting amplifier. (c) Effects of applying β_2.

source transistor M_1 and $[M_{b,1}\cdots M_{b,n}]$, respectively. Resistors R_1 and R_2 are used to generate a one-V_{OD} reference voltage (V_{ref}) for proper functioning the A_{error} (made by a PMOS differential pair). Since the drain voltage of all the current-source transistors $[M_{b,1}\cdots M_{b,n}]$ is $V_{dd}/2$ (i.e., the output node of the PGA), a resistor R_3 is necessary to maintain the same V_{OD} for transistor M_1. The current paths are switched by the PMOS transistors, $[M_{s,1}\cdots M_{s,n}]$ that placed directly below the V_{dd}, rather than the current sources themselves, to prevent charging/discharging the gate-capacitances of $[M_{b,1}\cdots M_{b,n}]$. MOS Capacitor C_{BP} is used to suppress the switching noise.

Another corollary of the SCR technique is on the feedback factor (β). By appropriately selecting the relationship between the resistors $[R_{x,1}\cdots R_{x,n}]$, the required closed-loop gain (i.e., $-R_{fb}/R_{ff}$), the DC-levels of the virtual ground ($V_{in,cm}$) and output ($V_{out,cm}$) matches,

$$\beta = \frac{R_{ff} \,//\, R_{x,1} \cdots // \, R_{x,n}}{R_{ff} \,//\, R_{x,1} \cdots // \, R_{x,n} + R_{fb} \,//\, R_{fb,1} \cdots // \, R_{fb,n}} = \frac{V_{in,cm}}{V_{out,cm}} \qquad (2)$$

Then, β will be constant at all gains, stabilizing the bandwidth and other advantages of feedback such as linearity improvement [4]. For instance, with 1-V supply, the $V_{in,cm}$ and $V_{out,cm}$ can be set to 0.1 V and 0.5 V, respectively. If the gain ranges from -12 dB to 12 dB with 6-dB step size, the β will be maintained at 0.2 by setting $R_{fb,n}$=4·$R_{x,n}$ for n=1,2,3.... Without the technique, β will be varied between 0.2 (at 12 dB) and 0.8 (at -12 dB).

III. Switchable DC-Offset Canceler Inside OpAmp Technique

DC-offset cancellation for baseband PGA is a costly and complex issue. Building a low-corner-frequency highpass pole can prevent baseband signal from deep damage, but impose large chip area in realization and degrade the settling time in gain change. This paper proposes a **switchable, low-noise, area-efficient** and **speed-enhanced** DC-offset cancellation method - *S-OC inside OpAmp*, which is highly appropriate for low-voltage operation since the normally used feedback node – virtual ground – will not be exploited to correct the DC imbalance. Such a feature is ultra imperative as a low-voltage OpAmp offers no input swing.

Switchability – Adaptive DC-offset cancellation helps to minimize transient in gain change (e.g., switched transconductors [5] and successive switching [6]), but requires fast-and-free switchable DC-offset cancellation circuit to implement. The

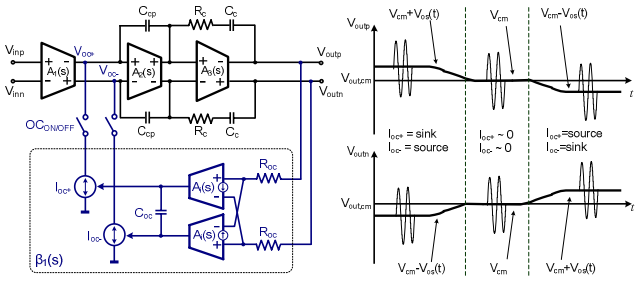


Fig. 4 (a) Block schematic of the OpAmp and S-OC and (b) its operations in canceling the dynamic DC-offset.

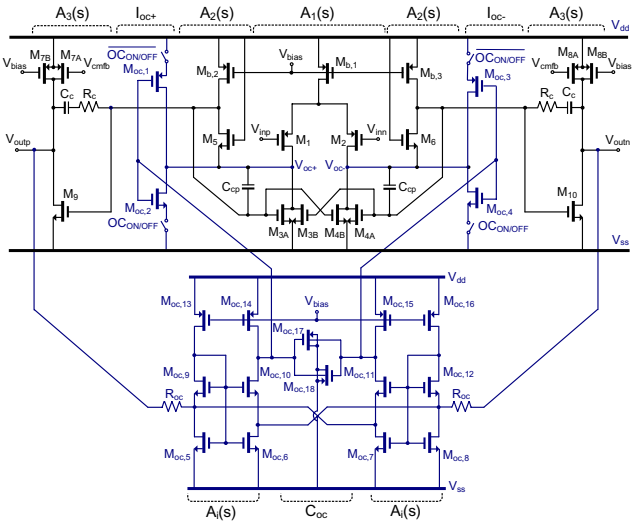
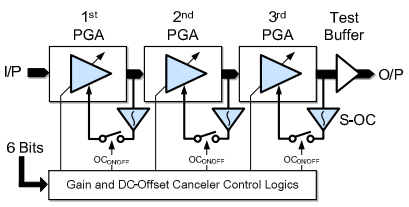


Fig. 5 Full-circuit schematic of the OpAmp and its S-OC.

proposed current-mode S-OC well fulfills such requirements. The principle is explained in Fig. 3(a), by using the inherent signal-conversion [i.e., voltage (V) or current (I)] characteristics of a two-stage OpAmp, $A_{OL}(s)$, which is divided into three stages, i.e., $A_1(s)$, $A_2(s)$ and $A_3(s)$, representing a transconductance, transimpedance and voltage amplifier, respectively. The former two stages form the first gain stage and create a low-impedance node, x_L, in their interface. It is well-known that a low-impedance node (e.g., the virtual ground) allows operational independence of multiple current-mode inputs. The proposed S-OC is originated from such a concept. Building a servo loop closes $A_2(s)$ and $A_3(s)$ by using a transconductance integrator, $\beta_1(s)$, can minimize the loading effect between the OpAmp and S-OC, such that switches ON/OFF the S-OC (with $OC_{ON/OFF}$) will not induce transient or disturbance to the original behavior of the OpAmp.

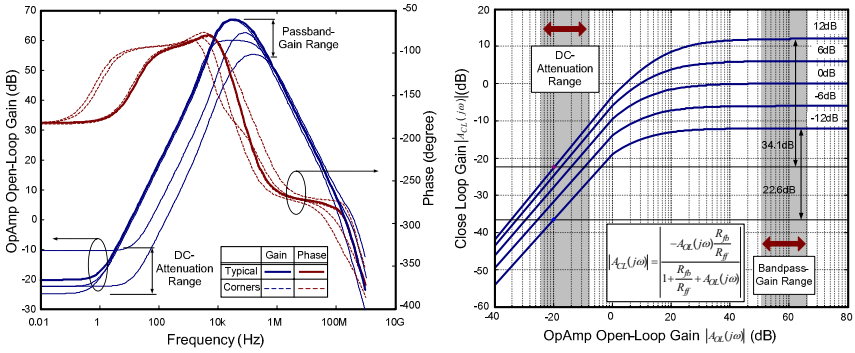
Low Noise – Using x_L as the feedback node offers better noise performance than conventional methods that normally used the virtual ground. The reasons have two. 1) x_L is inherent low impedance, while the quietness of the virtual ground is maintained by the loop gain that will decay in high frequency. 2) The input-referred noise of the S-OC will be lowered by the gain of the $A_1(s)$, especially noticeable in cascade-use of multiple PGAs.

Area Efficiency – As described by Fig. 3(b) and (c), it is one of the properties of negative feedback that closed-loop use of the DC-offset-canceled OpAmp, $A_{OL,OC}(s)$, in an inverting amplifier, $A_{CL,OC}(s)$, can shift the highpass (lowpass) pole to lower (higher) frequency, by a quantity approximately equal to the loop gain, i.e., from f_{LP} to $f_{LP,fb}$ for the lowpass pole (P_{LP}), and from f_{HP} to $f_{LH,fb}$ for



PLAN	1ST	2ND	3RD	TOTAL
MAX.	12dB	12dB	6dB	30dB
MIN.	-12dB	-12dB	2dB	-22dB
STEP	6dB	6dB	2dB	

Fig.6 Implemented PGA and gain plan.



(a) (b)

Fig. 7 (a) AC performances of the OpAmp (typical and corners). (b) Closed-loop gains of the PGA versus OpAmp DC and passband gain ranges from Fig. 7(a).

the highpass pole (P_{HP}). Another property is that a closed-loop response is a scaled version of the open-loop one once the feedback is frequency invariant. Thus, DC attenuation provided by the $A_{OL,OC}(s)$ further increases the DC-offset suppression due to closed-loop gain error (as discussed next in Section IV). The consequence is a considerable amount of chip area can be saved given that a deep highpass pole with low-corner frequency is extremely area hungry if building by passives (i.e., resistors and capacitors).

Speed Enhancement - The proposed S-OC not only cancels the static, but also the dynamic offset voltage with faster convergent speed. As described by Fig. 4(a) and (b), the output currents, I_{oc+} and I_{oc-}, are current sources/sinks exchangeable to cancel the DC-offset differentially (i.e., double speed). Of course, both I_{oc+} and I_{oc-} will be inactive when there is no DC imbalance.

Implementation - The full-circuit schematic of the OpAmp and its S-OC is shown in Fig. 5. $A_1(s)$ is a PMOS differential pair formed by M_1 and M_2 with a cross-coupled active load obtained formed by M_{3A}, M_{3B}, M_{4A} and M_{4B}, which self-biased the DC-level and stabilized the common-mode gain of $A_1(s)$ [7]. The inherent low input impedance of $A_2(s)$ is created by M_5 (M_6). The $A_3(s)$ is miller-compensated by R_c and C_c. The R_{oc} converts the output voltage into current for the micro-ampere-biased current-mode amplifier, $A_1(s)$, which drives the C_{oc} to extract the DC imbalance. The s-domain transfer function of the complete $\beta_1(s)$ is given by,

$$\frac{I_{oc+}(s) - I_{oc-}(s)}{V_{outp}(s) - V_{outn}(s)} \approx 2\frac{A_{i,dc}/C_{oc}}{(s+1/r_oC_{oc})}\frac{gm_{oc}}{R_{oc}} \quad (3)$$

where $A_{i,dc}$ and r_o are the DC gain and output resistance of $A_1(s)$, respectively. Controlling the r_o can minimize the corner frequency without disturbing the gain, while the other parameters control both the gain and corner frequency. By biasing the $M_{oc,5}$ - $M_{oc,16}$ all with micro-ampere current, r_o becomes large enough to lower the corner frequency to less than 20 kHz. gm_{oc} is the transconductance of I_{oc+} (I_{oc-}) formed by $M_{oc,1}$ and $M_{oc,2}$ ($M_{oc,3}$ and $M_{oc,4}$). They benefits from low-voltage operation (i.e., $V_{th,n}+|V_{th,p}|>V_{dd}$) will not be able to switch-ON together to cause instability. The capacitor C_{oc} is formed by $M_{oc,17}$ and $M_{oc,18}$ in parallel-compensation way to reduce the area occupation with low-linearity penalty.

IV. Design and Simulation Results

The presented two techniques were implemented in a 3-stage PGA as shown in Fig. 6, each stage has individual S-OC for adaptive stage-DC-offset cancellation. Coarse followed by fine gain controls was utilized to minimize transient in gain change.

The simulation results of the OpAmp are presented as its net performances were not directly measured. Simulated with 1-V supply, the open-loop responses of the offset-canceled OpAmp in the typical and the four main process corners are obtained in Fig. 7(a). Its bandpass characteristic only provides sufficient gain around the passband, while highly rejects the low frequency region. Based on such simulation results, the closed-loop gain versus the OpAmp open-loop gains in stopband and passband regions are plotted in Fig. 7(b). Ideally, the DC attenuation offered by the OpAmp can improve the DC-offset and *1/f* noise suppression ranges from 22.6 dB to 34.1 dB due to closed-loop gain error. Of course, the passband is maintained in the accurate-gain region.

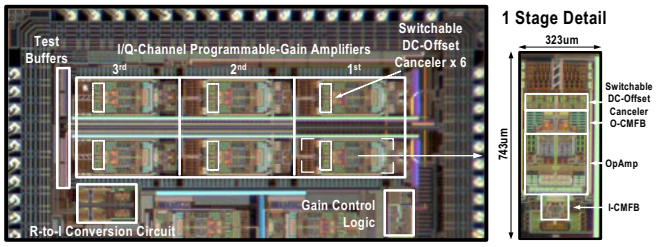


Fig. 8 Chip microphotograph of the PGA (include I and Q channels).

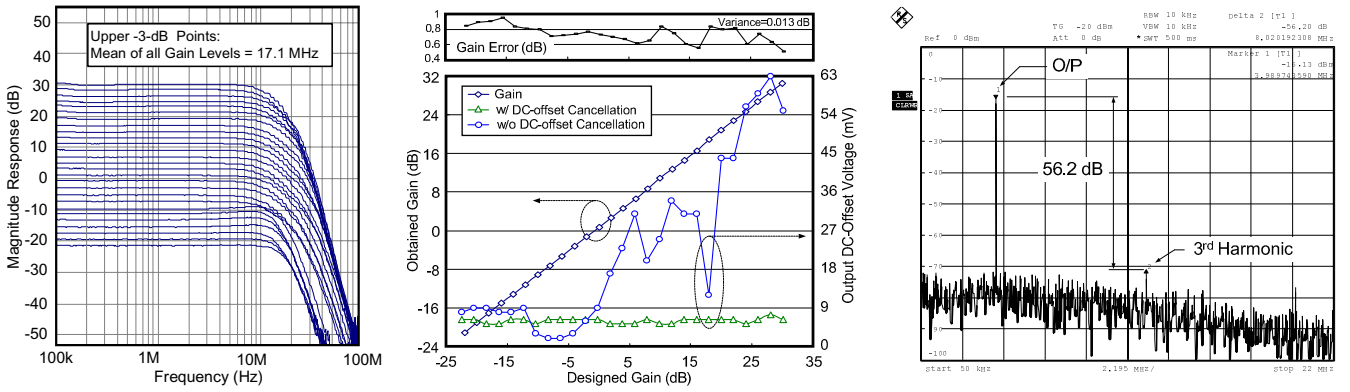
V. Experimental Results

The chip microphotograph of the PGA is shown in Fig. 8. Two paths were implemented for the I and Q channels of a receiver. The frequency responses over all gains are shown in Fig. 9(a), the mean and standard deviation of the upper -3-dB point are 17.1 MHz and 8.3 % (dominated by the gain steps ≤ -10 dB), respectively. The designed gains versus the obtained ones, gain error, output offset voltage (V_{os}) with and without cancellations is plotted together in Fig. 9(b). Linear-controlled gains were achieved with a 0.013-dB gain-error variance. The non-canceled V_{os} increases accordingly with gain but fluctuates in between due to random mismatch. The

TABLE I. Measurement Summary.

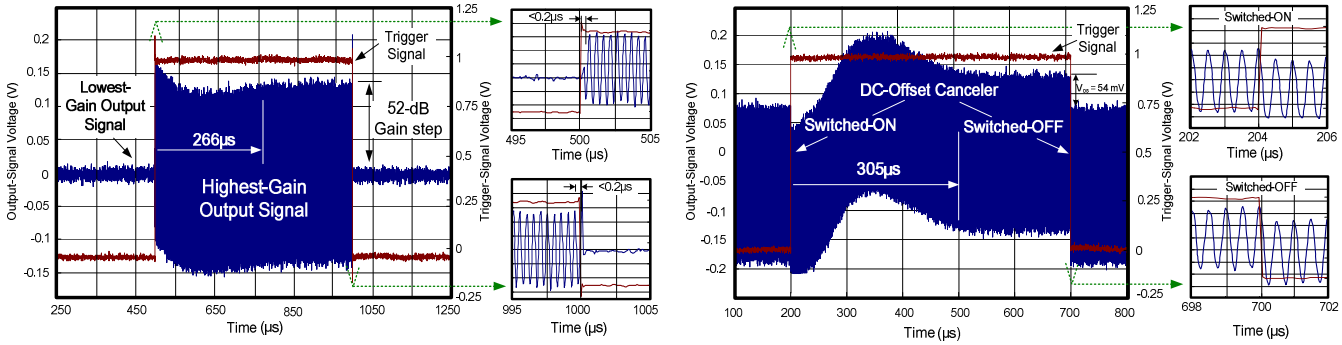
Voltage Gain Range (2 dB/Step)		-22 dB ··· +30 dB
Upper/Lower -3-dB Point	Mean of All Gains	17.1 MHz / 22.5 kHz
	Standard Deviation	8.3 % / 11.2 %
Output Noise Density	At 30-dB Gain	273.1 nV/√Hz
	At -22-dB Gain	20.5 nV/√Hz
Transient duration (tested by a 52-dB gain step)		< 0.2 µs
$IIP3_{in\text{-}band}$ (Gain Level=30 dB)		+8.4 dBm
SFDR (f_{in}=4 MHz, Gain Level=30 dB)		56.2 dB / 39.7 dB *Δ
Output Offset Voltage V_{os} †		5.7 mV / 23 mV *
Current Consumption †‡		7.4 mA
Supply Voltage		1 V
Technology ($V_{th,n}$=0.52 V, $V_{th,p}$= -0.65 V)		0.35-µm CMOS
Active Area of one channel /one S-OC		0.72 mm² / 0.02 mm²

†: Mean of all gains. ‡: Exclude the test buffers.
*: Without DC-offset cancellation. Δ: 2nd harmonic dominant.



(a) (b) (c)

Fig.9 (a) Frequency response at all gains. (b) Designed gain versus output gain, gain error, DC offset with and without DC-offset cancellation. (c) Dynamic-range measurement with 4-MHz single-tone input.



(a) (b)

Fig. 10 Dynamic performances with (a) 52-dB-gain step and (b) switched-ON/OFF the DC-offset canceler.

canceled V_{os}, which is practically non-zero, remains constant at 5.7 mV, implying small dynamic V_{os} will turn out in gain change. The spurious-free dynamic range (SFDR) is 56.2 dB [Fig. 9(c)].

The transient in gain change was measured with the largest gain step (52 dB) applied. As shown in Fig. 10(a), the output signal reaches the desired gain level in less than 0.2 µs. In between, the highpass pole causes only small DC variation and settles within 266 µs. The next Fig. 10(b) shows the dynamic behavior of the S-OC when it is switched. No noticeable transient happens at the start and stop slots, and the offset voltage was canceled within 305 µs. Other performance metrics are summarized in Table I.

VI. Conclusion

This paper presented two novel techniques to build a high-performance and low-voltage PGA for an IEEE 802.11a/b/g-compliant receiver. The SCR technique minimized the transient in gain change and bandwidth variation over gains, whereas the *S-OC inside OpAmp* technique offered switchable, low-noise, area-efficient and speed-enhanced DC-offset cancellation.

Comparing the achieved results with the state-of-the-art baseband PGAs and gain-controlled amplifiers (GCAs) [Fig. 11], this work reports the first 1-V design (at least 1.5 V down from the rest) with a medium-gain range of 52 dB without noticeably increasing the power or using leading-edge technologies.

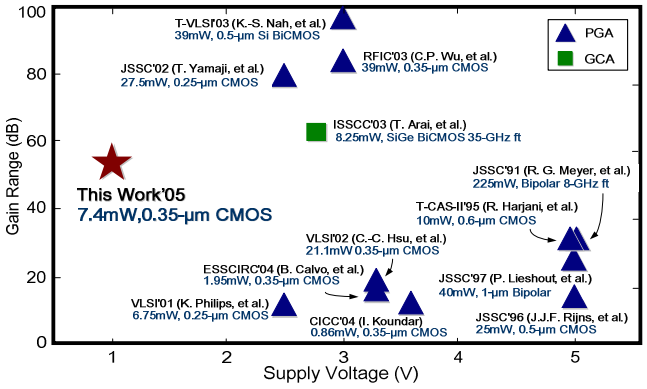


Fig. 11 Comparisons of the state-of-the-art baseband PGAs & GCAs.

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