An 11b 900 MS/s Time-Interleaved Sub-ranging Pipelined-SAR ADC

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***Abstract* - This paper presents a sub-ranging 6-way time-interleaved pipelined-SAR ADC that achieves 900MS/s and 9.3 ENOB in 65nm CMOS. The architecture optimization is based on a pipelined-SAR structure that obtains high-speed with an optimized number of channels, thus leading to relaxed calibration with higher efficiency in power and area consumption. The proposed channel-selection-embedded bootstrap performs sampling instants synchronization without additional components, thus effectively suppressing the spurs from time skews below -65 dBFS. The mismatch errors due to offset and gain are all solved on-chip, whose spurs are suppressed below -67 dBFS. The prototype achieves 66 dB SFDR and 51.5 dB SNDR with a Nyquist input exhibiting a FoM of 56 fJ/conv.step.**

I. INTRODUCTION

High-speed and high-resolution ADCs are demanded for today's applications such as broadband satellite receivers, cable TVs and software-defined radios [1]. Recently, several power efficient and sampling rate in GHz range ADCs have been reported [1]-[5]. The conversion rate is boosted by using highly time-interleaved (TI) schemes, while the most critical design challenge is the time spurs that degrade both SNDR and SFDR. The timing skews can be reduced and tolerated by design constraints [4]-[6], while the active T/H circuit [5] and the required precise clock distributions burn >10s mW power. The highly Time-Interleaved(TI) SAR ADC with timing-calibration obtains the best power efficiency for the GHz speed goal [3], which removes the power and accuracy trade-off in the clock generator. However, the calibration sensitivity is limited by the type of input signal [1] or the other non-idealities among sub-SAR ADCs such as reference noise, offset and gain mismatches [1]-[3]. The skew calibration achieves better than 63dB SFDR in a TI-SAR ADC with GHz sampling rate and 10b resolution, while the calibration power from offset, gain and timing occupies near 50% total ADC power.

This paper presents an 11b TI-sub-ranging pipelined-SAR ADC that achieves a maximum 1.1GS/s sampling rate with competitive power-efficiency as compared with the timing-calibrated TI-SAR ADCs. We propose two optimizations based on: 1) ADC's sampling front-end for better SFDR by using the proposed channel-selection-embedded bootstrap rather than timing-calibration; 2) ADC's architecture for both high-speed and high-resolution by implementing hybrid structures and multi-shared elements to relax settling and accuracy requirements. The design reduces the calibration effort (only offsets are corrected on-chip) [7] and less number of channels, thus leading to low area cost.

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II. OVERALL ADC ARCHITECTURE

The overall ADC architecture is depicted in Fig. 1, which consists of 2 main TI sub-ranging ADCs operating at 450MS/s for an aggregate 900MS/s. Each channel is built with a 2b flash ADC shared by 3×TI-ADCs architecture to achieve high-speed and better power efficiency. The sub-ADCs are implemented with a 150MS/s pipelined-SAR architecture that has a low stage-gain to relax the comparison accuracy in each bit cycle as well as the offset mismatch requirement. Since there is a total number of 6 time-interleaved channels, the sampling front-end is designed properly to suppress the performance degradation due to the timing skew errors.

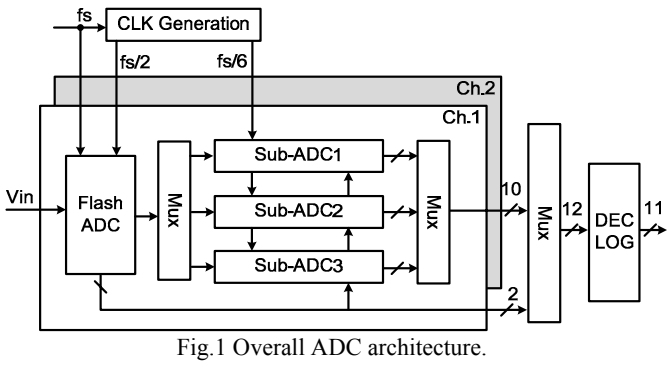

Fig.1 Overall ADC architecture.

III. PROPOSED CMCLK BOOTSTRAP CIRCUIT

The sampling network of these 6 TI-ADCs is shown in Fig.2. To maintain good power efficiency, the active T/H circuit and

power hungry clock generator for precise TI clock signals are avoided. The strategy used in this design is similar to [6] that synchronizes the sampling instances of n TI-channels with a full speed master clock. The concept in [6] is demonstrated in parallel with the proposed solution, of which the clock path is highlighted in gray in Fig.2. The master clock Φ_M is selectively applied to two time-interleaved master bootstrap circuits via a MUX or AND gate controlled by the clock signals Φ_1 and Φ_2. As this design targets for high-resolution, a channel-selection-embedded (CSE) bootstrap is proposed, which minimizes the master clock path to the bootstrap terminal by simply performing the channel selection in the bootstrap itself. The sampling network of the ADC is built with two main S/Hs associated with 6 sub-S/H channels. The input signal is sampled passively onto the capacitor C_F and the DAC according to the time-sequence. The series connection between the master and slave switches [4] avoids the time skews among the sub-channel's sampling. The penalty is the reduced bandwidth, which can be traded by using larger sized sampling switches. The achievable sampling bandwidth of this design is higher than 4GHz. The spur due to the timing skews in main S/H channels can be suppressed to a value below -65 dBFS by using the proposed CSE-bootstrap of Fig.3. The sampling instances in the main channel is defined by a common-master clock Φ_M, which is applied directly to the transistor M2. The

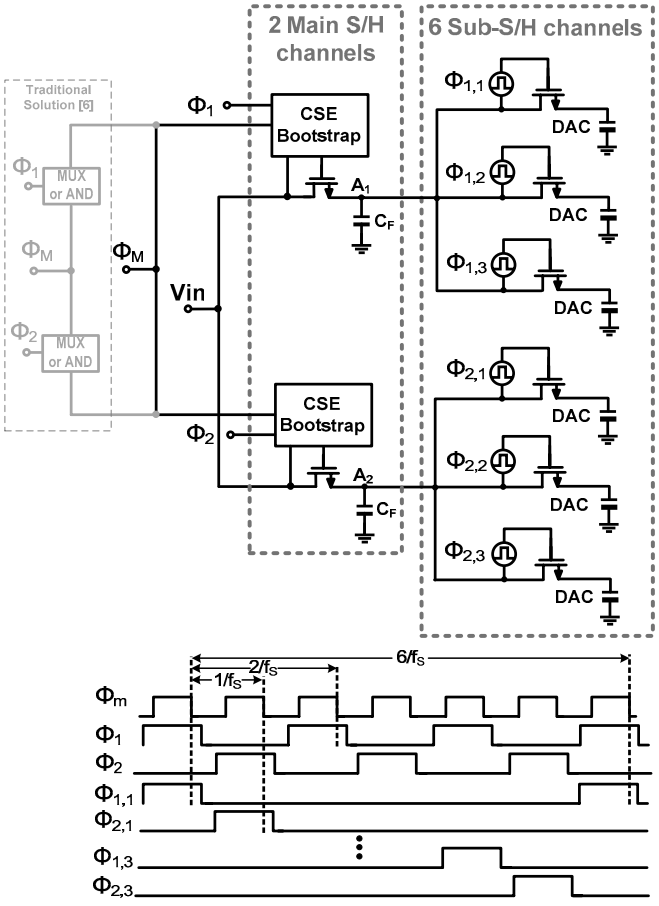

Fig. 2 Time-Interleaved sampling front-end and its timing diagram.

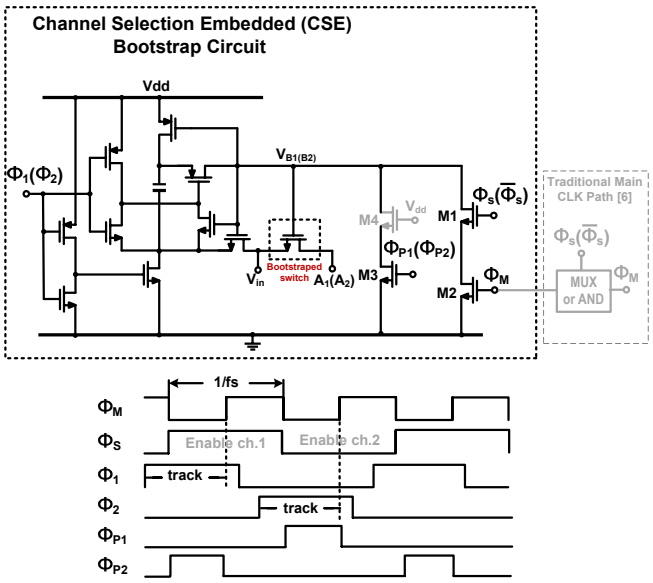

Fig. 3 Proposed Channel-Selection-Embedded bootstrap circuit and its control timing diagram.

transistor M1, of which the gate is usually connected to V_{dd}, now is used to enable the channel according to the clock signal Φ_S. The solution avoids the additional devices such as MUX or AND gate implemented in series with the master clock signal, which minimizes the clock jitter injected in the main clock path to the bootstrap terminal. The 1st(2nd) channel starts to track the input signal, when $\Phi_1(\Phi_2)$ is high. Either of the channels stops tracking, while M1 and M2 are both turned on. The sampling instance is determined by the rising edge of Φ_M that pulls down the gate voltage of the sampling switch from $V_{in}+V_{dd}$ to Gnd. The simulated spread on the falling edge of $V_{B1(B2)}$ is reduced to 320 fs by using a 6μm device for both M1 and M2. The transistor M3 is assisted to avoid the floating of $V_{B1(B2)}$, which is not necessary, if the floating duration is short. Also, the transistor M4 could be added to avoid the overstress of M3. The tracking time is ~800ps, and the starting time determined by clock signals Φ_1 and Φ_2 is not critical. The small clock buffers are used for non-critical control signals Φ_1, Φ_2, Φ_{p1}, Φ_{p2} and Φ_S to optimize the power dissipation from the clock generator. The master clock is generated via an inverter chain with a single-ended 900MHz sine wave signal input. Also, it is routed separately to the gate terminal of M2 in the main S/Hs, of which the distances are optimized and symmetrical routing is implemented to guarantee a good matching between two master clock paths.

IV. Proposed Sub-ranging Pipelined-SAR Architecture

Fig. 4 details the architecture of each main channel that is composed by 3 TI sub-ranging pipelined-SAR with a shared 2b flash and op-amp. The 1st-and the 2nd-stage determines the coarse 6 bits and the fine 6 bits, respectively, which have 1 bit overlapping for digital-error-correction to relax the sampling

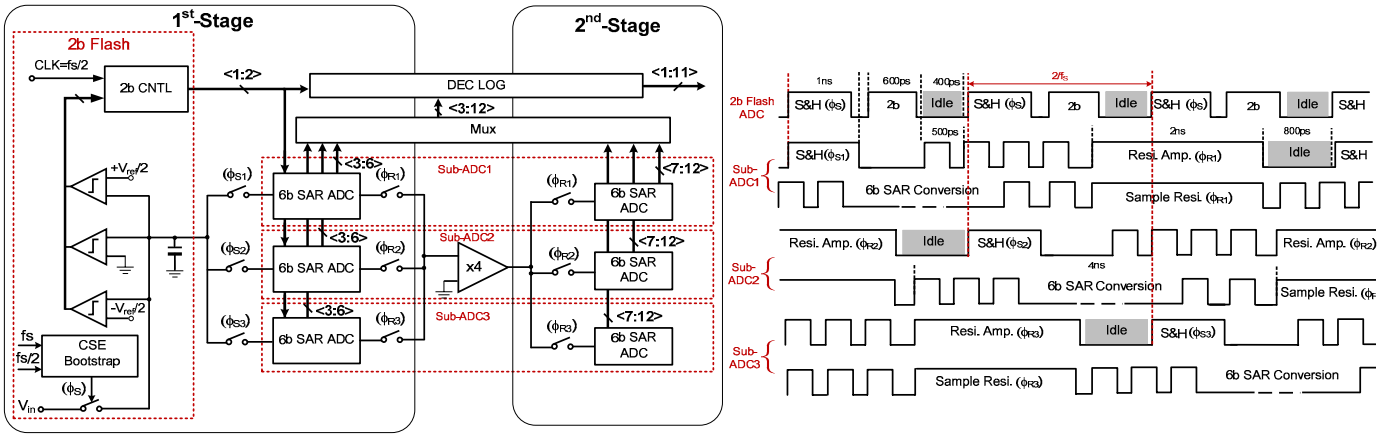

Fig.4 Main channel ADC architecture and its timing diagram.

and comparison accuracies between the flash ADC and the sub-SAR ADCs in 1st-stage to 8b. The flash ADC resolves 2 MSBs, and the controller passes the logic to the corresponding sub-SAR ADC that starts to resolve the remaining 4 bits. The residue is then amplified by 4 to the 2nd-stage 6b SAR ADC, where extra 2b are implemented to cancel the offsets in the op-amp and the comparator of the 2nd-stage. The flash takes 600ps for comparison and 2 MSBs settling. Since the LSBs are switched in the subsequent SA cycles, the self-time loop runs synchronously with a clock period of 500ps. The op-amp is shared by the sub-ADCs, and its bandwidth determines the number of TI-sub-ADCs. It takes 2ns for amplification that implies a GBW of 1.55GHz. The stage-gain error and channel gain mismatches are tolerated by intrinsic capacitor matching. Therefore, no gain calibration is used in this design. When compared with 2b/cycle conversion in the 1st-stage [7], this structure simplifies SA control logic and relaxes the loop period by more than 20%. There is enough idle time left in the flash and sub-SAR ADCs to track and compensate the offsets in the background, when suffering from temperature and supply variations, although that was not implemented here.

V. Measurement Results

The ADC occupies 0.146mm^2 (430μm×340μm) of core area and was fabricated in 1P7M 65nm CMOS (Fig. 5). Fig. 6 shows the measured FFT of the ADC with the input signal frequencies at DC and near Nyquist, where the SNDR is only limited by the noise instead of the mismatches in the sub-channels. With a DC input the noise is mainly originated from the reference voltages due to the switching transients in sub-DACs. Since the amplification phase in sub-ADCs is overlapped by the conversion phase in other channels, the reference variations degrade the amplification accuracy. The spurs due to the gain mismatch between the sub-channels are below -67 dBFS, thus the gain calibration is not necessary. When the input signal goes up to Nyquist, the noise from clock generator limits SNR to 51.7dB, with only a slight drop in SFDR and THD. This SNR degradation is mainly limited by the jitter from the clock generator corresponding rms value of 650 fs. The jitter is larger than the design expectation, which can be significantly improved by using a differential clock generator instead of a single-ended. On the other hand, the SFDR due to time skew is 66 dB, which verifies the effectiveness of the proposed CSE-bootstrap. According to the measured dynamic performance of the ADC in Fig.7, the SFDR is above 60 dB up to a 530 MHz input frequency, and the SNR limits the ADC performance. The maximum sampling frequency can go up to 1.1GS/s, when the digital supply increases to 1.3V. The DNL/INL after offset calibration is 0.66/1.5LSB, as shown in Fig.8. The power consumption is 15.5mW at a 1.2V supply, including 5.5mW analog power and 10mW digital power. The ADC achieves a FoM of 28 fJ @DC and 56 fJ @Nyquist input. The performance summary and comparison with the most advanced and recent high-speed and high-resolution ADCs are listed in Table I, which confirms that this design achieves a better SFDR without the timing correction. Also, as the design requires less calibration efforts, it leads to a much smaller area and the best FoM.

VI. Conclusions

This paper presents a speed and resolution optimized 6-way TI pipelined-SAR architecture, which achieves high-speed and high-resolution with excellent power efficiency. The speed, power and number of TI channels are optimized by implementing a flash + 3 TI-pipelined-SAR structure. Also, the proposed CSE-bootstrap achieves the time-skew spurs lower than -65 dBFS. The design limitations in TI-ADCs including offset, gain and timing are all solved on-chip, and the spurs due to the mismatch errors are well below the design limitation. This structure exhibits lower calibration complexity and achieves higher efficiency in terms of power and area consumption, when benchmarked with the state-of-the-art.

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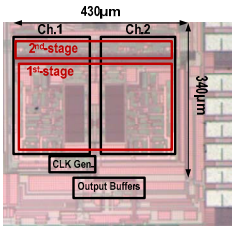

Fig. 5 Die chip photograph.

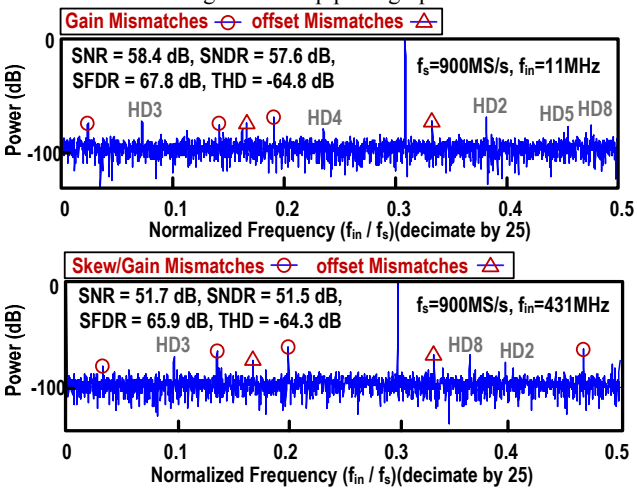

Fig. 6 Measured FFT fin @DC and Nyq. with fs @900MS/s.

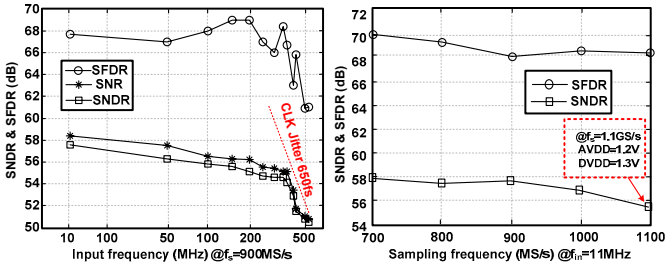

Fig. 7 Measured dynamic performance.

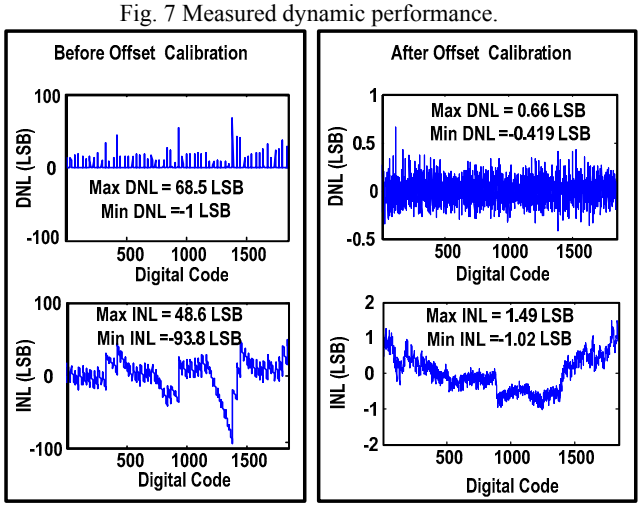

Fig. 8 Measured Static performance.

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TABLE I : Performance Summary and Comparison with State-of-the-Art

	[1] ISSCC' 14	[2] ISSCC' 14	[3] JSSCC' 13	[8] VLSI' 13	This Work	
Architecture	TI-SAR	TI-SAR	TI-SAR	Pipeline	TI-Pipelined-SAR	
Technology (nm)	40	65	65	65	65	
Resolution (bit)	10	10	10	10	11	11
Sampling Rate (MS/s)	1.62	1	2.8	0.8	0.9	1.1
Supply Voltage (V)	1.1	1	1	1.2	1.2/1.2	1.2/1.3
Input Swing (V_{p-p})	1	N/A	N/A	1.8	1.2	1.2
SNDR @DC (dB)	51	53.5	53.5	51	57.6	56.2
SNDR @Nyq. (dB)	48	51.2	51.2	48	51.5	50.7
SFDR @Nyq. (dB)	62	60	55	N/A	65.9	64
DNL/INL (LSB)	N/A	0.1/0.1	N/A	0.7/1.8	0.66/1.5	0.69/1.6
Area (mm^2)	0.83	0.78	1.7	0.18	0.15	
Power (mW)	71	19.8	44.6	19	15.5	18
FoM @DC (fJ/conv.step)	150	51	56	53	28	32
FoM @Nyq. (fJ/conv.step)	210	62	78	71	56	58
Require Timing Correction	Yes	Yes	Yes	No	No	
Calibration (on-chip)	Offset, gain, time	Offset	Offset, time	No	Offset	