Time Interleaved Current Steering DAC for Ultra-High Conversion Rate

Da Feng, Sai-Weng Sin
State-Key Lab. of Analog and Mixed-Signal VLSI
University of Macau
Macao, CHINA
E-mails: fengda@gmail.com, terryssw@umac.mo

Edoardo Bonizzoni, Franco Maloberti
Dep. of Electrical, Computer and Biomedical Engineering
University of Pavia
Via Ferrata 1, Pavia, ITALY
E-mails: [edoard.bonizzoni, franco.maloberti]@unipv.it

***Abstract*—A four-path time interleaved current steering DAC is presented. It requires the same number of unity current generators of the plain counterpart, thanks to the use of a digital $\Sigma\Delta$ modulator, thus leading to a lower number of unity current switchings. The benefit is that the non-linearity caused by clock feedthrough is attenuated. Behavioral level simulation results show that the SFDR of a 12-bit DAC operating at 12 GS/s can be 60 dB.**

I. Introduction

Digital-to-analog converters (DACs) with medium-high resolution and conversion rate in the several GS/s range are more and more necessary for applications in the communication field. The DAC must provide very high sampling rates because new standards employ ultra wide bandwidths, [1]–[4]. The extremely high cutoff frequency, f_T, of the CMOS transistors designed with deep sub-micron technologies enables the switching of currents at extremely high rates. Thus, the current steering DAC architecture is the most adequate solution for ultra-high speed applications.

The current-steering architecture has been widely used in circuits and experimentally demonstrated very good performances in the hundreds MS/s range, [5]–[7]. The current steering scheme gives at the output a current injected into a resistive load. At very high frequency, the current flows through a coaxial cable and the load must have the cable matching value, typically 50 Ω.

The classical current steering architecture uses 2^N unity current generators switched toward the output(s) (for the single ended or the differential implementations) by differential switches made by MOS transistors. The matching between unity current generators and the switching strategy (i.e. the use of binary, unary, segmented selection, possibly using the random walk), [6]–[10], are well studied. All those issues are not discussed here because they are assumed known and properly applied to the design of current steering DACs.

What this paper considers is the limit that becomes significant when the sampling rate is in the multi-GS/s range: the clock feedthrough. When a MOS transistor switches on or off, a given amount of charge, corresponding to the charge in the channel, is injected at the two sides of the channel. Moreover, there is an injection of charge caused by the capacitive coupling between gate and output node. If the injection is non linear, harmonic distortion results. The limit is not very important at relatively low speeds, but is relevant at very high speed because the signal charge given by unity current multiplied by the clock period becomes low.

This paper first analyzes the problem associated to the clock feedthrough and then proposes a time interleaved scheme capable to reduce the clock feedthrough non-linearity by the interleaving factor.

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II. Clock Feedthrough

The circuit of Fig. 1 represents the unity cell of an N-bit current steering DAC switching its unity current, I_u, on the load resistances R_1 or R_2 ($R_1 = R_2 = R_L$), under the control of the driving signals V_1 and V_2. The current generators kI_u and $(2^N-1-k)I_u$ are for the other unity elements. They determine the output voltages for a given input code, k.

The switching of that single cell causes injection of charge into the output loads. The transistor turning on needs charge to create the channel; the one turning off disperses the channel. The charge in the channel is given by

$$Q_{ch} = (C_{ox}WL)(V_{GS} - V_{th}) \tag{1}$$

where C_{ox} is the oxide capacitance per unit gate area.

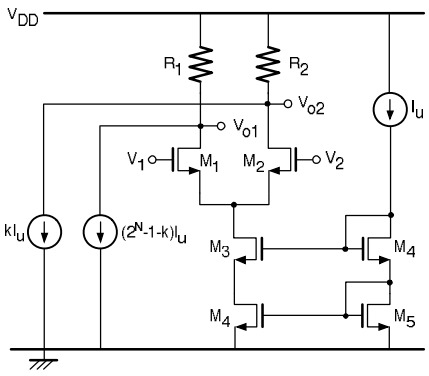

Fig. 1. Unity current steering cell schematic diagram.

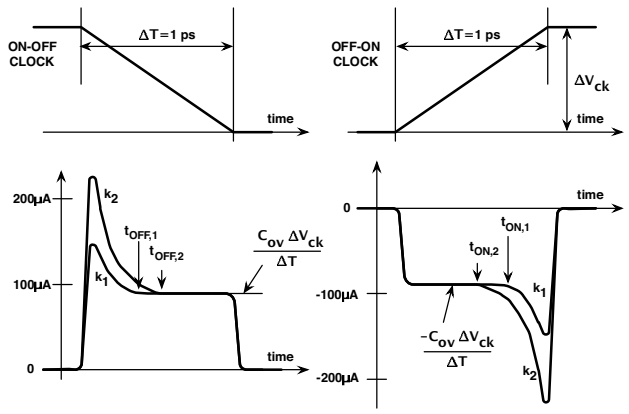

Fig. 2. Current waveforms at clock transitions.

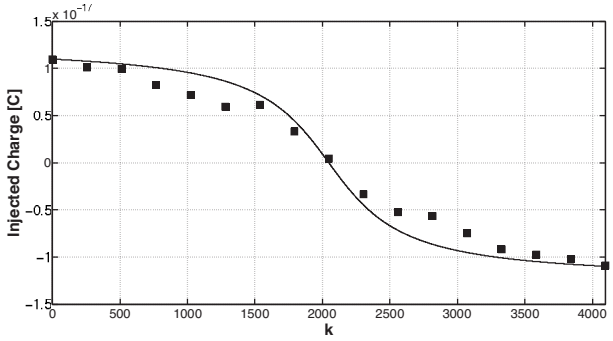

Fig. 4. Total charge injected with differential RZ driving at clock transitions.

If the conversion speed is several GS/s, the clock period is hundreds of ps and the rise and fall time of the phases driving the switches must be extremely small. Since the switching is almost instantaneous, in first approximation, we can assume that there is no difference between the injections on the two switch sides: half of the channel charge goes to the source and half to the drain. Moreover, there is the C_{ov} coupling, being C_{ov} the overlap capacitance per unit width. Therefore, the clock feedthrough charge is approximated by

$$Q_c = \frac{1}{2}(C_{ox}WL)(V_{GS} - V_{th}) + Wx_{ov}C_{ov}\Delta V_{ck} \qquad (2)$$

where x_{ov} is the overlap extent.

Since deep sub-micron technologies use oxides with high dielectric constant, C_{ox} is relatively large. The estimation of Q_c for a minimum area transistor realized with a 65 nm technology ranges from 80 aC to 150 aC. With $1\,V_{FS}$, 12-bit and $R_L = 50\ \Omega$, the unity current is 2.929 μA that, for 3GS/s and 50% return to zero, leads to 498 aC, only 3-6 times larger than the one due to the clock feedthrough.

Computer simulations give rise to a quantitative estimation of the clock feedthrough. The circuit of Fig. 1 implemented with a 65-nm CMOS technology, minimum transistor sizes, $R_L = 50\,\Omega$, $N = 12$, and $I_u = 2.929$ μA is the test vehicle. The rising and falling edge of the driving signals $V_{1,2}$ is 1 ps.

The current injected into the output node depends on the overdrive voltage determined by the value of the number of unity cells which are switched on. Fig. 2 shows typical waveforms. The figure outlines the time at which the transistor goes off and on. The off-to-on and the on-to-off waveforms seem symmetrical but in reality there is a slight difference. Because of the very fast switching, the peak of the glitch of current is much larger than the switched current itself.

Fig. 3 shows the charge injected for the off-to-on and on-to-off transitions as a function of the input code k, where the dots and the lines (solid and dashed) denote behavioral level simulation results and polynomial fitting curves, respectively. The result is not linear because the charge on the channel depends on the overdrive voltage. The charge due to the capacitive coupling is almost output voltage independent. Moreover, the transition on-to-off differs from the inverse of the one of the complementary case. The two curves can be used to estimate the injected charge for non-return-to zero (NRZ), differential NRZ, return-to zero (RZ) and differential RZ. The NRZ cases give rise to very poor results. Even the single ended RZ is source of significant non-linearity. As expected, the differential RZ is the optimal solution.

With a differential RZ mode, the positive injection partially balances the negative injection; the resulting residual charge, $Q_{c,d,RZ}$ gives rise to the diagram of Fig. 4. There is a linear

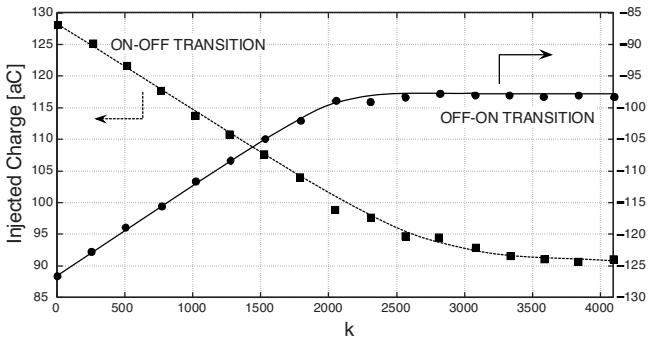

Fig. 3. Charge injected as a function of the input code k.

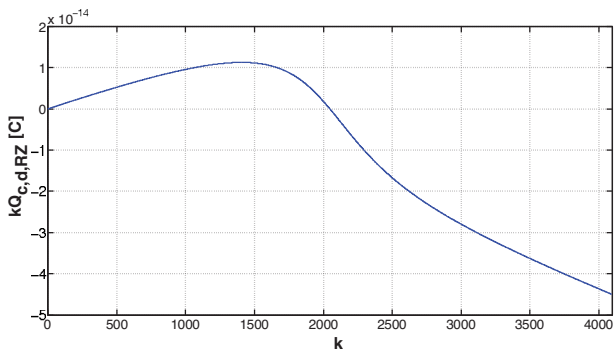

Fig. 5. Distortion current as a function of the input code k.

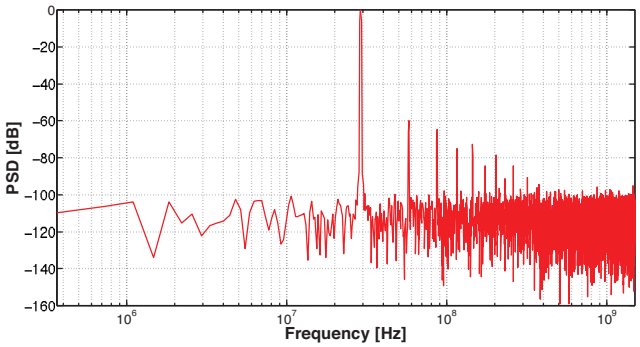

Fig. 6. Simulated output spectrum of a 12-bit 3-GS/s current steering DAC.

component, whose effect is a gain error, and a non linear component that causes harmonic distortion. When k unity current sources switch on and off, the total injected charge is the one shown in Fig. 5. For sine wave symmetrical with respect to the mid point ($k = 2048$), there is a remarkable distortion when the amplitude is larger than 0.1 full scale peak to peak.

The distortion current, $I_d = Q_{c,d,RZ}/T$, added to the average unity current and multiplied by the number k of current sources performing the on-to-off transition gives the output voltage

$$V_{out}(k) = k\left[\bar{I}_u + \frac{Q_{c,d,RZ}(k)}{T}\right]R_L \qquad (3)$$

When the conversion rate is high, the distortion current becomes several $\bar{I}_u$ and the non-linearity gives rise to significant harmonic distortion.

The accuracy of the simulation results has been indirectly verified with the experimental results given in [2]. The paper describes a 12-bit 2.9 GS/s current steering DAC with 2.5 V_{FS}. It achieves 80 dB SNR. A behavioral simulation of a 12-bit 3-GS/s DAC which accounts for the $kQ_{c,d,RZ}$ behavior of Fig. 5 obtains the output spectrum shown in Fig. 6. Harmonic tones are well visible. The SFDR is dominated by the second harmonic tone. It is at -60 dB_c, matching the experimental result published in [2].

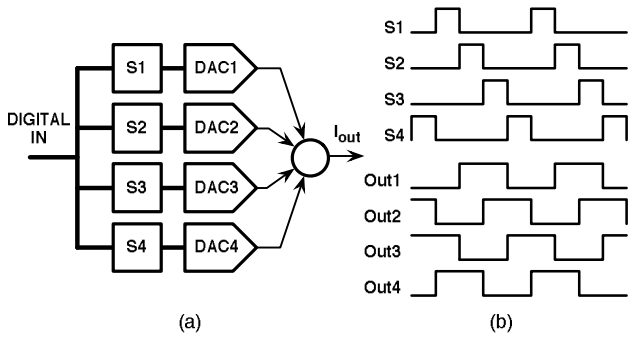

Fig. 7. a) Four paths time-interleaved RZ current steering DAC. b) S_i are the sampling periods, Out_i the phases controlling the four outputs.

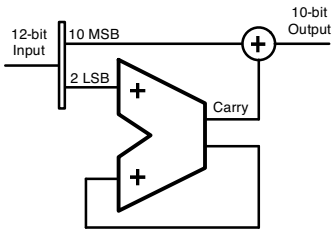

Fig. 8. Digital ΣΔ used before the time interleaved DAC to reduce the resolution from 12-bit to 10-bit.

III. Time Interleaved Architecture

Possible methods for reducing the clock-feedthrough non-linearities are: use low switching rate, use a low number of switching elements, use a large full scale voltage to increase the unity current. The first method is not possible for ultra-high speed. The second is a limit to resolution. The last one is possible within limits.

The use of a time-interleave scheme increases the conversion speed. Fig. 7 shows a 4-path architecture with RZ. Every channel samples the digital input every 4 clock periods and the outputs have a 50% duty cycle for the required return-to-zero. The architecture gives rise to a $(1+z^{-1})$ transfer function. There is a zero at Nyquist ($f_N = f_{ck}/2$) and a non negligible attenuation as the frequency increases. However, the simple digital IIR filter $(1/(1 + 0.875z^{-1}))$ compensates for the loss until more than half of f_N.

The time interleaved solution augments the conversion rate, but does not help in reducing the number of unity current generators that switch on and off. A possible solution is to use a single pair of switches for the parallel connection of a binary power of unity current sources. The disadvantage, however, is a mismatch in the on-resistance of the switches and this is source of non-linearity. The solution proposed here is to exploit the oversampling, always used in DACs. It grants a gray region between the band of interest and its replica used by the reconstruction filter.

Suppose that the used oversampling is 8. The use of a digital ΣΔ can reduce the number of bits at the input of each DAC by 2 so that the number of unity elements switched in each path is divided by 4 and the number of total switched elements remains unchanged. The digital ΣΔ, as Fig. 8 shows, processes the 2-LSB of the digital word. It is a simple 2-bit accumulator whose carry-out is added to the 10 MSB of the input. The error caused by the truncation from 12 to 10 bit passes through a noise shaping function $(1 - z^{-1})$, enough to limit the loss of the SNR to a fraction of bit. The digital ΣΔ operates at the full speed of the converter. That is challenging but possible with deep sub micron technologies. Moreover, parallel processing reduces the computation speed.

IV. Simulation Results

The above described method has been validated at the behavioral level using the Matlab-Simulink™ environment. The scheme of Fig. 7 with 4 paths made by 12-bit DACs with return-to-zero output gives rise to the output spectrum

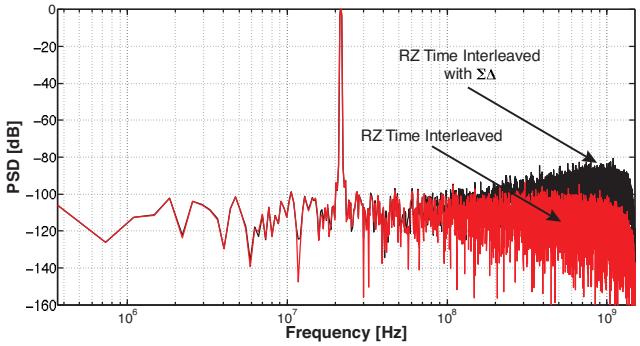

Fig. 9. Simulated output spectrum of a time interleaved RZ DAC with and without ΣΔ.

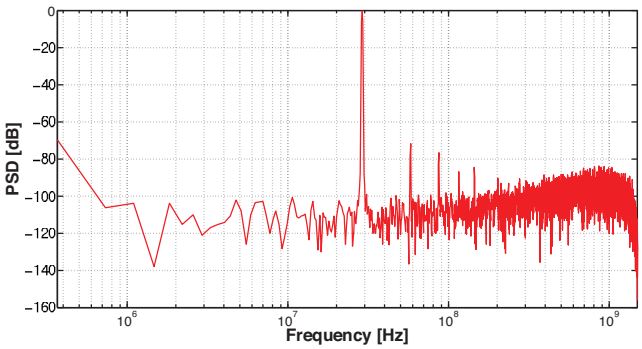

Fig. 11. Simulated output spectrum of the proposed DAC when considering clock feedthrough effect.

of Fig. 9. There is, as expected, a zero at Nyquist due to the $(1+z^{-1})$ transfer function determined by the time-interleaved RZ. The quantization noise power from zero to $f_N/8$ leads to a SNR of equal to 83 dB corresponding to 13.5-bit. The use of the digital ΣΔ which reduces the required number of unity current sources from 2^{12} to 2^{10} gives rise to the second spectrum of Fig. 9. The SNR is 80.7 dB equivalent to 13.1-bit. The 0.4-bit cost is affordable when considering the benefit on the SFDR shown below.

The non-linear injection of charge caused by clock-feedthrough gives rise to the spur signal shown in Fig. 10. It comprises a component at the input frequency and high order harmonics, as shown by the spectrum of Fig. 11. The second harmonic tone is at -72 dB_c. Compared to the spectrum of Fig. 6, there is a 12 dB improvement in the achieved SFDR.

The design can trade the 12-dB benefit granted by the ΣΔ time interleaved architecture with other features. It can reduce the full scale voltage across the 50 Ω loads or can increase the conversion speed. For the latter option, the method permits to increase by a factor 4 the conversion speed. The considered case can extend its operation up to 12 GS/s, while achieving a SFDR of 60 dB.

V. Conclusion

The non-linearity of the clock feedthrough is the main limit to SFDR for high conversion rate current steering DACs. This study, after quantifying the limit, shows that a 65-nm CMOS time interleaved architecture with four 10-bit DACs driven by a digital ΣΔ modulator processing the 12-bit input obtains 60-dB SFDR at 12 GS/s.

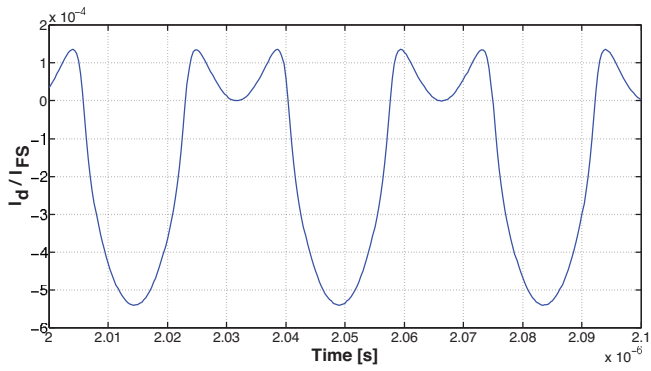

Fig. 10. Transient simulation of the distortion current.

Acknowledgment

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