A Highly-Linear Ultra-Wideband Balun-LNA for Cognitive Radios

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Abstract— This paper presents an highly-linear ultra-wideband balun low-noise amplifier (LNA) for cognitive radios covering the 50MHz to 10GHz band. It exploits a three-stage dc-coupled common-source amplifier, with *RC* degeneration at the last stage to optimize the gain, linearity and output gain-phase balancing. Designed in 65nm CMOS, throughout the covered band the simulated voltage gain is ~24dB whereas the noise figure is <3.6dB. Due to the *RC* degeneration IIP_2 and IIP_3 reach 32.4dBm and -2dBm, respectively. The power consumption is 21.7mW at 1.2V.

I. INTRODUCTION

The rapid downscaling of CMOS has led to more compact and faster RF circuits. The emerging cognitive-radio (CR) receivers demand a high-performance ultra-wideband (UWB) balun low-noise amplifier (LNA) to support many alternative communication channels from 50MHz to 10GHz, avoiding the need of multiple off-chip baluns and maximizing the hardware reuse in expensive nm-length CMOS technologies [1]. The UWB balun-LNA to be addressed here will adopt the resistive-feedback technique to achieve inductive peaking for widening the passband bandwidth without any inductor. The LNA is supposed to be applied in a zero-IF receiver as outlined in Fig. 1.

The two key challenges associated with CR receivers are: 1) the broadband characteristic, i.e., relatively flat gain, low noise figure (NF) and matching over the covered frequency band; plus 2) the linearity. A high linearity is essential to minimize unwanted mixing of in-band blockers, which can consume much more power than the desired frequency.

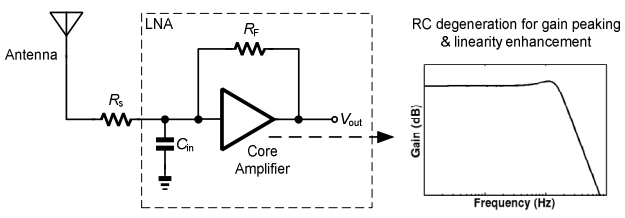


Fig. 1. LNA utilization in a direct-conversion receiver.

In this work, in order to achieve sufficient input matching quality (i.e., S_{11} <-10dB), low NF, high linearity, including both IIP2 and IIP3, and low power consumption, a novel UWB balun-LNA will be introduced, which exhibits an optimized tradeoff among the desired parameters and is more adequate for ultra-scaled CMOS technologies.

The conventional common-gate (CG) LNA [2], which was preferable for its wideband impedance matching capability ($R_{in} = 1/g_m$), unfortunately shows a high NF (typically greater than 3dB). Here, the concept reported in [3] that employs three common-source (CS) amplifiers in cascade as the LNA core is extended, proposing an UWB balun-LNA that is capable of generating differential outputs, avoid any inductor and improve output gain-phase balancing, IIP2 and IIP3.

Section II discusses the design considerations of the proposed wideband balun-LNA. Section III highlights the simulation results. The conclusions are drawn in Section IV.

II. PROPOSED UWB BALUN-LNA

The schematic of the proposed UWB balun-LNA is depicted in Fig. 2. The input signal is fed into the CS input stage. The external capacitor C_{in} is for AC coupling. With the high-pass corner frequency as low as 50MHz C_{in} is selected as 150pF to guarantee high-quality matching at low frequency. Here, the LNA employs three CS stages in cascade to provide sufficient

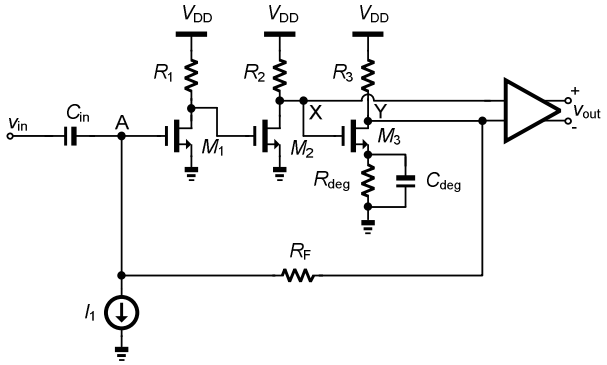


Fig. 2. Schematic of the proposed UWB balun-LNA.

loop gain for the negative feedback with R_F to achieve better noise figure and input matching. The input transistor M_1 has a large width to minimize the noise since the thermal noise of a MOS device is approximately given by $I_{n,M}^2 = 4kT\gamma g_m$, where γ is the noise factor of the transistor, k is the Boltzmann's constant and T is the temperature.

The output signal is obtained from the pseudo-differential sensing i.e. subtracting v_Y from v_X. Based on such a pseudo-differential sensing the even-order linearity (IIP_2) can be improved due to partial signal cancellation. However, the non-linearity cancellation relies on phase and gain matching nodes X and Y. To minimize the difference between X and Y, the gain of the third stage is therefore sized to be close to 0 dB. In [3] the third stage of the LNA is a simple CS amplifier which provides a relatively large gain, thus leading to a degraded nonlinearity cancellation.

In the proposed LNA source degeneration is applied (*RC* parallel branch) in the third stage to lower the gain, as well as providing better matching between nodes X and Y, besides improving also the linearity. However, the source degeneration resistor R_{deg} degrades the high frequency input matching. Thus, the degeneration capacitor C_{deg} is added to boost up the bandwidth of the balun-LNA, helping as well the input impedance matching at high frequency.

The calculations of the gain and R_{in} are based on the equivalent circuit shown in Fig. 3.

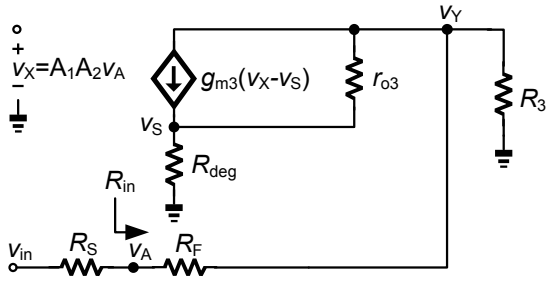


Fig. 3. LNA's small signal model of gain and R_{in}.

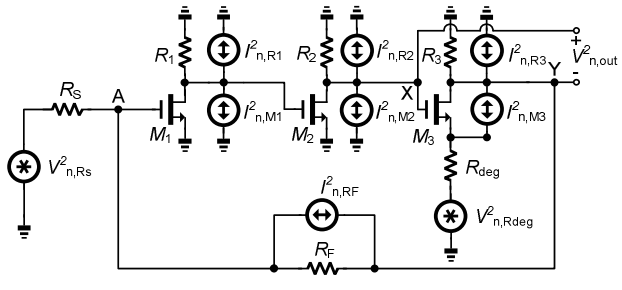


Fig. 4. Noise model.

In order to simplify the calculations the body effect will not be considered. The close loop gain and the input impedance can be determined as,

$$A = \frac{v_A}{v_{in}}\frac{v_X - v_Y}{v_A} = \frac{2R_{in}}{R_{in}+R_S}\frac{v_X - v_Y}{v_A} \quad (1)$$

$$v_X = A_1A_2v_A$$

$$v_Y = (R_3||R_F||R_{eq})(\frac{1}{R_F} - \frac{g_{m_3}A_1A_2r_{o_3}}{R_{eq}})v_A$$

$$R_{in} = \frac{1+\frac{R_F}{R_3}+\frac{R_F}{R_{eq}}}{\frac{1}{R_3}+\frac{1+A_1A_2g_{m3}r_{o3}}{R_{eq}}}, \quad (2)$$

where

$$A_1 = -g_{m_1}(R_1||r_{o_1})$$
$$A_2 = -g_{m_2}(R_2||r_{o_2})$$
$$A_3 = -\frac{g_{m_3}r_{o_3}[R_3||(R_S+R_F)]}{R_3||(R_S+R_F)+R_{eq}} \quad (3)$$
$$R_{eq} = r_{o_3} + (1+g_{m_3}r_{o_3})R_{deg} \quad (4)$$

According to (3) and (4) the resistor R_{deg} degenerates the gain of the third stage (A_3) therefore enhancing the gain matching. However, the tradeoff is that the close loop gain will also degrade as determined by (1). Input reflection S_{11} depends on input matching. In a CS amplifier the input impedance is capacitive. When the feedback resistor R_F is applied it will modify the input impedance in order to match 50Ω (2). In the proposed structure R_{in} is designed at 42.3Ω.

Considering wideband applications, the noise figure calculation only accounts the thermal noise, according to the circuit shown in Fig. 4. The total output noise power is given by

$$\overline{V^2}_{n,out} = \sum \overline{(V_{n,x} - V_{n,y})^2}$$
$$= \frac{1}{(1-\beta A_o)^2}\sum \overline{(V_{n,xo} - V_{n,yo})^2}$$
$$= \frac{1}{(1-\beta A_o)^2}(\overline{V^2}_{n,in}+\overline{V^2}_{n,\beta}+\overline{V^2}_{n,1}+\overline{V^2}_{n,2}+\overline{V^2}_{n,3})$$

where

$$\overline{V^2}_{n,in} = \overline{V^2}_{no,R_S}$$
$$\overline{V^2}_{n,\beta} = \overline{V^2}_{no,R_F}$$
$$\overline{V^2}_{n,1} = \overline{V^2}_{no,R_1} + \overline{V^2}_{no,M_1}$$
$$\overline{V^2}_{n,2} = \overline{V^2}_{no,R_2} + \overline{V^2}_{no,M_2}$$
$$\overline{V^2}_{n,3} = \overline{V^2}_{no,R_3} + \overline{V^2}_{no,M_3} + \overline{V^2}_{no,R_{deg}}$$
$$A_o = A_1A_2A_3$$
$$\beta = \frac{R_S}{R_S+R_F}$$

Thus, the noise figure is obtained as

$$NF = \frac{1}{4kTR_S} \frac{\overline{V^2}_{n,out}}{(\frac{R_{in}}{R_S+R_{in}}A)^2} \quad (5)$$

According to (5) the noise of the third stage can be ignored, being the NF 2.3 dB.

TABLE I
PARAMETERS OF BALUN LNA

Parameter	Value	Parameter	Value
M_1 (W/L)	115.5 µm /0.12 µm	R_3	77 Ω
M_2 (W/L)	32 µm /0.06 µm	R_F	450 Ω
M_3 (W/L)	58.8 µm /0.06 µm	R_{deg}	15 Ω
R_1	70 Ω	C_{deg}	1.5 pF
R_2	150 Ω	C_{in}	150 pF

III. SIMULATION RESULTS

The proposed UWB balun-LNA has been designed and optimized in 65nm CMOS, with Cadence™ as the simulator. Table I shows the obtained model parameters. The devices employed are 1.2-V thin-oxide transistors and the loading capacitance is assumed to be 40 fF (differentially). Figure 5 shows the simulated gain and NF of the balun-LNA and also compares it with the measured circuit results from [3]. The voltage gain ranges from 23.9 to 24.9dB when the frequency changes from 50MHz up to 10GHz and the achieved NF varies from a maximum of 3.6dB (50MHz) to a minimum of 2.7dB (1GHz), and finally increases to 3.4dB at 10GHz. The simulated S_{11} of the LNA is plotted in Fig. 6. The S_{11} is less than -10dB over the covered frequency and the phase margin is around 49°.

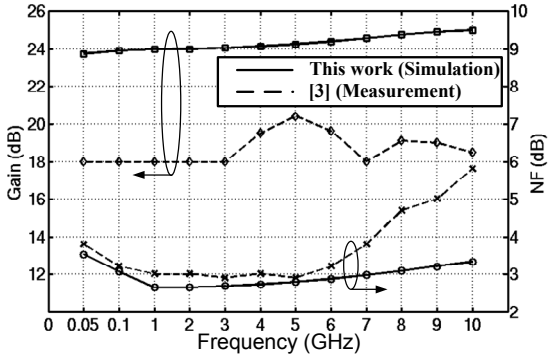


Fig. 5. Simulated gain and NF of the proposed LNA and comparison with the circuit from [3].

The gain and phase matching of the nodes X and Y throughout the passband were also observed. With better gain and phase matching a better IIP_2 can be achieved due to the sizing strategy, as described in Section II. As presented, the gain matching can be improved due to the degeneration of the gain of the third stage A_3. The impedance R_{deg} is 15Ω such that a better gain and phase matching can be obtained. On the other hand, we can optimize the bandwidth between the second and third stages to achieve better phase matching. However, reducing the power of the second stage will directly disturb the linearity. Here, the power of the third stage can be increased by reducing the power of the first stage. As mentioned before, the first stage contributes with a high gain in order to minimize the noise of LNA. The simulated gain and phase mismatches are plotted in Fig. 7(a) and (b), respectively. The gain mismatch ranges from 1.8 to 3.5dB and the phase mismatch ranges from -6.8 ° to 1.2 °, when the frequency varies from 50 MHz to 10 GHz.

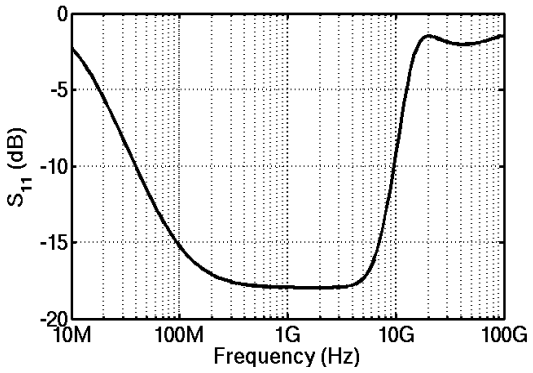
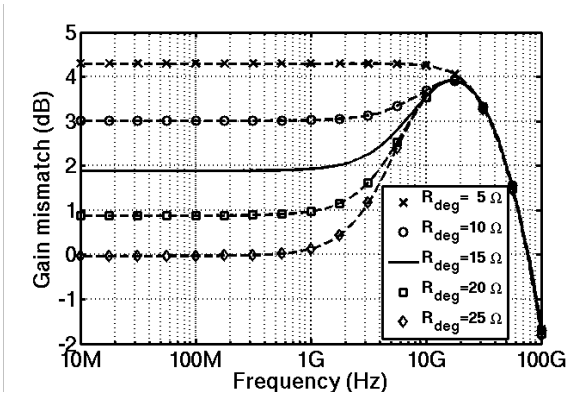
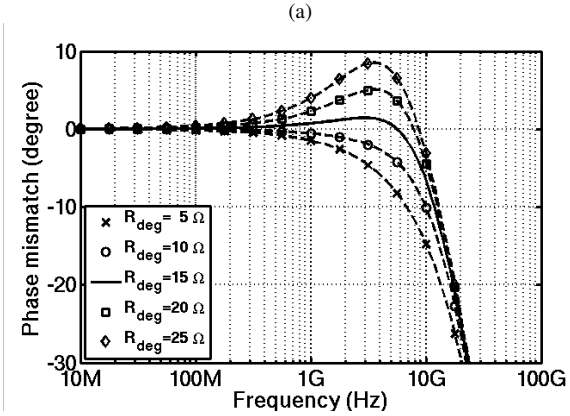


Fig. 6. Simulated S_{11}.



(a)



(b)

Fig. 7. Output mismatches with respect to R_{deg}: (a) gain and (b) phase.

For the IIP_2 and IIP_3 simulation results two-tone tests with spacing of 300 MHz are applied. The simulated IIP_2 and IIP_3 of the balun-LNA are shown in Fig. 8, together with the measured results from [3]. Finally, Table II compares the overall performance of the proposed UWB balun-LNA with the state-of-the-art, confirming the feasibility of the proposed structure in improving both IIP_3 and IIP_2 with minor add-on circuitry, while the other parameters are also maintained highly comparable.

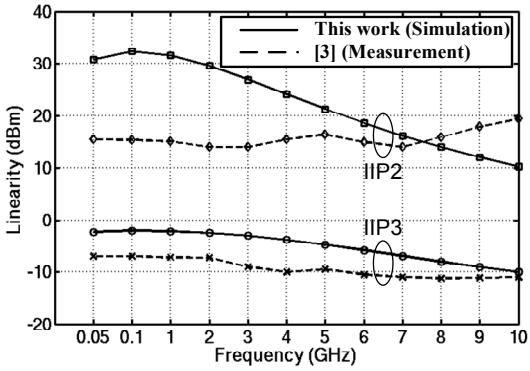


Fig. 8. IIP_2 and IIP_3 of the proposed UWB balun-LNA and comparison with the circuit from [3].

TABLE II
COMPARISON OF THE PROPOSED BALUN-LNA
TO THE STATE-OF-THE-ART.

	[3]	[4]	[5]	[6]	[7]	This work*
CMOS Tech.	65 nm	65 nm	90 nm	0.18 µm	90 nm	65 nm
Bandwidth (GHz)	0.05-10	0.2-5.2	0.5-8.2	3.1-10.6	2.7-4.5	0.05-10
S_{11} (dB)	<-10	-12	-7	-11	-7.5	<-10+
S_{21} (dB)	18-20	13-16	22-25	9.8	18-19.6	24-25
NF (dB)	2.9-5.9	2.9-3.5	1.9-2.6	4.5-5.1	4.0-5.0	2.7-3.6
IIP_2 (dBm) (min/max)	14/ 19.5	>20	NA	10/ 20	NA	10.2/ 32.4
IIP_3 (dBm) (min/max)	-11.2/ -7	>0	-4/ -16	-6.2/ -5	-8	-10/ -2
Power (mW)	22	14	42	20	8	21.7

* Simulation results. + 50 MHz to 9.3 GHz.

IV. CONCLUSIONS

The performance of a novel UWB balun-LNA employing cascade of CS amplifiers with resistive feedback, pseudo-differential sensing and partial *RC* degeneration, showing improved linearity and better output gain-phase balancing, has been demonstrated in 65nm CMOS. Extensive simulation results verify the feasibility of the circuit with respect to the state-of-the-art. Throughout the covered band the simulated voltage gain is >23 dB whereas the noise figure is <3.6 dB. The IIP_2 is 32.4dBm and the IIP_3 is -2dBm. The power consumption is 21.4mW at 1.2V.

ACKNOWLEDGEMENT

This work was funded by the Research Committee of University of Macau, and Macao Science and Technology Development Fund (FDCT).

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