A 0.6V 8b 100MS/s SAR ADC with Minimized DAC Capacitance and Switching Energy in 65nm CMOS

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***Abstract*—This paper presents a monotonic multi-switching technique that is implemented in a 8b SAR ADC. The proposed switching reduces 1/2 total DAC capacitance and achieves more than 80% switching energy saving when compared to the most advanced V_{CM}-based or merged capacitor switching methods. Besides, conversion redundancies are added to compensate the errors resulting from insufficient DAC settling and reference noise. The proposed 8-bit SAR ADC operates at 100MS/s with 0.6V supply in 65nm CMOS. The simulation results show that the design achieves 48.8dB SNDR with only 0.524mW power. The Figure-of-Merit (FoM) is 23.35fJ/conversion-step.**

I. INTRODUCTION

Technique down scaling benefits the digitalized analog-to-digital (ADC) architecture such as Successive Approximation Register (SAR) ADCs, since the shrink of supply and the size of transistor significantly improve the power efficiency of the digital circuitry. The performances of previous SAR ADC designs are often limited by the analog blocks, including the comparator [1]-[3] and digital-to-analog converter (DAC), while recently many approaches have been targeting the optimizations of its analog power efficiency: 1) The static power dissipations from reference generator [1]-[3] and preamplifier [3] are avoided by using supplies directly as reference and a simple dynamic latch; 2) The switching energy and conversion linearity are improved by applying advanced switching approaches [1]-[3]. The above solutions significantly reduce its analog power to a level that is even lower than the digital circuit power consumption. Accordingly, for a design target of low (1kS/s-1MS/S) or medium speed (10MS/s-100MS/s) ADC, SAR ADCs achieve the lowest FoM when compared with the other type of ADCs [4]. Obviously, one effective solution to further minimize the power dissipation in a SAR ADC is to use an ultra-low-supply. Because the dynamic digital power is defined by $\alpha C_{LOAD} V^2_{DD}$ (α is an activity factor of a clock) it reduces exponentially as the supply scales down.

However, the reduction of V_{DD} allows smaller signal power and decreases the Signal-to-Noise Ratio (SNR), leading to a stringent requirement of kT/C noise, as well as the accuracy of the comparator and DAC settling. The kT/C noise can be minimized by increasing the total array capacitance. Inserting some redundant bits can effectively alleviate the conversion error including dynamic offset, insufficient DAC settling and supply variation.

This paper presents an 8b 100MS/s SAR ADC in 0.6V supply. The design can achieve both high-speed and conversion linearity by using two proposed strategies: 1) Optimizing the number of the redundancy bit and its extra capacitance to solve the trade-off between the accuracy relaxation and increased sampling capacitance; 2) Utilizing a proposed monotonic multi-switching method to achieve reduction of total array capacitance by 50% and more than 80% more switching energy saving when compared with its counterpart in [2]. Because this design implements a binary-weighted DAC with additional 56% redundancy capacitance, the total sampling capacitance is sufficient to satisfy the KT/C noise. Moreover, the compensation redundancy method in terms of tolerance of settling error and reference sensitivity is theoretically analyzed.

II. MONOTONIC MULTI-SWITCHING METHOD (MMS)

A. The SA Algorithm

The proposed switching technique, called monotonic multi-switching method (MMS), uses three reference voltages: V_{CM}, V_{REF} and ground to normalize the analog input range from 0 to 2^N-1. V_{XP} and V_{XN} are assumed as the two outputs of the DAC circuit and the comparator decides which is the larger. Its output *s(k)* at *k*-th step is defined by

$$s(k) = \begin{cases} 1 & (V_{XP} < V_{XN}) \\ 0 & (otherwise) \end{cases} \quad (1)$$

If *s(1)*=1, the negative input of the comparator is unchanged and the positive input in the *k*-th step is given by

$$V_{XP}(k) = V_{inp} + \sum_{i=2}^{k} s(i-1) * 2^{-(i-1)} \quad (2)$$

Oppositely, the positive input is kept the same and the neg-

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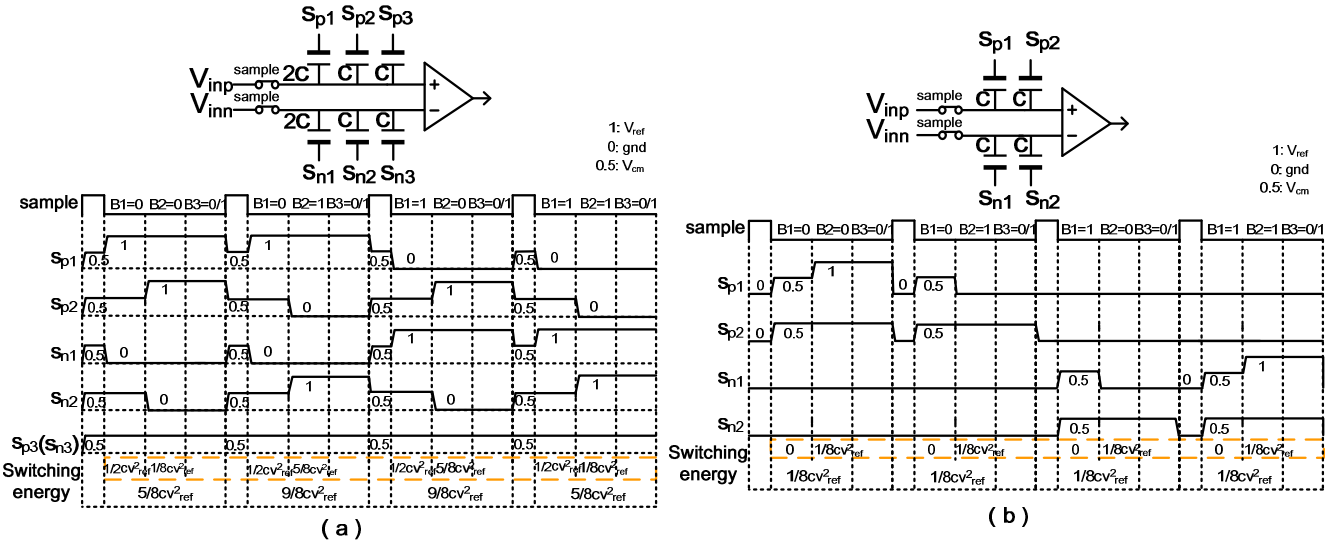

Fig. 1 Switching procedure of a 3-bit SAR ADC:(a) merged capacitor switching method; (b) proposed MMS method.

ative in the *k*-th step is given by

$$V_{XN}(k) = V_{inn} + \sum_{i=2}^{k} s(i-1) * 2^{-(i-1)} \tag{3}$$

where V_{inp} and V_{inn} are the differential analog inputs. Thus, the SAR ADC output Dout is given by

$$Dout = 2^{N-1} + \sum_{i=2}^{N} (1 - 2s(i-1)) * 2^{N-i} - s(N) \tag{4}$$

B. *Switching Procedure of MMS*

As some other advanced switching methods [1]-[3] tried to improve the aspects of switching energy efficiency and area reduction of the DAC circuit, the proposed MMS method cuts down more than half of total capacitance and saves 80% energy when compared with the merged switching.

Fig.1 details the merged switching and proposed MMS method in a 3-b example. In the sampling phase, the differential input V_{in} is stored in the capacitor array. MMS keeps all bottom plates connected to the ground while merged switching connects them to V_{CM}. Actually, both methods do not consume any energy in the sampling mode.

As shown in Fig. 1(b), for the first transition (*T1*), up transition is defined while V_{XP} increases. Otherwise, it is called down transition. For other transitions, if V_{XP} or V_{XN} increases, the transition is an up transition. Otherwise, it is a down transition. Taking *B1B2B3=011* as an example, the SAR ADC goes through one up transition and one down transition, successively.

In the MMS method a significant difference is the sign of the most significant bit (MSB) which determines the following SA comparison. Fig.1(b) shows that when *B1=0*, namely V_{inp} is smaller than V_{inn}, P-DAC array switches all bottom plates to V_{CM} and keeps N-DAC stable until the end of the conversion. Otherwise, the operation will be the opposite.

Switching energy is defined as the energy drawn from the reference voltage like V_{CM} or V_{REF} for conversion transition

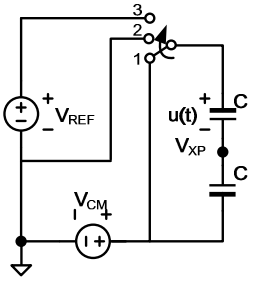

Fig.2 The switching procedure after B2 confirmed the positive input of the comparator

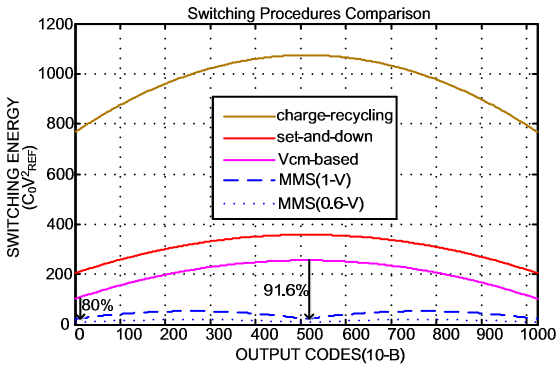

Fig. 3. Switching energy versus output code for different switching methods in 10-b resolution

[2][5]. In *T1*, MMS keeps the charge distributed by the capacitors as the same, not wasting any energy during *T1*.

After obtaining the second bit, the switching process of the second transition at *B1=0* is shown in Fig.2. The switch (SW) is connected to node '1' in *T1*. If *B2* equals to 0, it means that V_{XP} is still smaller than V_{XN}. Hence, SW in *T2* will be switched to '3' namely the up transition. Otherwise, it will be connected to '2' namely the down transition. Therefore, *t1*, *t2*, *t3* is respectively assumed as SW connected to '1', '2', '3' and *u(t)* is the voltage between the two nodes of the MSB capacitor.

By using *Laplace* transform to analyze the RC circuit, then *u(t)* is,

$$u(t)=\begin{cases}(-(V_{inp}+\frac{V_{REF}}{2}))\exp(-t/\tau)+(\frac{V_{REF}}{4}-V_{inp})(1-\exp(-t/\tau)) & (t_1 \text{ to } t_3)\\ (-(V_{inp}+\frac{V_{REF}}{2}))\exp(-t/\tau)+(-\frac{V_{REF}}{4}-V_{inp})(1-\exp(-t/\tau)) & (t_1 \text{ to } t_2)\end{cases} \quad (5)$$

where at t_1, $u(t_1)= -(V_{inp}+V_{REF}/2)$ and if given enough time to settle, $u(t_2)= -V_{inp}-V_{REF}/4$ and $u(t_3)= -V_{inp}+V_{REF}/4$.

For the up transition, if the capacitor array settles during t_3, the total energy drawn from V_{REF} and V_{CM} is

$$\begin{aligned}E_{1\to3} &= V\times i(t)t = V_{REF}\int_{t1}^{t3} i(t)dt + V_{CM}\int_{t1}^{t3} i(t)dt \\ &= V_{REF}\int_{t1}^{t3}\left(-C\times\frac{du(t)}{dt}\right)dt + V_{CM}\int_{t1}^{t3}\left(-C\times\frac{du(t)}{dt}\right)dt \\ &= -V_{REF}\times C\times\big(u(t3)-u(t1)\big)-V_{CM}\times C\times\big(u(t3)-u(t1)\big)=\frac{1}{8}CV^2{}_{REF}\end{aligned} \quad (6)$$

Assuming R is the switch resistance, the resistance energy E_R in the up transition is

$$E_R = R\times i^2(t)t = R\int_{t1}^{t3} i^2(t)dt = R\int_{t1}^{t3}(\frac{du(t)}{dt})^2 dt \quad (7)$$

From (5), the derivative of $u(t)$ can be used to calculate E_R and is $1/16\ CV^2{}_{REF}$. Other energy stored in the DAC array with the effective series capacitance, $1/2C$, is $1/16\ CV^2{}_{REF}$. Thus, the total switching energy drawn from the reference voltage is the addition of the resistance energy and the accumulation energy in the capacitor network. By following the above calculations, the switching energy of down transition can also be calculated as the same as that of the up transition.

Fig. 3 compares the switching energy of, the set-and-down[1], merged switching[2], charge-recycling[3] and the proposed MMS methods. This figure assumes an equal unit capacitor for the 10-bit SAR ADC. Actually, comparing with the conventional switching procedure, the charge-recycling, set-and-down, and V_{CM}-based methods use the 1.2-V supply voltage, and achieve 37%, 81% and 87% switching energy reduction, respectively. On the other hand, MMS reduces more than 96% or 98% with either 1-V or 0.6-V supply, respectively. Moreover, Table I exhhibits different features of these various switching.

In addition, since V_{CM} is the additional reference of the DAC array, the SAR ADC must ensure its stability. As usual, the V_{CM} generated by a resistance ladder is directly related with such resistance. A more stable V_{CM} means larger energy consumed by the resistance. On the other hand, the resistance in the ladder cannot be very large. Moreover, the input common-mode (CM) of the comparator varies between the peak voltage of the input and the V_{CM} according to the proposed switching. As a result, the CM variation would cause dynamic offset. The sensitivity of $V_{REF}/2$, especially with ultra-low-supply, can cause signal dependent reference error (SDRE). Actually, if the variation of $V_{REF}/2$ is less than 1LSB, the final conversion would not affect too much the ADC performance. Otherwise, SDRE can result in wrong conversion for some particular points of the sine wave input signal leading finally to a significant SNDR drop.

In sum, a comparator insensitive to the input CM range [6] must be designed, and the redundancy [7] should also be combined to compensate the conversion errors happening in the previous decisions

Table I. Comparison of switching methods

Methods	Features		
	No. of capacitors	*No. of unit capacitors*	*Normalized Power*
Proposed	2N-2	2^{N-2}	0.013
Merged	2N	2^{N-1}	0.063
Set-and-down	2N	2^{N-1}	0.19
Energy-saving	4N-2	2^N	0.44
Split capacitor	4N	2^N	0.63
Conventional	2N+2	2^N	1

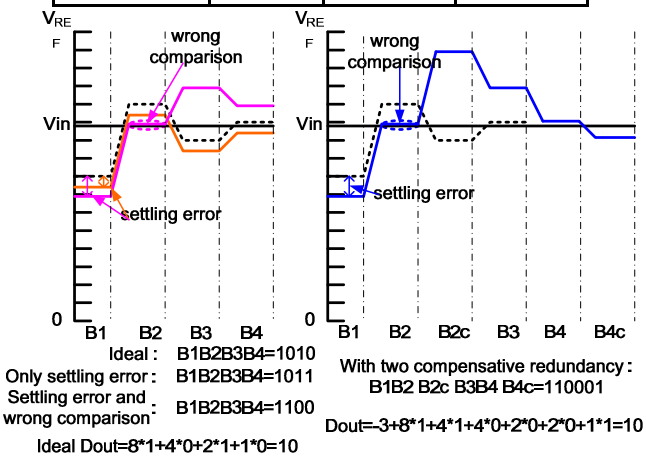

Fig. 4 Compensative redundancy to correct settling and decision errors

III. Compensative Redundancy Method

This redundancy method inserts two compensative capacitors with the termination capacitor used for bringing three redundant cycles to correct the error caused by supply variations and also relaxing the accuracy requirement for the comparator. Finally, the digital error correction converts 11b digital codes to 8b binary codes.

When there is a settling error or V_{CM} variation before getting the digital codes, the desired voltage $V_{REF}/(2n)$ (n-th transition) cannot be correctly added to inputs of the comparator. And also if the comparator result is wrong for one bit, the following switching would be different. These dynamic errors degrade the performance of the non-redundancy ADC. However, this compensative redundancy ADC can tolerate them with the help of some redundant compensative decisions. In Fig.4, a 4-b SAR ADC example and the respective conversion procedure are shown. The compensative method uses two redundant cycles to achieve 4b resolution.

Taking an example after the comparator finished the first comparison, for the MMS method, the first bit determines which input (V_{XP} or V_{XN}) will be added by $V_{REF}/2$. Then, if the comparator makes the second decision when the first DAC switching settles to 50% of its target value ($V_{REF}/2*50\%$), the maximum error is $V_{REF}/2$ ($V_{REF}/2*50\%+V_{REF}/4$), namely the incomplete settling value of the first DAC switching plus the second DAC switching. Either V_{CM} or supply voltage variation can cause the error. Because the remaining

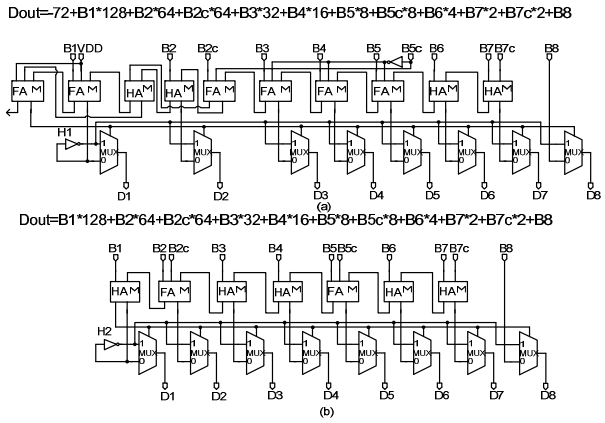

Fig.5 Digital correction circuit at B1=0 or 1

capacitors can only add $V_{REF}/4$ voltage to the DAC array, an additional voltage $V_{REF}/4$ must be compensated. The redundancy method inserts exactly a compensative capacitor that is the sum of the remaining capacitors' value which can produce the expected compensation voltage.

Two compensative capacitors are inserted in the binary capacitive DAC array and the percentage to the normal DAC array is 56%. Consequently, the amplitude of the input signal swing is $V_{REF}*(C_{or}/C_{total})$ where C_{or}, C_{total} is respectively the total capacitance without or with compensative capacitors. In the design, the peak-to-peak amplitude of input swing is 640mW with a unit capacitor of 3.6fF.

IV. Circuit Design & Schematic Simulation Results

The proposed MMS switching SAR ADC with compensative redundancy consisting of a dynamic comparator, DAR array, SAR logic and digital error correction are shown in Fig.5. The digital error correction aims to convert the 11b codes with error correction to 8b binary codes. The bit weights of the 11b codes are 128, 64, 64, 32, 16, 8, 8, 4, 2, 2, and 1. The digital output is

$$D_{out} = - (\sim B1)*72 + (128*B1+64*B2+64*B2C+32*B3+ 16*B4+8*B5+8*B5C+4*B6+2*B7+2*B7C+B8)$$

Because the digital codes have an offset of 72 at B1=0, the correction circuit has two components: one logic operation to remove the offset at *B1=0* and the other is the sum of multiplying digital by their bit weights at *B1=1*. Consequently, the sign of MSB controls one multiplexer to decide which one is the output. Fig.5 shows the logic implementation of the digital correction circuit, which consists of 3 inverters, 8 full adders, 9 half adders and 17 multiplexers. The half-adder H1 and H2 are used to detect overflow. If the signal swing is over range, overflow occurs and the digital output codes will be set to either 0 or 255 to keep the normal function.

The proposed 8-bit SAR ADC is designed in 65nm standard-V_T CMOS process. Except the clock generator and the digital error correction circuit, all other components were designed at transistor-level.

From transistor-level simulations, the SAR ADC using MMS without redundancy can tolerate 1% V_{CM} mismatch on the resistance ladder. If the variation becomes larger, the

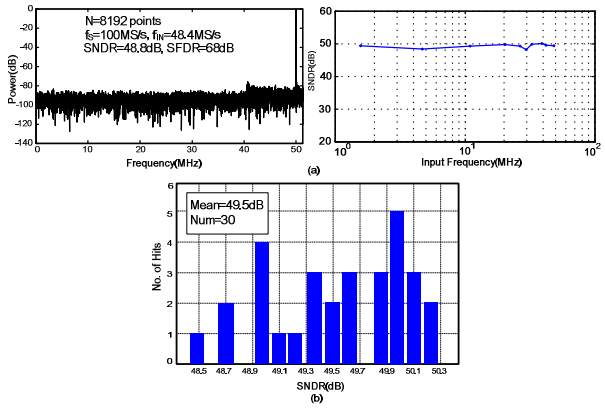

Fig.6 @ f_{IN}=48.4MHz, f_S=100MS/s (a)Simulated SNDR (with transient noise) versus input frequency and FFT of the 8192 digital output;(b) 30-time Monte-Carlo simulation

SNDR will drop significantly. With the bond-wire supply used, the SNDR of the ADC without redundancy is lower than 40dB. However, the compensative redundancy leads to a SAR ADC with MMS obtaining a stable SNDR, in the order of 48dB.

Fig. 6 (a) shows the SNDR versus input frequency and also provides the FFT spectrum at Nyquist input. The ENOB is 7.81-b and excluding the digital error correction and clock generator, the power consumption is about 0.524-mW from a 0.6V supply. According to the FoM equation defined as $Power/(2^{ENOB}*f_S)$, the ADC achieves 23.35*fJ/conversion-step*. Moreover, Fig.6 (b) shows the result of 30 times Monte-Carlo analysis, where the mean value is 49.5dB.

V. Conclusion

An 8b 100MS/s 0.6V SAR ADC with MMS switching and compensative redundancy has been designed in 65nm CMOS process. The ADC achieves the lowest switching energy and reduces more than 50% of the total capacitance when compared with merged SAR ADC. The ADC consumes less than 0.524-mW of power at the 100MS/s.

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