22.2 A 1.7mm² Inductorless Fully Integrated Flipping-Capacitor Rectifier (FCR) for Piezoelectric Energy Harvesting with 483% Power-Extraction Enhancement

Zhiyuan Chen[1], Man-Kay Law[1], Pui-In Mak[1], Wing-Hung Ki[2], Rui P. Martins[1,3]

[1]University of Macau, Macau, China
[2]Hong Kong University of Science and Technology, Hong Kong, China
[3]Instituto Superior Tecnico, Universidade de Lisboa, Portugal

Energy Harvesting is crucial to the development of miniaturized implants to achieve minimal invasiveness and system autonomy. While RF wireless power transfer suffers from substantial tissue attenuation, a wireless piezoelectric energy harvester (PEH) is more attractive for deep-tissue implant applications [1]. Typical PEH interfaces with a full-bridge rectifier for AC-DC conversion with limited extractable electrical power due to the PEH inherent capacitance (C_p). The parallel-synchronized-switch harvesting-on-inductor (P-SSHI) technique [2, 3] can increase the output energy by flipping the PEH voltage using resonance, whereas other techniques in [4] and [5] focus on boosting the PEH voltage swing to increase the extracted power. Yet, all of them require a bulky external high-Q inductor (up to the mH range in [3] and [5]) to ensure a high power-extraction enhancement. This work reports an inductorless fully integrated PEH interface, achieving a high voltage flipping efficiency (η_F) of 0.85 and a maximum output-power increasing rate (MOPIR) of 4.83× when compared with a full-bridge rectifier interface.

Conventionally, a large inductor extracts more power from the PEH [2] by extending the damping duration, with the assumption that the resonance frequency is much higher than the excitation frequency (f_{EX}) [4]. In cases that require a high excitation frequency as in PEH implants, the dependency of the resonance frequency and the extracted power on the inductor size ultimately sets a hard performance tradeoff, since both the phase offset and the flip time (t_{flip}) can significantly impact the system performance. The lack of on-chip high-Q inductors also renders the traditional approach inappropriate for PEH implants, where the system volume is of utmost importance. Our innovation to the PEH system (Fig. 22.2.1) is the introduction of a 7-phase flipping-capacitor rectifier (FCR). Instead of using an external high-Q inductor as the energy storage element, it achieves voltage reversion across C_p during the zero crossing of I_p through a reconfigurable capacitor array to effectively increase the conduction time, thus realizing a fully-integrated solution.

The reconfigurable capacitor array incorporates 4 flying capacitors ($C_{1\text{-}4}$) and 21 switches (Fig. 22.2.2). To reduce the charge redistribution loss due to flipping the PEH voltage (V_{ab}) we propose a step-wise reconfiguration cycle for both the positive and negative transition cycles (PTC/NTC) and optimize the arrangement of the capacitors to reduce the parasitic loss in each step. $C_{3,4}$ is twice the size of $C_{1,2}$ to balance the charge flow in each branch. During t_{flip}, the capacitor array (with a total capacitance C_{total}) swiftly flips V_{ab}, with the rebuilt voltage (V_r) computed as:

$$\frac{V_r}{V_{rect}} = \left[\frac{(1+x)^2}{x}\prod_{n=1}^{\frac{N-3}{2}}\frac{\left(1+\frac{x}{(n+1)^2}\right)^2}{\left(1+\frac{x}{n(n+1)}\right)^2} - \frac{4x}{(N-1)^2}\right]^{-1} \quad (1)$$

where $x=C_{total}/C_p$ and N≥3 is odd, which denotes the number of phases (N=1 is the special case of a switch-only rectifier). A larger V_r (and hence a higher power extraction enhancement) can be obtained by increasing both C_{total} and N. We choose x=18 and N=7 to balance the power extraction efficiency and design complexity and to achieve a theoretical η_F and MOPIR of 0.85 and 6.85× (Fig. 22.2.1), respectively.

The number of switching phases and RC settling limit the value of t_{flip} in FCR. With f_{EX}=110kHz, we choose a t_{flip} of ~1μs to optimize the losses due to reduced conduction angle and incomplete charge transfer (Fig. 22.2.3). The active rectifier with a common-gate comparator ensures high-speed operation to meet the stringent timing requirement while eliminating the diode voltage drop of passive rectifiers. The V_{ab} shorting phase aligns with the zero crossing of I_p to reduce the energy loss during t_{flip}. Controlled by V_C, M_C adjusts the current flowing through M_x to achieve a comparator delay tuning of 8.5ns/mV. M_f provides a positive feedback loop to guarantee fast comparator transitions. The SR latch enforces operation only during t_{flip}. The switches are transmission gates with active body biasing (Fig. 22.2.2) to reduce the switch on-resistance and secure a settling time of <150ns.

Figure 22.2.4 shows the schematic and the timing diagram of the phase generator, which provides the control vector $\overrightarrow{V_L}$ to the switch driver at $V_{p<1,2>}$ transitions. To guarantee non-overlapping controls and complete charge transfer, we introduce digital calibration in the pulse generator (PG) and the delay generator (τ_D), with delay inverters controlled by $C_{<0,1>}$ to adjust the pulse width and delay with a resolution of 25ns. The 6 τ_D blocks for delaying $V_{p<1>}$ ($V_{p<2>}$) generate $D_{1,-3}$ to $D_{1,3}$ ($D_{2,-3}$ to $D_{2,3}$), which are subsequently processed by PG to get $P_{1,-3}$ to $P_{1,3}$ and $d_{1,-3}$ to $d_{1,3}$ ($P_{2,-3}$ to $P_{2,3}$ and $d_{2,-3}$ to $d_{2,3}$) for pulse delay control. These control signals are systematically organized to generate ϕ_{-3} to ϕ_3, which are further combined to produce $\overrightarrow{V_{L<1:11>}}$. The phase combine circuit generates the multiphase pulses to effectively reduce redundant switching activities by 41% (from 41 to 24), thus improving the gate driving loss.

The proposed 7-phase FCR fabricated in 0.18μm CMOS occupies an active area of 1.7mm². The PEH (P5A4E) from Piezo Systems, Inc. serves as both the transmitter (76.4×76.4×1mm³) and the receiver (5×1×1mm³), placed 6cm apart inside an oil-filled container with oil serving as the transmission medium. C_p of the receiver is 80pF. $C_{1,2}$ and $C_{3,4}$ are 240 and 480pF, respectively. A 1V supply powers the phase generator for delay adjustment. Figure 22.2.5 shows that the measured PEH voltage swing at no load increases by >4× (from 2V to 8.5V) with the FCR turned on. After phase offset adjustment, the measured η_F increases to 0.85, corresponding to a 7% energy-loss reduction during t_{flip}. The FCR can deliver 50.2μW with a loading of 680pF//125kΩ at 110kHz. With 4 measured samples, the achieved MOPIR is larger than 3.3× from 80 to 130kHz, with an average of 4.78× at 110kHz.

Figure 22.2.6 illustrates the chip summary and performance benchmark. The proposed PEH system with FCR achieves an MOPIR better than 1.7× when compared to those of [2,4] that require small external inductors (47 and 330μH). Unlike [3,5] that achieve high MOPIR by using an excessively large external high-Q inductor, in the order of mH, this work reports a PEH that exhibits a high MOPIR (4.83×) and η_F (0.85) in a compact area using zero external components. Figure 22.2.7 shows the die micrograph with the area dominated by $C_{1\text{-}4}$ (84.7%).

Acknowledgements:
The authors thank Macao FDCT, MYRG100-FST13-LMK and MYRG2015-AMSV-00140 for financial support.

References:
[1] T. Maleki, et al., "An Ultrasonically Powered Implantable Micro-Oxygen Generator (IMOG)" *IEEE Trans. Biomed. Circuits Syst.*, vol. 58, no. 11, pp. 3104-3111, Nov. 2011.
[2] Y. K Ramadass, et al., "An Efficient Piezoelectric Energy-Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," *ISSCC*, pp. 296-297, Feb. 2009.
[3] D. A. Sanchez, et al., "A 4μW-to-1mW Parallel-SSHI Rectifier for Piezoelectric Energy Harvesting of Periodic and Shock Excitations with Inductor Sharing, Cold Start-up and up to 681% Power Extraction Improvement," *ISSCC*, pp. 336-337, Feb. 2016.
[4] D. W. Kwon, et al., "A Single-Inductor 0.35μm CMOS Energy Investing Piezoelectric Harvester," *ISSCC*, pp. 78-79, Feb. 2013.
[5] Y. S. Yuk, et al., "An Energy Pile-up Resonance Circuit Extracting Maximum 422% Energy From Piezoelectric Material in a Dual-Source Energy-Harvesting Interface," *ISSCC*, pp. 402-403, Feb. 2014.

 978-1-5090-3758-2/17/$31.00 ©2017 IEEE

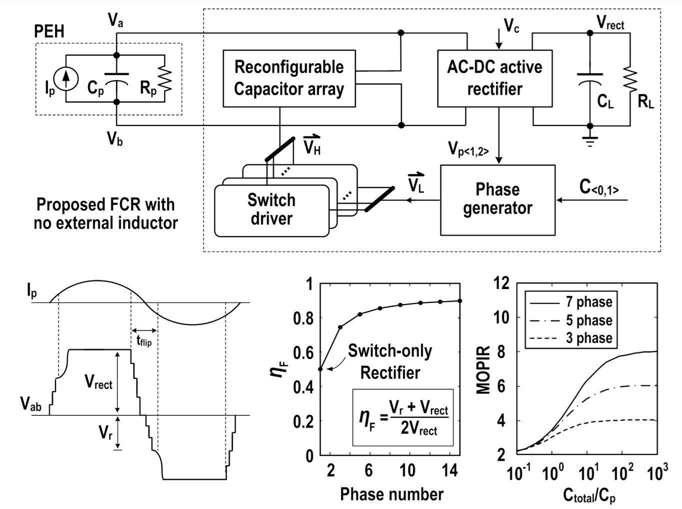

Figure 22.2.1: Proposed fully integrated flipping-capacitor rectifier (FCR) for piezoelectric energy harvesting, and its simulated voltage flipping efficiency (η_F) and MOPIR.

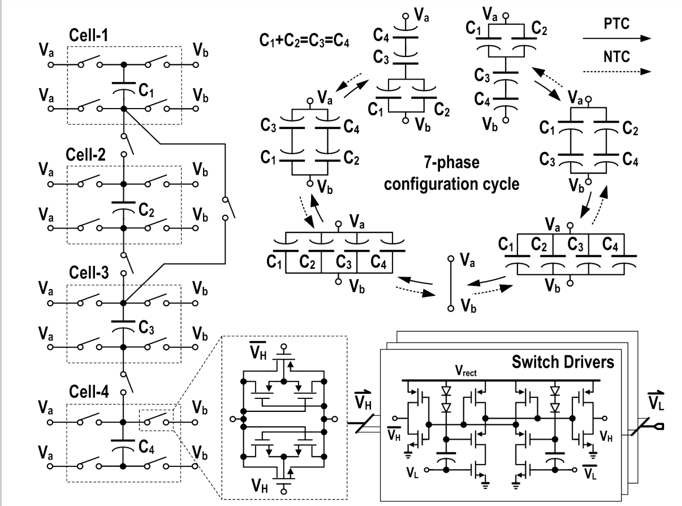

Figure 22.2.2: Implemented 7-phase FCR and its configuration cycles during both positive and negative transition cycles (PTC/NTC), and details of the switch drivers.

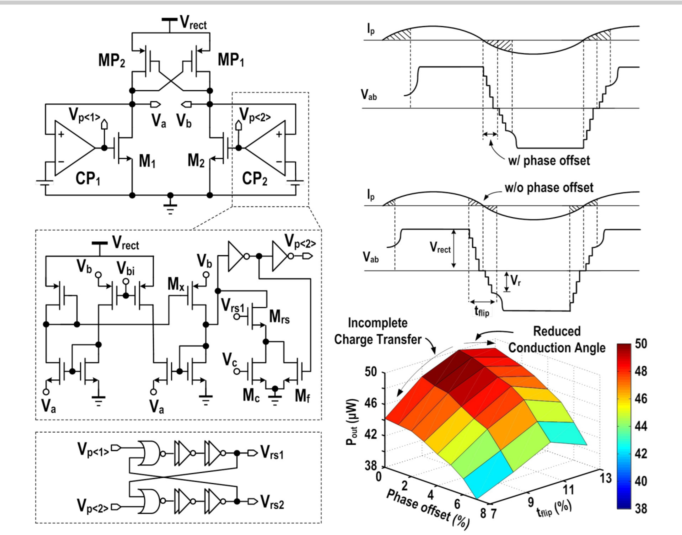

Figure 22.2.3: Active rectifier and the simulated P_{out} with different phase offset and t_{flip}.

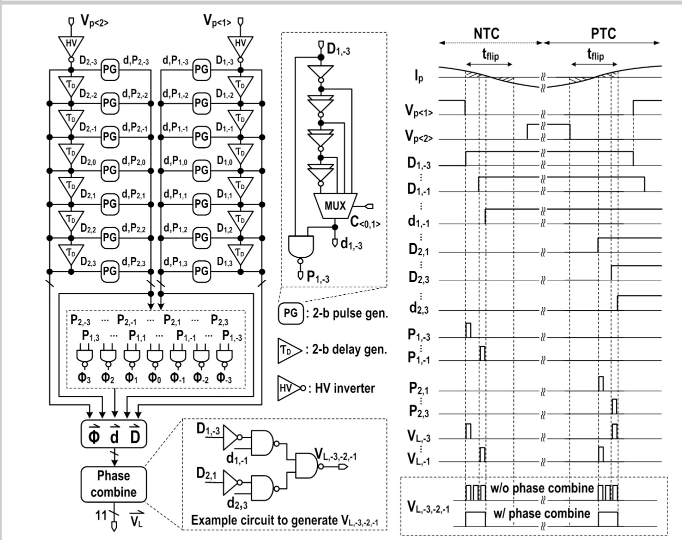

Figure 22.2.4: Phase generator with phase-combining interface and its timing diagram.

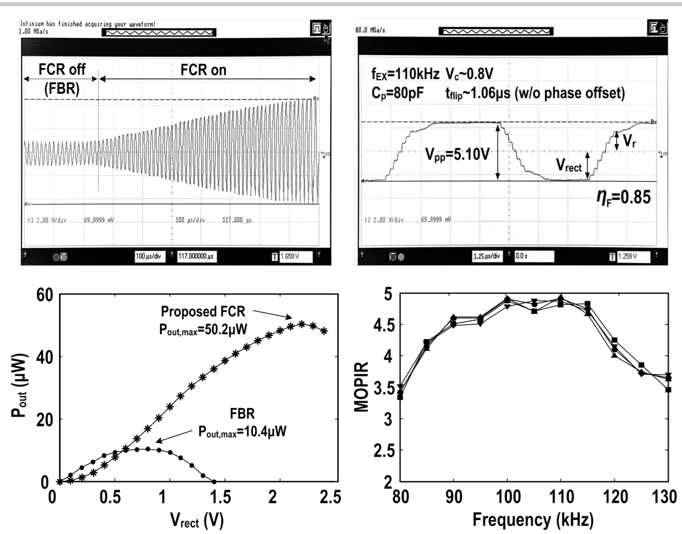

Figure 22.2.5: Measured transient waveforms of the FCR, with its P_{out} compared to on-chip full bridge rectifier, and MOPIR at different excitation frequencies.

	This work	ISSCC'16 [3]	ISSCC'14 [5]	ISSCC'13 [4]	ISSCC'09 [2]
Technology	**0.18 µm**	0.35 µm	0.35 µm	0.35 µm	0.35 µm
Energy Extraction Technique	**Flipping-Capacitor Rectifier**	P-SSHI	Energy Pile-Up	Energy Investment	P-SSHI
Piezoelectric Harvester	**Piezo Systems Inc. (P5A4E @ 5mm^3)**	MIDE V21B & V22B	Emulated (Transformer + RC)	MIDE V22B	MIDE V22B
Key Component	**On-chip MIM Capacitor (C_{total} = 1.44 nF)[a]**	External Inductor (L = 3.3 mH)	External Inductor (L = 10 mH)[b]	External Inductor (L = 330 µH)	External Inductor (L = 47 µH)
Max. Output Power Increasing Rate (MOPIR)	**4.83x 4.78x[c]**	6.81x	4.22x	2.47x	2.8x
Max. Voltage Flipping Eff. (η_F)	**0.85**	0.94	0.77[b]	0.6	0.75[b]
Chip Size	**1.7 mm^2**	0.72 mm^2	5.5 mm^2	2.34 mm^2	4.25 mm^2
Output Power	**50.2 µW**	160.7 µW[d]	87 µW	52 µW	32.5 µW
Operating Freq.	**110 kHz**	225 Hz	100 Hz	147 Hz	225 Hz

[a] Total capacitance for $C_{1\text{-}4}$
[b] Estimated from the corresponding literature
[c] Averaged over 4 measured samples
[d] Off-resonance with 3.35g acceleration

Figure 22.2.6: Performance summary and benchmark with state of the art.

22

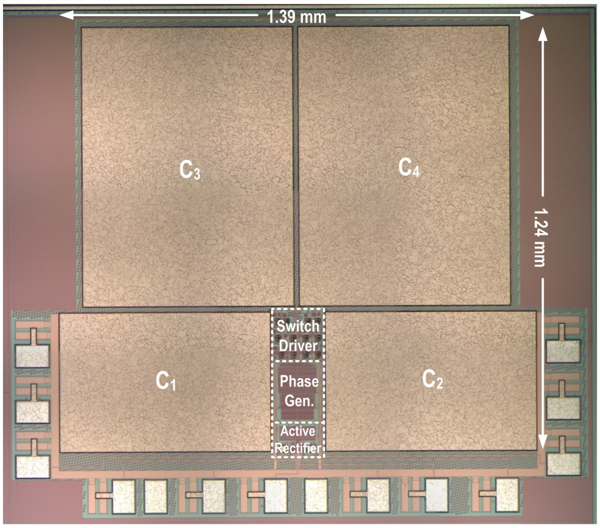

Figure 22.2.7: Die micrograph of the implemented flipping-capacitor rectifier (FCR).

978-1-5090-3758-2/17/$31.00 ©2017 IEEE