9.6 A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration

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The noise-shaping SAR (NS-SAR) hybrid architecture has shown its potential in achieving tens of MHz bandwidth (BW) together with high resolution [1-2]. However, in [1], the performance is debilitated by the passive 1st-order NS, thus limiting the achievable SNDR below 70dB; while with an NS order as high as 4 for SNDR > 70dB based on the interleaving structure [2], power-hungry preamplifiers are essential for residue summation and low-noise targets, which in consequence restricts its Schreier FoM (FoMs) to 166dB. Whereas the 0-1 MASH SDM based on the pipeline-SAR structure retains an FoMs > 170dB [3], the speed of this single-channel ADC is confined by the 1st-stage with the BW of 12.5MHz, and its power-hungry residue amplifier (RA) occupies > 70% of the total ADC power. Besides, its inter-stage offset and gain mismatch are only foreground calibrated, thus suffering from VT variations. Last but not least, it accommodates an area-hungry bit weight calibration to ensure the DAC linearity. In the presented SAR-assisted NS pipeline ADC, a 2-input-pair dynamic amplifier is used for both pipeline operation and error feedback (EF) residue summation, thereby ensuring good power efficiency overall. Besides, a partial interleaving (PI) structure is adopted to relieve the speed constraint from the 1st-stage, which also allows introducing DWA to the PI-DACs without extra timing overhead.

Figure 9.6.1 illustrates the 6+5b SAR-assisted NS pipeline ADC with 1b overlapping between two stages, showing a single-ended circuit only, where the actual implementation is fully differential. Different from the conventional SAR-assisted pipeline ADC, after each conversion the full residue voltage of the 2nd-stage (V_{res2}) is extracted, fed back to the unity-input-pair of the RA and added to the amplified 1st-stage residue voltage (V_{res1}) in the following amplification phase. The summed and amplified voltage is further quantized in the 2nd-stage ADC, thereby the EF NS is realized. In this design, an additional residue feed-forward (FF) path is added in the 2nd-stage, where V_{res2} is quantized together with the input in the next conversion cycle through the 2-input-pair comparator. Despite the fact that the extra input pair of the comparator leads to additional noise, unlike conventional FF NS-SAR ADCs [4], such noise can be suppressed by the inter-stage gain on top of the NS in this design. With such a setup, the NTF of this EF-FF NS structure is $(1-z^{-1})/(1+z^{-1})$, where the FF path introduces a negative pole, leading not only to additional noise suppression at low frequency but also a sharper high-frequency slope of the NTF than the standard 1st-order NTF. Consequently, the presented design allows a small OSR for high BW while maintaining a sufficient NS effect.

Figure 9.6.1 also exhibits the circuit details of the adopted RA [4] with 2-input pair for residue summation. During the 1st-stage sampling (ϕ_s) and conversion phase (Clk_1), ϕ_a is low to disconnect the 1st-stage DAC from the RA input, isolating the interference induced by the variable input capacitance from the RA. Afterward, ϕ_a goes high to perform amplification and EF residue summation simultaneously. The inter-stage gain is selected as 8 to ensure the RA's linearity and a low additional noise from the extra unit input-pair. An attenuation capacitor introduced in the 2nd-stage allows both stages sharing the same reference voltage. To avoid extra time for residue feedback and feed-forward, the attenuation capacitor is further equally split into two capacitors (C_{e1} and C_{f1}), while another two identical capacitors (C_{e2} and C_{f2}) are added for a ping-pong operation. This is controlled by ϕ_{ns}, where C_{e1}/C_{f1} and C_{e2}/C_{f2} are alternatively configured as the loading capacitors of the RA or the residue feedback/feed-forward capacitors, respectively.

The speed of the conventional high-resolution pipeline-SAR structure is often restricted by the 1st-stage, where it has to accomplish the sampling and conversion with a large DAC, as well as a long amplification time for low noise from the RA. In this work, a coarse SAR quantizer with a partial interleaving (PI) technique is utilized to relieve such speed constraints. The decisions of the full-speed coarse SAR ADC are transferred to two time-interleaved (TI) large DACs (LDACs) to originate the 1st-stage residue on LDAC1 and LDAC2 alternatively. Thanks to the PI structure, the LDAC1/2 only needs to complete either the code-transfer and amplification or sampling operations in a single ADC period. It simultaneously extends the available sampling time for the LDACs, thus relaxing the bootstrapped sampling front-end design. Besides, the timing mismatch requirement between the TI clocks (ϕ_{s1} and ϕ_{s2}) is not critical (< 6ps) due to the 40MHz BW target. While the 6b coarse SAR can run fast with a small DAC, the DWA is inserted on the first 3 MSBs of the LDAC during the code-transfer, which induces no additional timing overhead as they are settled together with the remaining 3 LSBs. Since the 3-MSB mismatch error in the LDAC is 1st-order shaped by the DWA, the unit capacitor matching requirement decreases from 0.49% to 0.08%, which in turn eases the DAC area and the PI structure-induced area overhead. Eventually, only a kT/C-limit-sized LDAC is necessary. To correct the gain error of the main input pair in the RA, a dither-based LMS background calibration [5] is adopted, tuning I_{b1} and I_{b2} in the dynamic amplifier. A 1b pseudo-random number (PRN) is injected in the dummy unit capacitor after the first 6b conversion, which ensures a short calibration convergence time by reducing the interference from the input component. The EF unit gain is un-calibrated and the SQNR only degrades by 3dB with a large 25% gain variation.

Figure 9.6.3 presents the concept of the proposed calibration scheme, based on aligning the sign decisions of the residue voltage (V_{res1}) before and after amplification. The sign of the amplified V_{res1} can be directly accessed with D[5], while the sign of V_{res1}, i.e. D_{res}, is acquired by an extra comparison in the 1st-stage coarse SAR ADC that decouples the large DAC operation and allows the amplification processing in parallel. Such a scheme does not require extra phases or a critical input condition; it also has a high activation rate as the input is well randomized with 6b quantization by the 1st stage. When D_{res} = 0 and D[5] = 1 are detected, it indicates an overall positive offset voltage, then a negative calibration voltage (V_{cal}) is fed back to an extra calibration input pair of the 1st-stage comparator to align the inter-stage offset; conversely, V_{cal} becomes more positive when D_{res} = 1 and D[5] = 0. This calibration aligns the inter-stage offset of the 1st (V_{os1}) and 2nd stage (V_{os2}) comparator, as well as the RA ($V_{os,RA}$). A charge pump circuit generates V_{cal} and all the calibration logic is on-chip.

Fabricated in 28nm CMOS, the ADC occupies an active area of 0.016mm^2, including the offset calibration circuit (Fig. 9.6.7). It obtains a 40MHz BW at a 600MHz sampling frequency with an OSR of 7.5. Figure 9.6.4 plots the FFT spectrum of the ADC with -0.5dBFS input at 2MHz. The measured SNDR, SNR and SFDR are 75.2dB, 76.3dB and 87.1dB, respectively, with DWA, offset and gain calibration. It also shows that the SNDR variation is less than 2dB across 5 samples with all calibrations enabled. Figure 9.6.5 shows the SNR/SNDR versus the input amplitude and the ADC power breakdown. The measured dynamic range (DR) is 76.6dB and the ADC consumes 2.56mW from a 1V supply. Figure 9.6.6 summarizes the measured performance of this work and compares it with the state-of-the-art SAR-type NS ADCs with similar bandwidths. The presented ADC achieves an FoM_S of 177.1dB, showing a good energy efficiency with a BW > 10MHz and an SNDR > 70dB.

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[3] Y. Song et al., "A 77dB SNDR 12.5MHz Bandwidth 0-1 MASH ΣΔ ADC Based on the Pipelined-SAR Structure," *IEEE Symp. VLSI Circuits*, pp. 203-204, June 2018.
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[6] Y. Lim, et al., "A Calibration-free 2.3 mW 73.2 dB SNDR 15b 100 MS/s Four-Stage Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC," *IEEE Symp. VLSI Circuits,* pp. C98-C99, June 2017.

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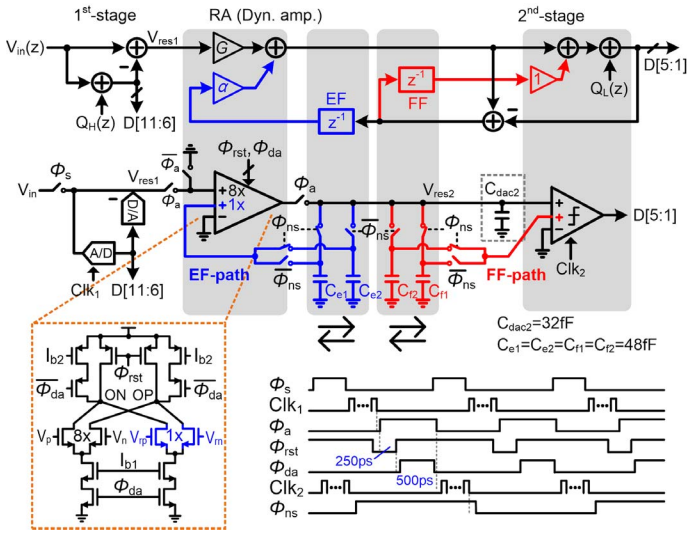

Figure 9.6.1: SAR-assisted NS pipeline ADC with EF-FF NS structure realized by ping-pong capacitors with dynamic-amplifier-based RA.

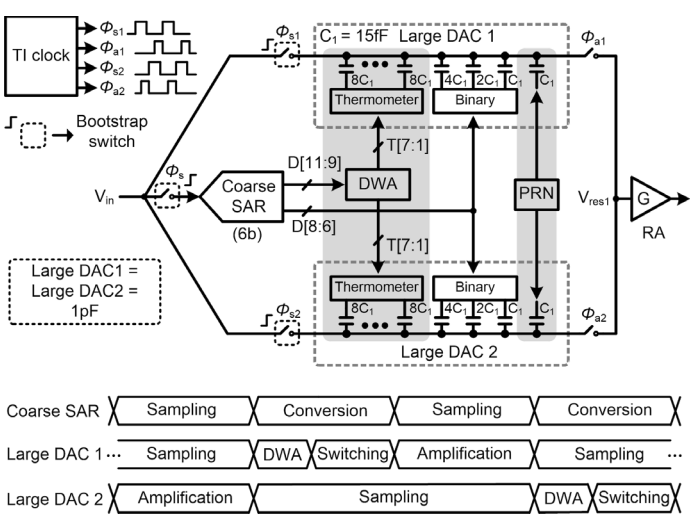

Figure 9.6.2: Block diagram & timing sequence of the 1st-stage SAR ADC with two interleaved large DACs.

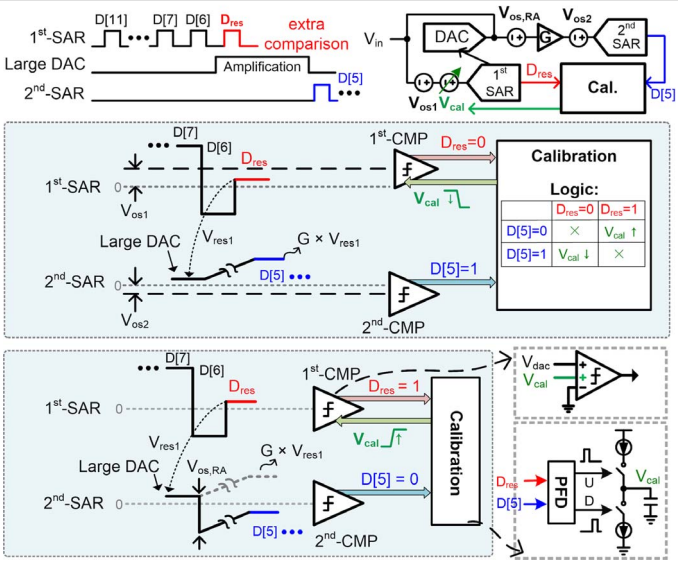

Figure 9.6.3: Proposed offset calibration method.

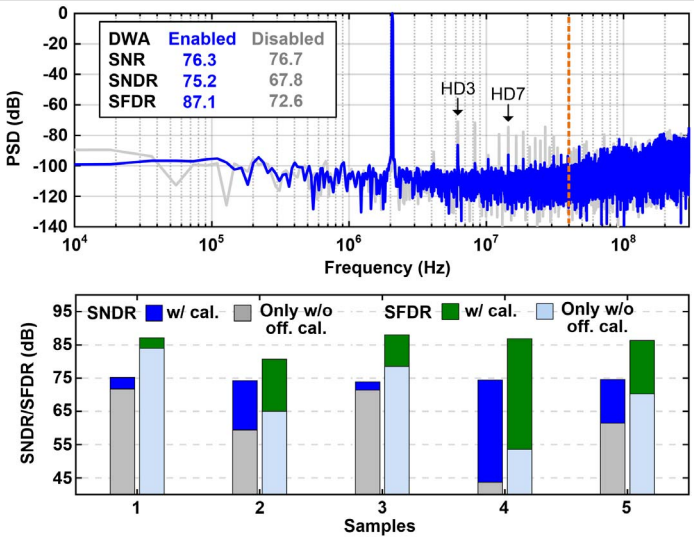

Figure 9.6.4: Measured 32768-point output spectrum at Fin = 2MHz of sample #1 and SNDR/SFDR variation over 5 samples before and after offset calibration.

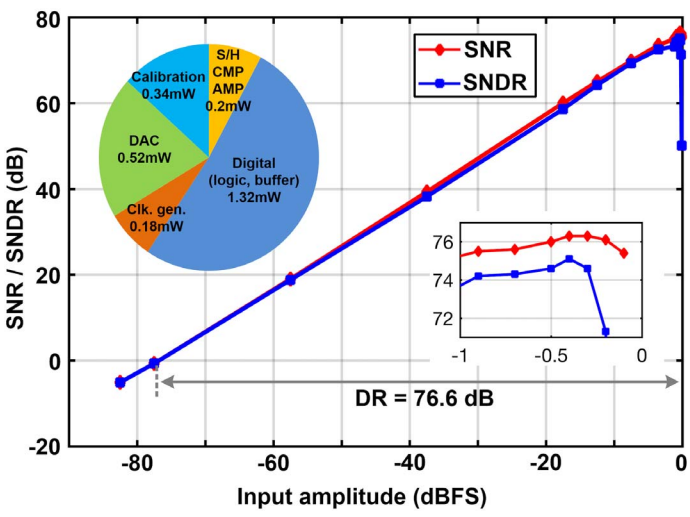

Figure 9.6.5: Measured SNR/SNDR of sample #1 vs. input amplitude and power breakdown.

	ISSCC'19 Lin [1]	ISSCC'19 Jie [2]	VLSI'18 Song [3]	VLSI'17 Lim [6]	This Work
Technology [nm]	14	40	65	40	28
Architecture	PNS SAR	TI NS SAR	NS Pipe-SAR	Pipe-SAR	NS Pipe-SAR
Fs [MHz]	320	400	200	100	600
OSR	4	4	8	1	7.5
BW [MHz]	40	50	12.5	50	40
SNDR [dB]	66.6	70.4	77.1	73.2	75.2
SFDR [dB]	77.4	88	90.7	90.4	87.1
DR [dB]	N/A	71.7	78.5	N/A	76.6
Power [mW]	1.25	13	4.5	2.3	2.56
FoM_W [fJ/step]	8.9	48.1	30.8	6	6.8
FoM_S [dB]	171.7	166.3	171.5	176.6	177.1
Area [mm^2]	0.0021	0.061	0.014	0.068	0.016
Offset calibration	Free	Free	Off-chip	Off-chip	On-chip

Figure 9.6.6: Summary of measurement results and comparison.

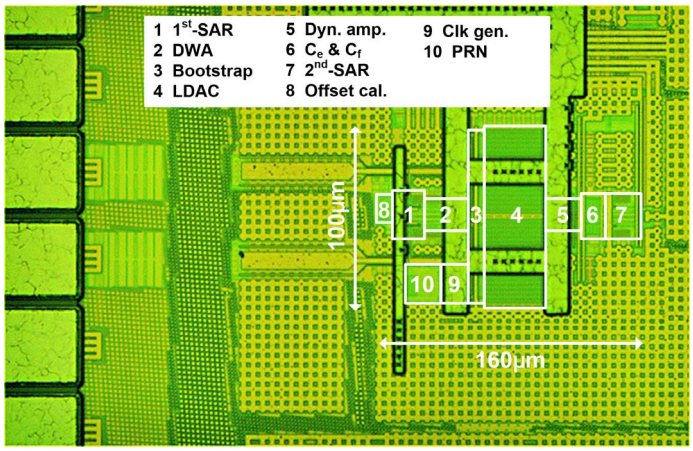

Figure 9.6.7: Chip photo.

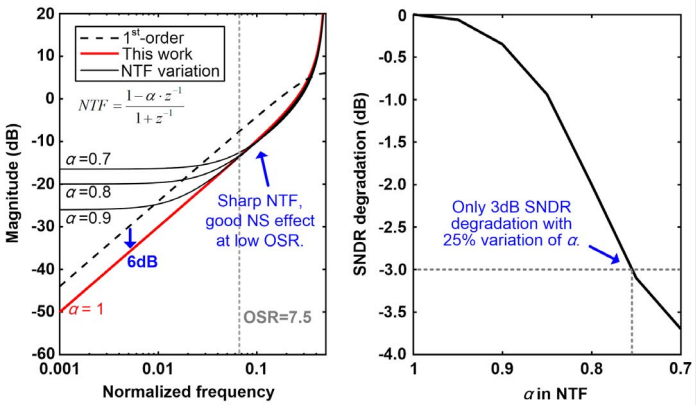

Figure 9.6.S1: Improved NTF in this work for good NS effect at low OSR and SNDR degradation versus EF feedback factor (α) variation.

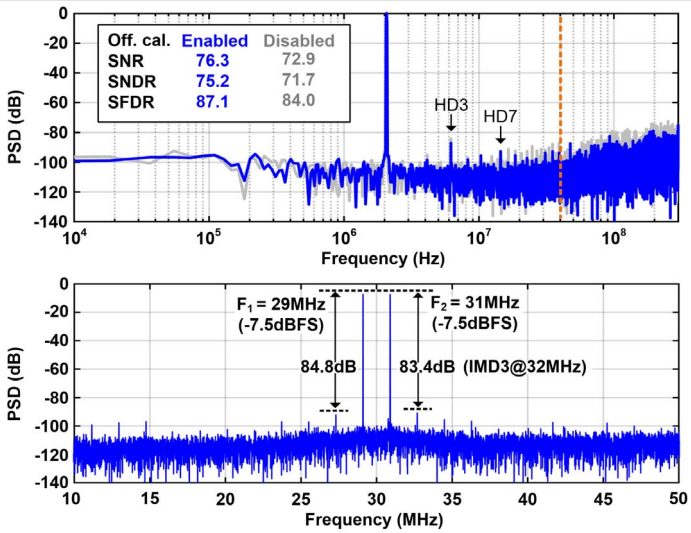

Figure 9.6.S2: Measured output spectrum when only offset calibration is enabled/disabled and two-tone test with all calibrations enabled of sample #1.

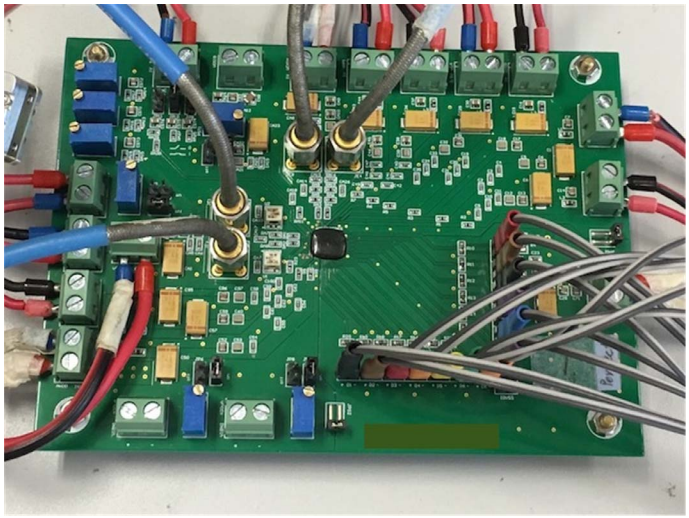

Figure 9.6.S3: Measurement setup.

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