17.9 A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA

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Low-power mm-wave sensors using an FMCW radar technology are opening up unprecedented opportunities in high-resolution object detection (e.g., gesture and breathing). Building a low-power mm-wave LO generator (LOG) fulfilling the stringent phase-noise (PN) requirement of the FMCW transceiver is still challenging [1]. A number of indirect mm-wave LOGs have been explored. As depicted in Fig. 17.9.1, a 20GHz VCO followed by a frequency tripler (×3) effectively lowers the PLL operating frequency by 3 times, benefiting not only the power budget but also the frequency-tuning range. Injection locking [2], harmonic-mixing [3], and voltage-mode implicit frequency tripling [4] are the mainstream ×3 techniques, where the first technique faces the trade-off between locking range and output power, whereas the second and third techniques call for a power-hungry mm-wave mixer or amplifier to recover a large output swing. Finally, all of them suffer from severe subharmonic spurs.

This paper reports a 60GHz current-reuse LOG featuring current-mode implicit frequency tripling. It simultaneously exhibits large output swing, low PN, and low subharmonic spurs without the aid of precise harmonic-frequency alignment as required in [4]. Specifically, our LOG includes: 1) a current-output VCO to generate a large 3rd-harmonic current (I_{D3}) with low PN; 2) an area-efficient passive harmonic-current filter (HCF) using the S-shape inductors to reject the 1st- and 2nd-harmonic leakage currents at f_{LO} (I_{D1}) and $2f_{LO}$ (I_{D2}); and 3) a current-reuse transimpedance amplifier (TIA) stacked atop the VCO and HCF to recover a large output swing with low power. Prototyped in 65nm CMOS, the proposed LOG exhibits a high FoM at a 1MHz offset (184.9 to 186.7dBc/Hz) over a 14.5% tuning range (54.9 to 63.5GHz). The subharmonic spurs are <–61dBc.

For the voltage-mode implicit frequency tripling, a Class-F VCO of the LOG suffers from a severe trade-off between the current ratio I_{D3}/I_{D1} and PN, due to its drain-to-gate (D2G)-feedback topology (Fig. 17.9.2 left). With a constant gate swing (V_G), a large parallel resistance R_P is desired to boost the drain swing (V_D), thereby raising the I_{D3}/I_{D1} ratio. Yet, the $-g_m$ transistor stays longer in the triode region when the V_D swing is large, penalizing the PN contribution of the transconductance G_{DS}, due to the widened triode-region conduction angle ($\theta_{DG2}>\theta_{DG1}$). To avert this, we propose a source-to-gate (S2G)-feedback VCO (Fig. 17.9.2 mid), which has a constant triode-region conduction angle (θ_{SG}) regardless of the V_S swing. For a constant V_G swing, $\theta_{SG}<\theta_{DG}$ can be secured since V_D of the S2G-feedback VCO is fixed (V_{SUP}). As a result, our S2G-feedback VCO improves the I_{D3}/I_{D1} ratio and PN concurrently, when compared with Class-F VCOs.

A differential S2G-feedback VCO (Fig. 17.9.2 mid) can secure the differential-mode (DM) oscillation by magnetic cross-coupling (i.e. V_{S-} to V_{G+} and V_{S+} to V_{G-}) [5]. At 20GHz, a 2-turn secondary coil (L_S=500pH, Q_S=15.7) stacked atop a 1-turn primary coil (L_P=180pH, Q_P=12.5) maximizes the coupling factor (k_m=0.7) of the transformer, which upholds a large loop gain even in the presence of source degeneration. The source capacitor C_P offers another freedom to alternate the R_P seen from the source node when L_P, L_S, and k_m are fixed (Fig. 17.9.2 right). Generally, R_P goes up with C_P if the 1st resonant frequency (f_L) of the transformer tank is fixed at 20GHz. Differing from a Class-F VCO that achieves a large 3rd-harmonic voltage by aligning the 2nd resonant frequency (f_H) of the transformer tank with $3f_{LO}$, the I_{D3}/I_{D1} ratio in the S2G-feedback VCO reaches its minimum when $f_H=3f_{LO}$ (C_P=50fF), since the large tank impedance at $3f_{LO}$ blocks I_{D3}. Thus, we select a large C_P (150fF) to deliver a high I_{D3}/I_{D1} ratio of 0.34. Also, unlike a Class-F VCO that entails two-dimensional capacitor tuning to align f_H with $3f_{LO}$, the PN of the proposed S2G-feedback VCO is insensitive to the variation of f_H, with only a 1dB change when C_P swept from 105 to 195fF (±30%). Thus, varying only the gate capacitor C_S is adequate for frequency tuning. Raising C_P beyond 150fF allows an even higher I_{D3}/I_{D1} ratio and lowers the power consumption, but at the cost of a narrower frequency tuning range since C_S has to be reduced to uphold f_L=20GHz.

Using the linear time-variant model [6], we compare the impulse sensitivity functions (ISF) of the S2G-feedback VCO with a Class-F VCO at the same power budget (4.8mW) and supply (0.6V), as depicted in Fig. 17.9.3 (left). Due to the smaller triode-region conduction angle, the noise-modulating function (α_{GDS}) of our S2G-feedback VCO displays a narrower span than that of a Class-F VCO. The ISF (Γ) of our S2G-feedback VCO is around zero when the $-g_m$ transistor enters into the triode region, which further suppresses the noise contribution from the transistor G_{DS}. Thus, the effective ISF of G_{DS} ($\Gamma_{GDS,eff} = \Gamma \times \alpha_{GDS}$) is much smaller than that of a Class-F VCO, improving the PN and FoM by 3.4dB in simulations.

Figure 17.9.3 (right) details the schematic of our LOG by applying the S2G-feedback VCO. Since the HCF and TIA together provide low impedances for the VCO output currents, the small amplitude of V_D (~70mV) has a negligible effect on θ_{SG}. The TIA reuses the VCO current and recovers a large output swing of $360mV_{pp}$. A 1:1 transformer in the TIA further rejects the subharmonic voltages at the output and facilitates the connection to the following stage in the layout.

Figure 17.9.4 shows the schematic of the HCF. For an ideal situation $k_{1,2}$=0, we design the series LC tank to provide two impedance notches for the DM current I_{D1} at $\omega_{LO} = 1/\sqrt{L_1 (C_C + C_D)}$ and for the common-mode (CM) current I_{D2} at $2\omega_{LO} = 1/\sqrt{L_1 C_C}$. The parallel LC tank also offers an impedance peak at $\omega_{LO} = 1/\sqrt{L_2 C_2}$ to further suppress the fundamental current. We nest the 4 inductors together to save the die area and design $L_{a,b}$ in the S-shape to minimize the magnetic coupling ($k_{1,2}$) between $L_{a,b}$ and $L_{c,d}$ (Fig. 17.9.4 lower). Since the currents i_{ac1} (i_{bc1}) and i_{ac2} (i_{bc2}) induced by the current i_a (i_b) in L_a (L_b) tend to cancel each other, k_1 (k_2) is kept small in both DM and CM. If $k_1 \neq k_2$, the strong I_{D1} in L_a and L_b leaks to L_c (L_d) through magnetic coupling. Fortunately, using the S-shape inductors ensures $k_1=k_2$ (=0.05) since the amplitude of the induced currents i_{ac1} (i_{ac2}) and i_{bc1} (i_{bc2}) are ideally the same due to the symmetric layout. $L_{a,b}$ and $L_{c,d}$ are implemented in different metal layers (M9 and AP) to reduce coupling due to interwinding capacitors. EM- simulations verify that the current densities along the traces of L_c are all roughly zero when a differential input is excited between the ports T_1 and T_2. The HCF effectively rejects I_{D1} by 30.5dB and I_{D2} by 28.8dB. Together with the rejection provided by the TIA, the LOG output exhibits low 1st- and 2nd-subharmonic spurs of –49.1 and –47dBc, respectively, in simulations.

The LOG in 65nm CMOS (Fig. 17.9.7) occupies $0.12mm^2$ and dissipates 9mW. Figure 17.9.5 plots the measured PN profile at 59.8GHz. The PN is –100.7dBc/Hz at a 1MHz offset and the $1/f^3$ PN corner is ~580kHz. The $FoM_{@1MHz}$ varies by 1.8dB and peaks to 186.7dBc/Hz over a 14.5% tuning range from 54.9 to 63.5GHz. The DC isolation between V_{DD} and V_{B1} benefits the frequency pushing, which is 270MHz/V at 54.9GHz and 340MHz/V at 63.5GHz. Multi-chip measurements (5 samples) show <2dB variation of $FoM_{@1MHz}$. The 1st- and 2nd-subharmonic spurs measure <–61dBc, of which ~15dB is due to the test buffer.

Figure 17.9.6 benchmarks this work with the recent mm-wave LOGs in CMOS [4,7,9] and BiCMOS [8]. Comparing with [4,7] that entail a buffer stage to boost the 3rd-harmonic voltage while suppressing the large fundamental voltage at the Class-F VCO output, this work consumes less power and shows improved $FoM_{@1MHz}$ by >5.2dB, and subharmonic spurs by 10dB. Comparing with [8] that relies on quad-core coupling, our LOG reveals a comparable $FoM_{@1MHz}$ at a 5× smaller die area.

Acknowledgement:
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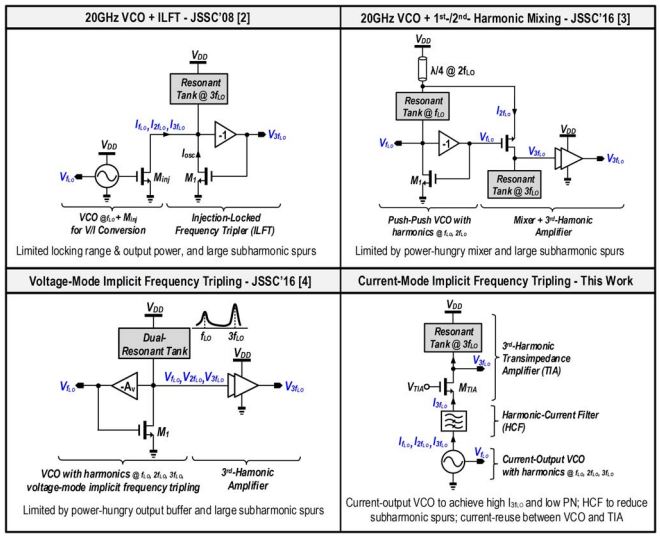

Figure 17.9.1: Basic topologies of the indirect 60GHz LOGs in [2-4] and this work.

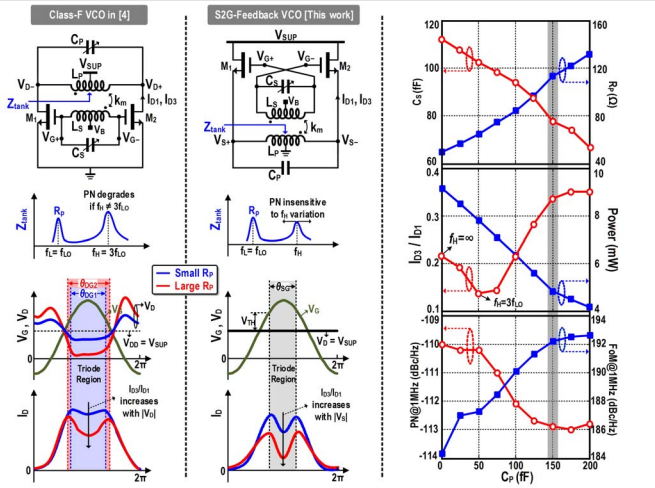

Figure 17.9.2: Class-F VCO (*Left*) and S2G-feedback VCO (*Mid*). The latter features a smaller triode-region conduction angle when generating a large I_{D3}/I_{D1} at a constant V_G swing, lowering the PN. *Right:* Performance metrics versus C_P in S2G-feedback VCO at 20GHz.

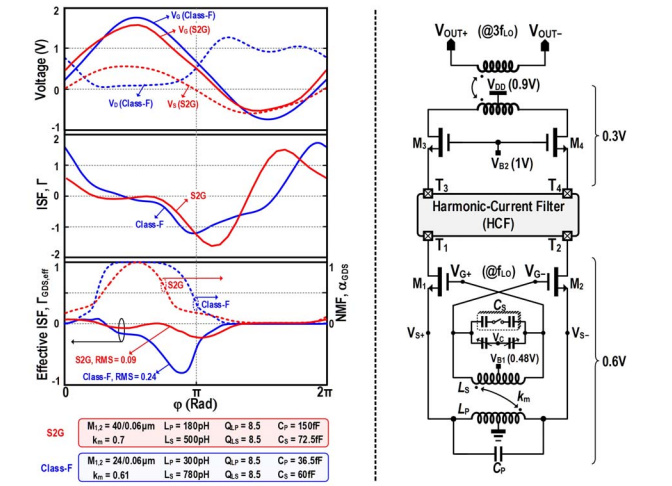

Figure 17.9.3: *Left*: The S2G-feedback VCO shows a much smaller effective ISF of transistor G_{DS} compared with the Class-F VCO, yielding 3.4dB better PN and FoM at the same power budget. *Right*: Applying the S2G-feedback VCO into the proposed LOG.

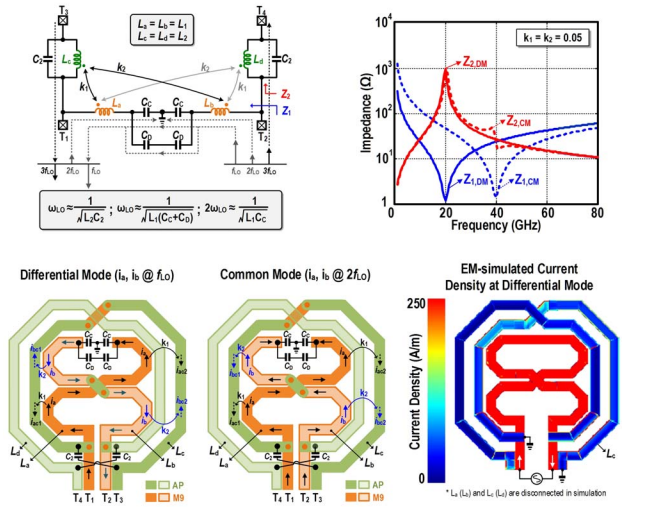

Figure 17.9.4: Proposed compact passive HCF. The S-shape inductors ($L_{a,b}$) ensure small $k_{1,2}$ (0.05) to avoid the 1st-/2nd-harmonic current leakages to $L_{c,d}$ via magnetic coupling.

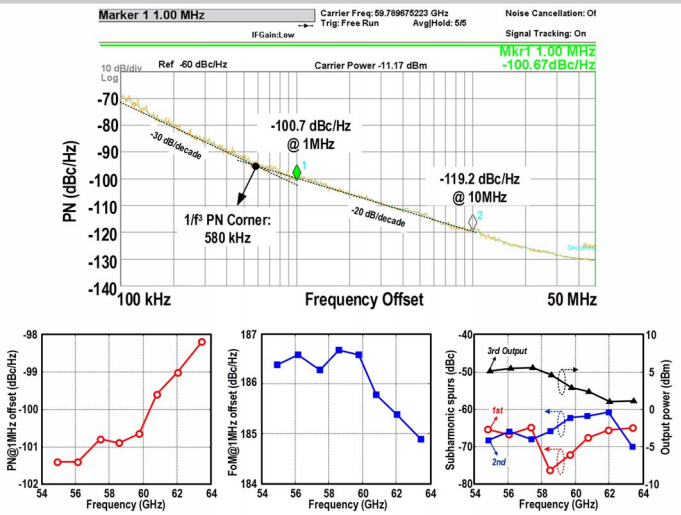

Figure 17.9.5: *Upper*: Measured PN profile at 59.8GHz. *Lower*: Measured PN, FoM, output at 3rd harmonic, and 1st-/2nd-subharmonic spurs against the output frequency.

		This Work	JSSC'16 [4]	JSSC'19 [7]	JSSC'17 [8]	ISSCC'15 [9]
Key Technique		**Current-Output VCO + HCF + Current-Reuse TIA**	Class-F VCO + Implicit Freq. Tripling	Class-F DCO + Implicit Freq. Tripling	Quad-Core coupled VCO w/ tail filter + Freq. Quadrupler	Mixer-based ILFT
Technology		65nm CMOS	40nm CMOS	28nm CMOS	55nm BiCMOS	65nm CMOS
Tuning Range (TR) (F_{min} to F_{max} GHz)		14.5% (54.9 to 63.5)	25.4% (48.4 to 62.5)	15.6% (57.5 to 67.2)	15% (70 to 81.4)	19.2% (70.5 to 85.5)
Supply Voltage (V)		0.9	0.7/1	0.9	1.2	1.2/1
Power P_{DC} (mW)		9	24&	29.5&	50	47.3
Output Frequency f_0 (GHz)		59.8	57.8	66.9	80	73
Eq. PN# at 60GHz (dBc/Hz)	@1MHz Δf	**−100.7**	−99.8	−98.9	−109	−96.4
	@10MHz Δf	**−119.2**	−121.9	−118.4	N/A	−118.5
FoM (dBc/Hz)	@1MHz Δf	**186.7**	181.5	179.8	187.5	175.2
	@10MHz Δf	**185.2**	183.7	179.3	N/A	177.4
Maximum Subharmonic Spurs (dBc)	1st	**−65**	−51	−51	N/A	N/A
	2nd	**−61**	−45	−44		
1/f³ PN Corner (kHz)		580	920	350	1000†	N/A
Die Area (mm^2)		0.12	0.13	0.11*	0.6	0.12*

FoM = − PN + $20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{DC}/1mW)$ # Eq. PN = PN + $20\log(60GHz / f_0)$ † Estimated from the PN plot
& Including the power of the first buffer stage for harmonic extraction * Estimated from the chip photo

Figure 17.9.6: Performance benchmark with the prior-art 60GHz LOGs.

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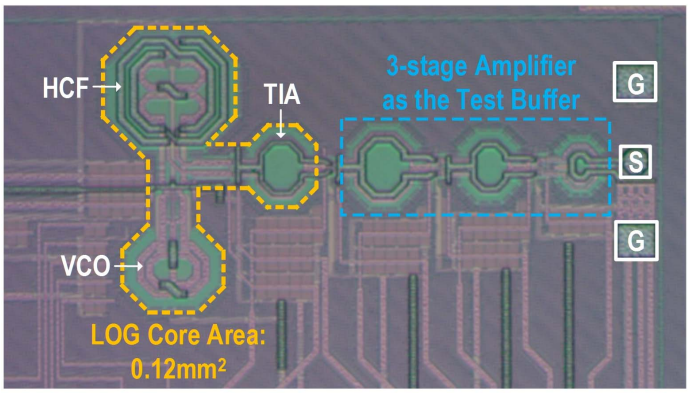

Figure 17.9.7: Die micrograph of the fabricated 60GHz LOG in 65nm CMOS. An on-chip 3-stage amplifier serves as the test buffer.

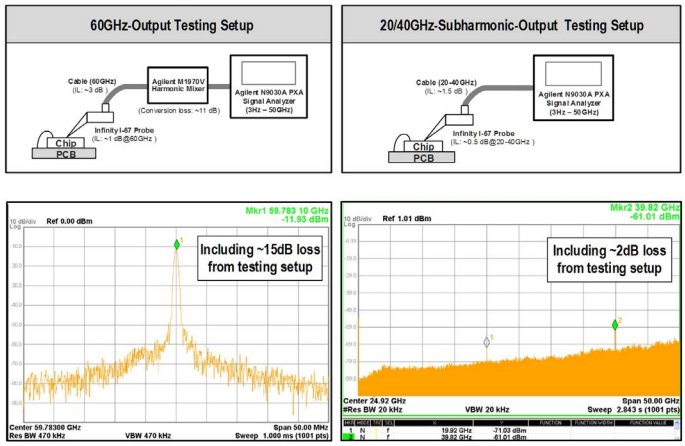

Figure 17.9.S1: *Upper*: Testing setups for the 60GHz and subharmonic outputs. *Lower*: Measured output spectrum at 60GHz and subharmonic spurs. The loss-de-embedded 1st-subharmonic spur is −72.1dBc and 2nd-subharmonic spur is −62.1dBc.

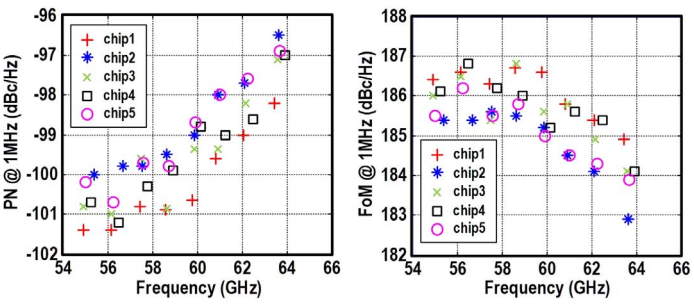

Figure 17.9.S2: Measured PN (left) and FoM (right) variations are <2dB among 5 samples.

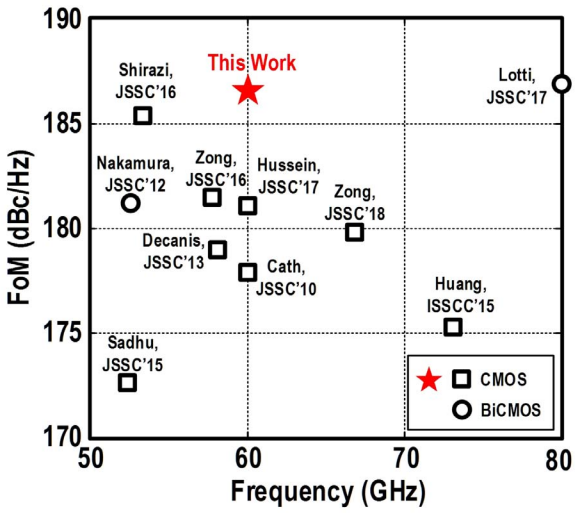

Figure 17.9.S3: Benchmark with the recent VCOs and LOGs in the 50-to-80GHz range.

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