20.5 A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH ΔΣ Modulator with 1.5b/4b Quantizers in 28nm CMOS

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The demands for wider cellular bandwidth (BW) drive the development of continuous time (CT) ΔΣ modulators (DSMs). Oversampling ratio (OSR) is generally restricted due to high signal BW. To obtain an adequate resolution while maintaining good power efficiency, CT DSMs generally need to achieve an aggressive noise shaping and employ a multibit quantizer (QTZ) [1-3]. Though multibit operation requires a highly linear feedback (FB) DAC, dictating sophisticated linearization techniques [1-3]. Multi-stage noise-shaping (MASH) topologies can be employed to increase the order and they can apply multibit quantization only in the latter stages, where linearity requirements are highly relaxed. However, MASH DSMs suffer from quantization noise (QN) leakage due to the mismatch between analog and digital filters.

The sturdy MASH (SMASH) topology has relaxed matching requirements to eliminate the QN leakage. Reference [1] has first realized the CT SMASH using multibit QTZs in both stages. Inevitably, the multibit DAC FB from the QTZ of the 1st stage poses the same nonlinearity issue as in single-loop designs. On the other hand, the use of inherently linear single-bit 1st stage combined with multibit 2nd stage in SMASH is much more critical than in a MASH DSM. This occurs because single-bit QN is highly tonal and – in SMASH – the output of the 2nd stage is fed back to the sensitive input of the 1st stage. Moreover, the extraction and cancellation of the QN from the 1st stage is still challenging due to delays and phase shifts in the CT SMASH.

To explore a more robust CT SMASH topology and circumvent the use of linearization techniques for a multibit DAC, this work presents a noise-coupling-assisted CT SMASH DSM employing 1.5b/4b QTZs in the 1st/2nd stages. By effectively eliminating 1.5b QN of the 1st stage, this topology enjoys the benefits of multibit DAC FB. The noise coupling (NC) technique [4] not only increases the noise-shaping order by one, but also significantly mitigates the linearity requirement of the multibit DAC in the input front end. This SMASH renders the 4th-order 1.5b 1st stage effectively into an overall 4th-order multibit DSM without needing a highly linear DAC, thus achieving aggressive multibit QN shaping and large maximum stable amplitude (MSA) without employing area- or power-hungry DAC linearization techniques.

Figure 20.5.1 presents the block diagram of the SMASH DSM. It employs a 3-0 dual-stage architecture with 1.5b/4b QTZs in the 1st/2nd stages. The output of the 2nd stage is directly fed back into the 1st stage through DAC_2 without using a digital adder [1]. A 1st-order NC is applied in the 1st stage to increase the noise-shaping order, while a digital filter $(1-z^{-1})$ is correspondingly placed at the output branch of the 2nd stage. The digital outputs of two stages, V_1 and V_2, are combined off-chip to generate the final output V_{out}. Thereby, the overall output becomes

$$V_{out}=STF_1*V_{in}+NTF_1*(1-z^{-1})*(1-STF_2)*E_{q1} - NTF_1*(1-z^{-1})*E_{q2}$$

where NTF_1 is the noise transfer function (NTF) generated by the loop filter $H_{LF}(s)$. Instead of using the 1st-order feedforward (FF) topology as in [1], this work chooses zero-order for the 2nd stage to implement a more accurate and robust unity-gain signal transfer function (STF_2). Thereby, the 1.5b QN E_{q1} can be more precisely eliminated compared to [1]. To obtain SQNR>85dB, the gain error of the NC path should stay within ±5%, which can be reliably achieved by implementing it using a switched-capacitor (SC) circuit. Another beneficial feature of the NC branch in the 1st stage is that it works as dithering, significantly reducing idle tones and harmonic spurs for 1.5b QN E_{q1} [4]. Furthermore, before the output of the 2nd stage is fed back into the front end, it is shaped by the digital filter $(1-z^{-1})$, thus reducing the in-band tone power. Consequently, both features significantly mitigate the linearity requirement of the outermost 4b DAC_2.

However, with the presence of 4b DAC_2 mismatch and non-linearity, the in-band noise floor still gets increased due to the QN-folding generated by the out-of-band cross-modulation, thus degrading the SNR. To mitigate this, a 2-tap FIR filter $(1+z^{-1})/2$ is adopted to reduce the out-of-band QN from the 2nd stage, which is eventually combined with the $(1-z^{-1})$ filter due to NC to result in $(1-z^{-2})/2$, without requiring additional hardware. To implement $(1-z^{-2})/2$, a tri-level encoder is employed, followed by a tri-level DAC. Moreover, the FIR filter reduces the jitter sensitivity of the outermost DACs.

Figure 20.5.2 presents a simplified schematic of the CT SMASH DSM, using the NRZ tri-level scheme for all DACs. The loop filter $H_{LF}(s)$ employs a 3rd-order mixed FF/FB architecture with H_{inf}=2.3. This mixed mode separates the high-gain and high-speed requirements into different integrators, allowing better op-amp power efficiency. A local resonator improves the NTF, and the input FF path reduces the swing of the internal nodes. A simple FIR compensation filter Fc(z) – incorporated in the inner FB paths – restores the original NTF from the introduced FIR filter in the outermost FB. In [1], to correctly extract E_{q1}, an RC low-pass filter is used to generate a propagation delay for the continuous input of the 1st QTZ, thus matching the delay of the 1st QTZ. However, this is sensitive to the PVT variations. To circumvent this issue, E_{q1} is extracted using an SC array [2] integrated in the 1.5b QTZ_1. After correct extraction, E_{q1} passes an SC buffer, and injects back into the 3rd integrator to facilitate the 1st-order NC. Meanwhile, the output of the SC buffer directly drives the QTZ of the 2nd stage.

Figure 20.5.3 depicts the detailed 1st-order NC implementation and excess loop delay (ELD) compensation incorporated in the 1.5b QTZ_1. During the n^{th} sampling phase, the bottom plates of the DAC capacitors C_{DAC1} and C_{DAC2} connect to the digital outputs V_1 and $V_2(1-z^{-1})$ from the previous cycle, while their top plates sample the output of the 3rd integrator. After that, by connecting the bottom plates to V_{CM}, the input node of the 1.5b QTZ_1 settles to $V_{Int3}-(V_1-V_2(1-z^{-1}))*z^{-1}*V_{Ref}$. Thereby, a negative FB path with a nominal unity gain is generated around the 1.5b QTZ_1, stabilizing the DSM with the 0.75*Ts ELD [5]. Since this ELD compensation (ELDC) method cannot help to reduce the swing of the last integrator, a scaling factor of 1/4 is applied in the 3rd integrator, reducing the swing as well as enhancing the feedback factor. To maintain the original NTF, the references of the 1.5b QTZ_1 are scaled down by a factor of 4, correspondingly. After the decision of the 1.5b QTZ_1, the digital codes V_1<1:0> are fed back to C_{DAC1} to produce the current residue E_{q1}. Setting the values of $C_{DAC1}=C_{res}$ and $C_{DAC2}=2*C_{res}$, the residue is correctly scaled as $E_{q1}/4$, and subsequently sampled by two capacitors C_{res} alternately [2]. Next, the residue charge is injected back to the 3rd integrator through a unity-gain SC buffer in a closed-loop operation. Thereby, a complete 1st-order NC path consists of the SC buffer and the summer formed by the 3rd integrator.

The prototype is fabricated in 28nm CMOS. Clocked at 1.2GHz, Fig. 20.5.4 shows the spectrum with a 6MHz, -1.6dBFS input signal. The measured SNDR/SFDR/DR are 76.6dB/87.9dB/80dB, respectively. The measured IMD3 is -84.6dBc/-82.5dBc with two -7.6dBFS inputs at 33.5MHz/36.5MHz. The MSA is around -1dBFS, which clearly shows the overall multibit operation of the SMASH DSM. With 1.2V/1.5V supply, the total power consumption is 29.2mW. Its breakdown is shown in Fig. 20.5.5. The achieved FOM_S is 168.9dB. Figure 20.5.6 compares the design to wideband CT DSMs. This work achieves state-of-the-art FOM with high linearity without employing any DAC linearization technique, thereby consuming an area of 0.085mm^2. Figure 20.5.7 shows the chip micrograph.

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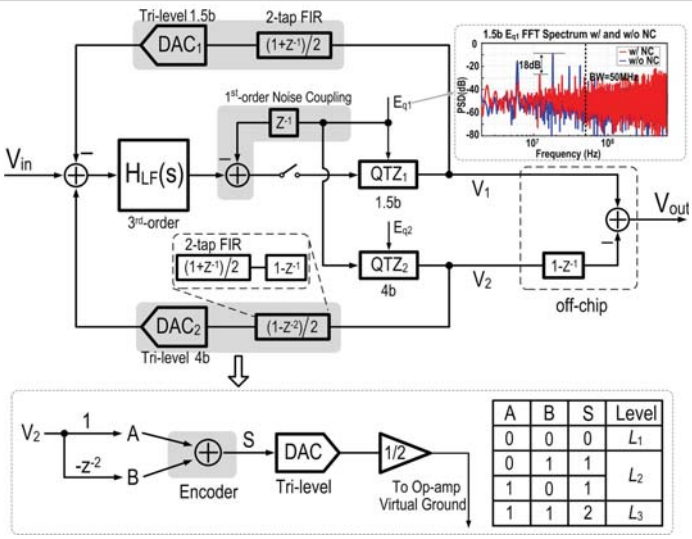

Figure 20.5.1: Block diagram of the CT SMASH DSM with illustration of the tri-level DACs.

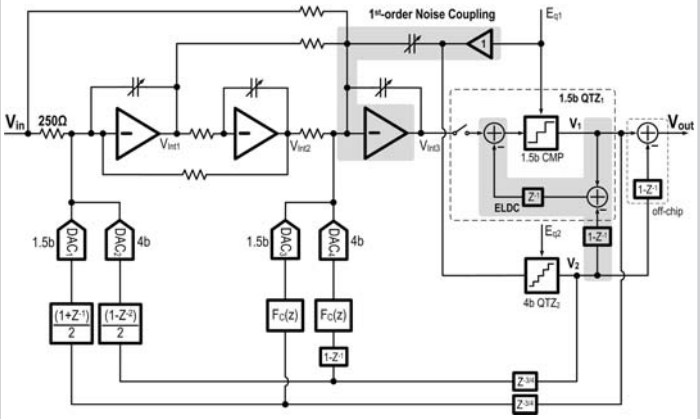

Figure 20.5.2: Simplified schematic of the CT SMASH DSM.

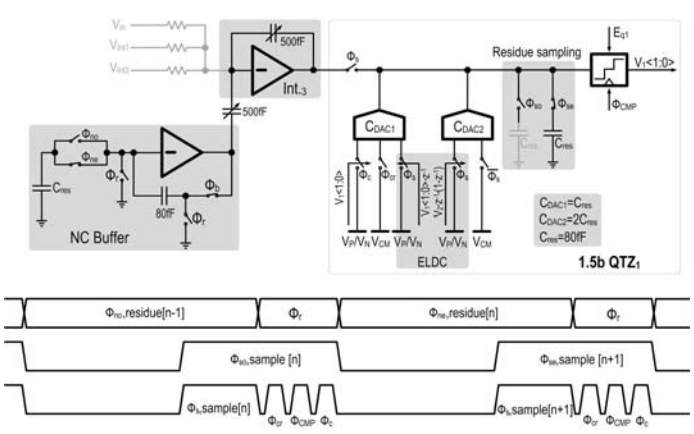

Figure 20.5.3: The 1st-order NC implementation and the ELDC incorporated in 1.5b QTZ$_1$ with the corresponding timing diagram.

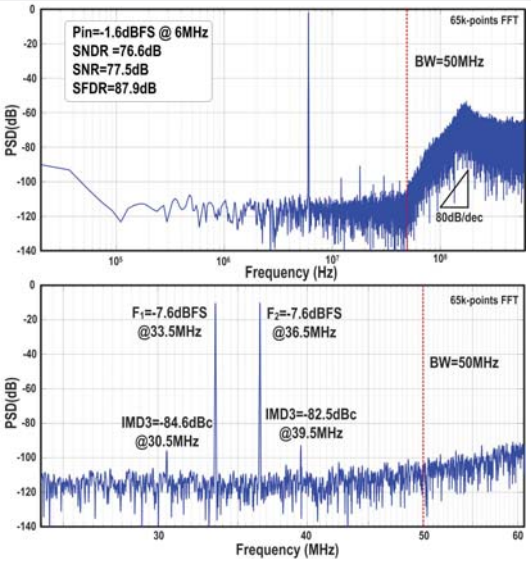

Figure 20.5.4: Measured spectrum of the CT SMASH DSM output and IMD3.

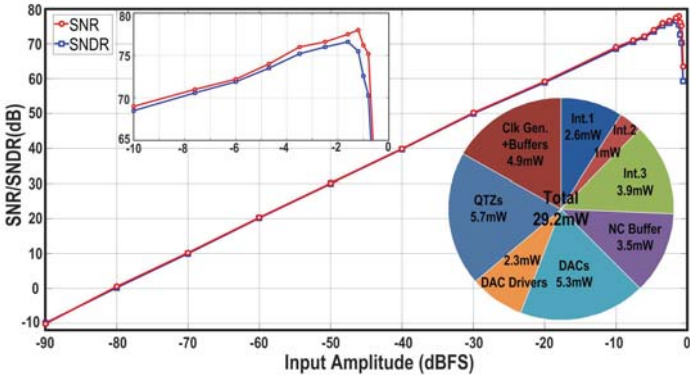

Figure 20.5.5: Measured SNR/SNDR vs. input amplitude and the power breakdown.

	This Work	ISSCC'18 He [3]	ISSCC'17 Huang	ISSCC'16 Wu [2]	ISSCC'15 Yoon [1]	VLSI'15 Loeda
Architecture	SMASH 4th-order 1.5b/4b	Single-loop 4th-order 4b	Single-loop 4th-order 7b	Single-loop 6th-order 4b	SMASH 4th-order 4b/4b	Single-loop 4th-order 1b
Process (nm)	28	28	16	65	28	40
Fs (GHz)	1.2	2	2.15	0.9	1.8	2.4
BW (MHz)	50	50	125	45	50	40
SNDR (dB)	76.6	79.8	71.9	75.3	74.6	66.9
SNR (dB)	77.5	80.0	72.6	78.5	76.1	N/A
DR (dB)	80.0	82.8	74.8	82.5	85	67.8
SFDR (dB)	87.9	95.2	N/A	83	89.3	N/A
THD (dBc)	-83.9	-94.1	-80	-78.1*	-79.9*	N/A
Supply (V)	1.2/1.5	1.16/1.5	1/1.35/1.5	1.2/1.8	1.2/1.5	N/A
Power (mW)	29.2	64.3	54	24.7	78	5.25
Area (mm^2)	0.085	0.25	0.217	0.16	0.34	0.02
DAC Calibration	Without	With on-chip	With on-chip	With off-chip	With on-chip	Without
FOM$_W$ (fJ/conv.-step)	52.8	80.5	67.2	57.7	177.7	36.3
FOM$_S$ (dB)	168.9	168.7	165.5	167.9	162.7	165.7

FOM$_W$=P/(2*BW*2^(SNDR-1.76/6.02)) FOM$_S$=SNDR+10*log$_{10}$(BW/P)

*THD calculated based on the difference between SNRs and SNDRs reported

Figure 20.5.6: Performance summary and comparison with the state-of-the-art wideband CT DSMs.

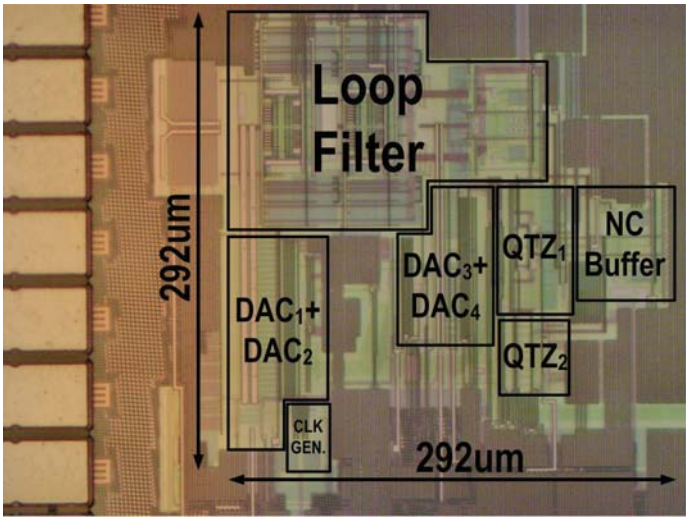

Figure 20.5.7: Chip micrograph.

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