17.2 A 0.0013mm² 3.6µW Nested-Current-Mirror Single-Stage Amplifier Driving 0.15-to-15nF Capacitive Loads with >62° Phase Margin

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For active-matrix LCDs [1] that have thousands of buffer amplifiers integrated in its column-driver ICs, ultra-low power and area circuit solutions are continuously urged to meet the market pressure on cost, image quality and display size. Multi-stage amplifiers have dominated those buffers due to their reliable DC gain, output swing, gain-bandwidth product (GBW) and slew rate (SR). Yet, different kinds of frequency compensation are also useful for stability, bottlenecking the capacitive-load (C_L) drivability, power and area efficiencies.

Classical single-stage amplifiers were underused in those buffers due to their limited capability in most metrics despite being almost unconditionally stable at any C_L and tiny in size. In view of this, it is beneficial to revisit the fundamental limits of single-stage amplifiers and deal with them differently. This paper introduces a nested-current-mirror (NCM) single-stage amplifier to advance its GBW-to-power/area efficiency and C_L drivability beyond the multi-stage designs, while preserving a rail-to-rail output swing. The fabricated NCM amplifier demonstrates 33× higher GBW and 47dB higher DC gain than those of a typical differential-pair (DP) amplifier at equal power and area. By benchmarking with the recent three-stage amplifiers [2]-[4], this work improves FOM_1 [=GBW·C_L/(Power·Area)] by >6.6×, and upholds a comparable FOM_2 [=SR·C_L/(Power·Area)]. The C_L drivability is >10× wider than [2]-[4], while avoiding the stability limit at the heavy-C_L side. These results justify advanced single-stage amplifiers as a potential replacement for multi-stage designs in traditional (e.g. 100pF/m coaxial cable) and advanced (e.g. low temperature polysilicon LCD) buffer interfaces.

Most single-stage amplifiers suffer from a tight tradeoff between power and performance. Telescopic amplifiers feature a GBW-to-power efficiency as high as that of the DP amplifier (Fig. 17.2.1), but sacrifice output swing. Folded-cascode amplifiers partially surmount such a limit, but at the expense of power. For LCD column drivers, current-mirror amplifiers are favored for their rail-to-rail output swing, and extra design flexibility via adjusting the mirror ratio, K. A large K benefits most metrics (i.e., effective transconductance ($G_{m,eff}$), GBW and SR), but at the expense of noise and phase margin (PM). Yet, no matter how large K is, most metrics of the current-mirror amplifier still lag behind those of the DP amplifier.

The basic principle of the NCM amplifier (Fig. 17.2.1) is to subdivide a current mirror into a number of pieces with different ratios, and sequentially combine their outputs to concurrently advance $G_{m,eff}$ and output resistance (R_{out}) beyond those of the DP and current-mirror amplifiers. Specifically, by sharing the current I_{b2} (for the left-half side) with N divided differential-input transistors [(I_1, M_1),(I_2, M_2)…(I_N, M_N)], their outputs can be combined via N nested current mirrors with ratios [(1:K_1),(1:K_2)…(1:K_N)]. Since M_1-M_N are located in the signal path, all of their transconductances, which contribute to $G_{m,eff}$, are multiplied and customizable via choosing K_1 to K_N. To achieve high DC gain and GBW, more mirror stages and bigger ratios are preferred. To lower the noise, the largest amount of current can be allocated to the 1st mirror with a small K_1. To enhance SR, most of the current can be assigned to the 2nd-last mirror with enlarged K_{N-1} and K_N. Indeed, the mirror stages and ratios are only limited by the PM and transistor mismatches. If a large C_L is imposed, PM is no longer the stability constraint. Any mismatches generate a voltage offset. Upsizing W and L of the DP amplifier transistors and mirrors improves matching and intrinsic gain. Both are important to the expected values of $G_{m,eff}$ and R_{out}. Along such a NCM process, R_{out} is improved as well since less current goes to the output stage. Thus, the DC gain can be as high as that of a folded-cascode amplifier, but without the output swing penalty. Moreover, unlike the folded-cascode and current-mirror amplifiers, cutting the current of the output stage does not essentially degrade SR. In fact, as long as $K_N I_N > I_{b2}$, the SR of the NCM can still outperform that of the DP amplifier.

This work implements a 4-step NCM amplifier (Fig. 17.2.2) with the sub mirror ratios used for design flexibility. The total bias current (3µA) is divided into 60 unit currents (I_u=50nA). On the right-half side, the DP amplifier transistors are split into M_1-M_4. Their outputs are summed via the mirrors realized by M_5-M_{12}. M_{13} collects the output of the left-half, to form the single-ended output with M_{12}. The analytical equations in Fig. 17.2.2 show how the mirror ratios K_1 to K_7 contribute to each performance metric. The DC gain is mainly given by $2K_2K_4K_6/(K_3K_5)$. This, together with K_7, roughly defines the GBW. Large $K_{6,7}$ is set to enhance SR. The noise is a tradeoff under small K_1 (and large K_2/K_1), as the transistor's noise is also amplified by the mirror ratios. To leverage them, the 1st mirror M_5-M_6 uses a moderate ratio of 3 (K_1=2 and K_2=6). The 2nd mirror M_7-M_8 draws less current under a larger ratio of 4 (K_3=1 and K_4=4) to boost the DC gain and GBW, as they contribute negligible noise. The 3rd mirror M_9-M_{10} also uses a ratio of 4 (K_5=2 and K_6=8), but the given current is doubled to enhance SR. The 4th mirror M_{11}-M_{12} is given the largest ratio (K_7=6) to benefit the SR and $G_{m,eff}$. Overall, the DC gain, GBW and SR are theoretically improved by 47.6dB, 48× and 1.8×, respectively, when compared to the DP amplifier. Though the noise voltage of NCM amplifier is 1.8× higher than that of the DP amplifier, it is still 1.44× better than that of the current-mirror amplifier under K=6 (equivalent to K_7 in Fig. 17.2.2).

The multipath feedforward nature of NCM creates three left-half-plane (LHP) zeros, ω_{z1} to ω_{z3}, reducing the negative phase shift caused by the four non-dominant poles ω_{p2} to ω_{p5} (Fig. 17.2.3). Since ω_{p2}-ω_{p5} and ω_{z1}-ω_{z3} are all beyond the unity-gain frequency, ω_u, the stability is unconditional during startup, large transients or saturation recovery. This fact differentiates it from explicit multipath feedforward compensation [5] that consumes extra power and is conditionally stable. Here, the stability is bounded by the light-C_L condition.

The NCM and DP amplifiers are fabricated in 0.18µm CMOS for comparison at equal power and area. Their measured AC and small-step responses are plotted in Fig. 17.2.4. The NCM shows 0.013-to-1.24MHz GBW, linearly scalable with C_L from 15 to 0.15nF, which are >33× higher than those of the DP amplifier. The extrapolated DC gain (84dB) of the NCM amplifier also compares favorably with that (37dB) of the DP amplifier. The stability of the NCM amplifier is limited at the light-C_L side (62.4° PM at 0.15nF C_L). The large-step responses are plotted in Fig. 17.2.5. The chip summary and photos are given in Fig. 17.2.6. The NCM amplifier has better overall FOM_1 (>33×) and FOM_2 (>1.8×).

Comparing with the recent three-stage amplifiers of Fig. 17.2.7, this work shows the highest FOM_1 (>6.6×), widest C_L drivability (>10×) and better stability (PM>62°). Before adopting any dynamic-biasing SR-enhancement technique [6], FOM_2 is still 2.2× higher than [2], but 1.2 to 1.47× lower than [3], [4].

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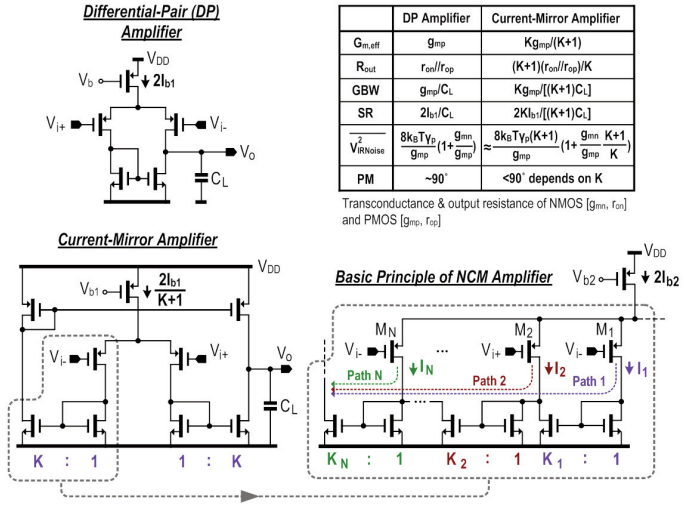
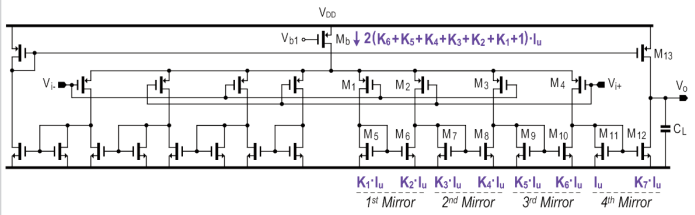


	DP Amplifier	Current-Mirror Amplifier
$G_{m,eff}$	g_{mp}	$Kg_{mp}/(K+1)$
R_{out}	$r_{on}/\!/r_{op}$	$(K+1)(r_{on}/\!/r_{op})/K$
GBW	g_{mp}/C_L	$Kg_{mp}/[(K+1)C_L]$
SR	$2I_{b1}/C_L$	$2KI_{b1}/[(K+1)C_L]$
$\overline{V_{IRNoise}^2}$	$\frac{8k_BT\gamma_p}{g_{mp}}(1+\frac{g_{mn}}{g_{mp}})$	$\approx \frac{8k_BT\gamma_p(K+1)}{g_{mp}}(1+\frac{g_{mn}}{g_{mp}}\frac{K+1}{K})$
PM	~90°	<90° depends on K

Transconductance & output resistance of NMOS [g_{mn}, r_{on}] and PMOS [g_{mp}, r_{op}]

Figure 17.2.1: DP amplifier outperforms the Current-Mirror amplifier in terms of $G_{m,eff}$, GBW, SR and noise, for any K. The NCM amplifier outperforms both by using the current to boost $G_{m,eff}$ and R_{out}.



This Design: $K_1=K_5=2$ $K_2=K_7=6$ $K_3=1$ $K_4=4$ $K_6=8$

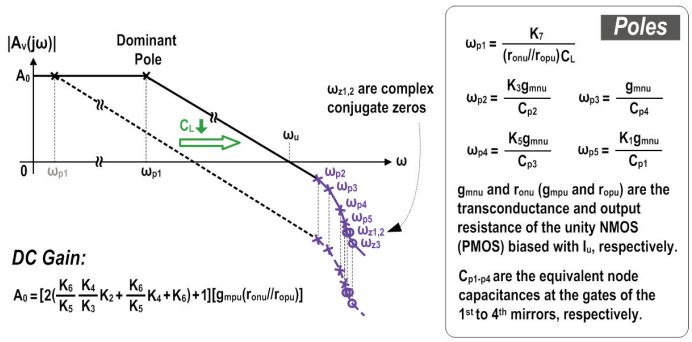
$I_b=(K_7+K_6+K_5+K_4+K_3+K_2+K_1+1)\cdot I_u$ $I_u=50nA$

$$G_{m,eff}=\frac{K_7[2(\frac{K_6}{K_5}\frac{K_4}{K_3}K_2+\frac{K_6}{K_5}K_4+K_6)+1]}{K_7+K_6+K_5+K_4+K_3+K_2+K_1+1}g_{mp} \qquad R_{out}=\frac{K_7+K_6+K_5+K_4+K_3+K_2+K_1+1}{K_7}(r_{on}/\!/r_{op})$$

$$GBW=\frac{K_7[2(\frac{K_6}{K_5}\frac{K_4}{K_3}K_2+\frac{K_6}{K_5}K_4+K_6)+1]}{K_7+K_6+K_5+K_4+K_3+K_2+K_1+1}\frac{g_{mp}}{C_L} \qquad SR=\frac{K_7(K_6+1)}{K_7+K_6+K_5+K_4+K_3+K_2+K_1+1}\frac{2I_b}{C_L}$$

$$\overline{V_{IRNoise}^2}\approx\frac{(K_7+K_6+K_5+K_4+K_3+K_2+K_1+1)[(\frac{K_6}{K_5}\frac{K_4}{K_3}\frac{K_2}{K_1})^2K_1+(\frac{K_6}{K_5}\frac{K_4}{K_3})^2(K_3+K_2)+(\frac{K_6}{K_5})^2(K_5+K_4)+K_6+1]}{[2(\frac{K_6}{K_5}\frac{K_4}{K_3}K_2+\frac{K_6}{K_5}K_4+K_6)+1]^2}\frac{8k_BT\gamma_p}{g_{mp}}(1+\frac{g_{mn}}{g_{mp}})$$

Figure 17.2.2: Implemented 4-step NCM single-stage amplifier.



Poles

$$\omega_{p1}=\frac{K_7}{(r_{onu}/\!/r_{opu})C_L}$$

$$\omega_{p2}=\frac{K_3g_{mnu}}{C_{p2}} \qquad \omega_{p3}=\frac{g_{mnu}}{C_{p4}}$$

$$\omega_{p4}=\frac{K_5g_{mnu}}{C_{p3}} \qquad \omega_{p5}=\frac{K_1g_{mnu}}{C_{p1}}$$

g_{mnu} and r_{onu} (g_{mpu} and r_{opu}) are the transconductance and output resistance of the unity NMOS (PMOS) biased with I_u, respectively.

$C_{p1\text{-}p4}$ are the equivalent node capacitances at the gates of the 1st to 4th mirrors, respectively.

Zeros

ω_{z1}, ω_{z2} and ω_{z3} are the roots of this 3rd-order polynomial: $N(s)=a_3s^3+a_2s^2+a_1s^1+a_0$

$$a_3=(K_6+1)\frac{1}{\omega_{p2}\omega_{p4}\omega_{p5}} \qquad a_2=(\frac{K_6}{K_5}K_4+2K_6+1)\frac{1}{\omega_{p2}\omega_{p5}}+(K_6+1)\frac{1}{\omega_{p2}\omega_{p4}}+(K_6+1)\frac{1}{\omega_{p4}\omega_{p5}}$$

$$a_1=(\frac{K_6}{K_5}K_4+2K_6+1)\frac{1}{\omega_{p2}}+(K_6+1)\frac{1}{\omega_{p4}}+(\frac{K_6}{K_5}\frac{K_4}{K_3}K_2+2\frac{K_6}{K_5}K_4+2K_6+1)\frac{1}{\omega_{p5}} \qquad a_0=[2(\frac{K_6}{K_5}\frac{K_4}{K_3}K_2+\frac{K_6}{K_5}K_4+K_6)+1]$$

Figure 17.2.3: Bode plot of the 4-step NCM single-stage amplifier.

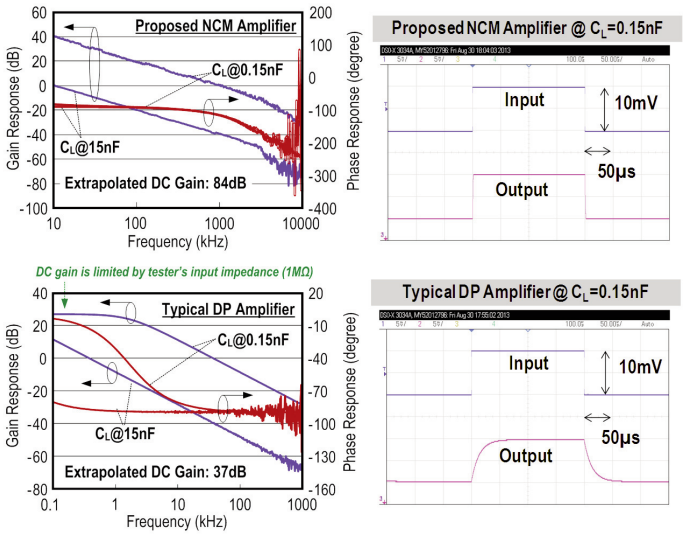


Figure 17.2.4: Measured AC (left) and small-step (right) responses of the NCM and DP amplifiers at equal power and area.

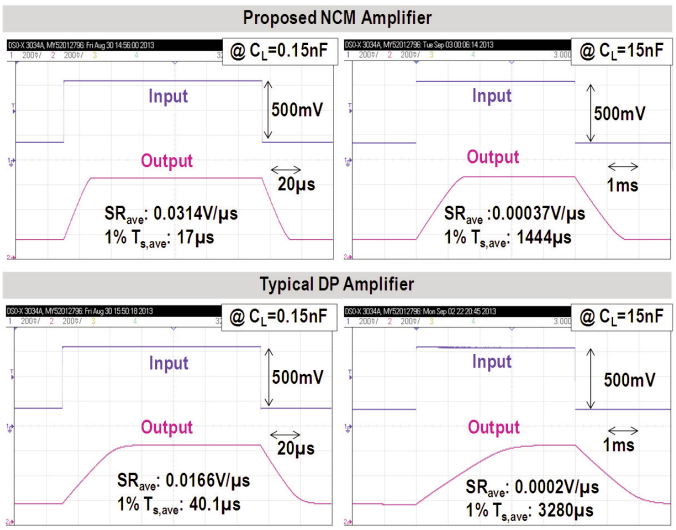


Figure 17.2.5: Measured large-step responses of the NCM (Upper) and DP (lower) amplifiers at equal power and area.

	Single-Stage Amplifiers					
Die Photo	Proposed NCM Amplifier			Typical DP Amplifier		
Load C_L (nF)	0.15	0.5	15	0.15	0.5	15
GBW (MHz)	1.24	0.396	0.013	0.0371	0.0116	0.00038
Phase Margin (degree)	62.4	81.4	90.2	91.7	92.5	92.9
Gain Margin (dB)	15.9	23.7	56.1	>60	>60	>60
SR_{ave} (V/µs)	0.0314	0.0115	0.00037	0.0166	0.0058	0.0002
1% $T_{s,ave}$ (µs)	17	47.1	1444	40.1	109	3280
DC Gain (dB) (extrapolated)	84			37		
Input-Referred Noise (nV/√Hz)	1470 @ 0.1kHz	440 @ 1kHz	140 @ 10kHz	680 @ 0.1kHz	270 @ 1kHz	106 @ 10kHz
Power (µW) @ V_{DD} (V)	3.6 @ 1.2			3.6 @ 1.2		
Chip Area (mm^2)	0.0013			0.0013		
CMOS Technology	0.18µm			0.18µm		
FOM_1 [(MHz·pF)/µW/mm^2]	39,744	42,308	41,667	1,189	1,239	1,218
FOM_2 [(V/µs·pF)/µW/mm^2]	1,006	1,229	1,186	532	620	641

Figure 17.2.6: Comparison of NCM and DP amplifiers under the same power and area.

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	Single-Stage Amplifier			*Three-Stage Amplifiers*		
	This Work (*NCM Amplifier*)			[2] JSSC Feb'11	[3] JSSC Sep'12	[4] * ISSCC'12
C_L Drivability ($C_{L,max}/C_{L,min}$)	100x			N/A	N/A	10x
C_L (nF)	0.15	0.5	15	0.15	0.5	15
GBW (MHz)	1.24	0.396	0.013	4.4	2	0.95
Phase Margin (degree)	62.4	81.4	90.2	57	52	52.3
Gain Margin (dB)	15.9	23.7	56.1	5#	8#	18.1
SR_{ave}(V/μs)	0.0314	0.0115	0.00037	1.8	0.65	0.22
1% $T_{s,ave}$ (μs)	17	47.1	1444	1.9	1.23	4.49
Input-Referred Noise ($nV/\sqrt{Hz}$)	1470 @ 0.1kHz	440 @ 1kHz	140 @ 10kHz	N/A	N/A	N/A
DC Gain (dB) (extrapolated)	84			110	>100	>100
Power (μW) @ V_{DD} (V)	3.6 @ 1.2			30 @ 1.5	20.4 @ 1.2	144 @ 2
Chip Area (mm^2)	0.0013			0.02	0.0088	0.016
CMOS Technology	0.18μm			0.35μm	65nm	0.35μm
FOM_1 [(MHz·pF)/μW/mm^2]	39,744	42,308	41,667	1,100	5,571	6,166
FOM_2 [(V/μs·pF)/μW/mm^2]	1,006	1,229	1,186	450	1,810	1,432

Figure 17.2.7: Performance comparison. * The data of [4] at 1.5nF is omitted here due to space limits. # means extracted values from figures.

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