2.7 A 0.003mm² 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz 1/f³ Phase-Noise Corner

Jun Yin[1], Pui-In Mak[1], Franco Maloberti[2], Rui P. Martins[1,3]

[1]University of Macau, Macau, China, [2]University of Pavia, Pavia, Italy, [3]Instituto Superior Tecnico, Lisbon, Portugal

Ring-VCOs (RVCOs) [1] have been avoided for over a decade for high-performance RF systems due to their much lower FOM (<165dB [2]) than that of their LC counterparts from low to high frequency offsets. Yet, as the cost of ultra-scaled CMOS technologies is escalating, the small-die-area and wide-tuning-range advantages of RVCOs have attracted more attention recently, aiming to break the FOM limit at the system level. In [2], a type-I PLL succeeds in suppressing the RVCO phase noise (PN) by extending the loop bandwidth to 10MHz ($f_{ref}/20 \rightarrow f_{ref}/2$), facilitating an ultra-compact (0.015mm²) frequency synthesizer for 2.4GHz WLAN. However, the type-I PLL only offers 20dB/dec phase-noise suppression for its RVCO. Thus, despite using large transistors (36/0.28μm), the 1/f³ PN corner (f_{1/f^3}) is still high (~4MHz), degrading the overall jitter performance of the PLL. This paper proposes a dual-mode time-interleaved RVCO (TI-RVCO). It offers interesting properties of extending the frequency tuning range and reducing f_{1/f^3} corner (~1MHz → ~100kHz), resulting in a better FOM over a wide range of frequency offsets (10kHz to 1MHz). The achieved f_{1/f^3} noise corner (~90kHz to 150kHz) is comparable to the state-of-the-art LC-VCOs [3, 4].

One effective way to suppress the 1/f³ noise is to avoid the 1/f noise upconversion, which can be predicted by the impulse sensitivity function (ISF) [1]. Since 1/f noises generated by NMOST and PMOST are uncorrelated, their induced PN power spectral densities is added (Fig. 2.7.1a). Assuming a triangular-shape ISF ($|\Gamma| = |\Gamma_{nmos}| = |\Gamma_{pmos}|$) and the same 1/f noise corner ($f_{1/f}$) for both NMOST and PMOST, the f_{1/f^3} of a multi-stage RVCO can be revised from [1] as

$$f_{1/f^3} = f_{1/f} \frac{3}{4\eta} \times \frac{1}{\text{No. of Stage}}$$

where η is a proportionality constant between each stage delay τ and the maximum slope k_{max} of the normalized RVCO output. Thus, given the transistor sizes and supply voltage (V_{DD}), increasing the number of stage helps reducing f_{1/f^3} corner, but at the expense of a lower output frequency.

The proposed TI-RVCO (Fig. 2.7.1b) extends the typical N-stage RVCO to NxM stages (M: the time-interleaved factor), such that all delay stages are relaxed in terms of operating frequency, i.e. f_o/M. A high-frequency output f_o is upheld by properly recombining the internal multi-phase outputs via a time-windowed phase combiner (TWPC). As long as the TWPC adds no noise, the RMS jitter of the combined output signal remains the same as that of a typical NxM-stage RVCO, while the output period is reduced by a factor M. Thus, the phase-noise profile of an NxM-stage TI-RVCO is an M-time-upshifted version of a typical NxM-stage RVCO (Fig. 2.7.1c), while keeping f_{1/f^3} unchanged. As a result, f_{1/f^3} would be reduced by M times when compared with a typical N-stage RVCO directly operating at f_o. The NxM-stage TI-RVCO can achieve the same 1/f² noise at large frequency offsets as the N-stage RVCO, since its 1/f² noise $\propto \Gamma_{rms}^2$ and thus $\propto 1/(NxM)^2$.

Enlarging the M factor can further reduce f_{1/f^3}, but this implies extra phases for combining, which exacerbates both delay mismatches in the TWPC and difficulty of the layout. Also, a large M factor leads to closer output spurs in the vicinity of f_o, i.e. $\pm hf_o/M$ where h=1,2,3... As the typical f_{1/f^3} of a RVCO, in advanced CMOS technologies, is around several MHz, a practical value of M can be 7, which is adequate to reduce f_{1/f^3} to several hundreds of kHz without compromising much on the spur level, power consumption and die area.

The desired phase combiner should be power efficient and should add minimum delay offset and mismatch between the different phases, which otherwise cause deterministic jitter and/or output spurs. The conventional phase combiner used in DLL-based clock multipliers [5] (Fig. 2.7.2a) suffers from a severe delay offset due to the asymmetrical inputs of the OR gate. Here, the proposed TWPC (Fig. 2.7.2b) eliminates fully the delay offset, as each selected phase can pass only through the transmission gate within the time window T_{win}. To ensure all time windows ($S_{5,10,15}$) are non-overlapping, T_{win} is upper-bounded by $(N-2)T_o/(2N)$ with N≥5. Thus, logic gates in the phase selector can be minimally sized to save power since T_{win} is long enough to tolerate reasonable PVT variations and mismatches. From Monte-Carlo (MC) simulations at f_o=3.5GHz (N=5, M=3), the mean and standard deviation, σ, of T_{win} are 87ps and 1ps, respectively. The tolerable time difference (T_p, Fig. 2.7.2b) is 29.7ps (σ=0.78ps), ensuring the rise/fall edge of each phase is captured within T_{win}. Comparatively, the phase combiner in Fig. 2.7.2a has a delay offset of +4/-6.4ps and a delay mismatch of σ=0.39ps, while the proposed circuit reduces the delay mismatch by 3.25× to σ=0.12ps and achieves a negligible delay offset (+10/-8fs) under a 0.1mW power budget.

To extend the tuning range, the TI-RVCO (Fig. 2.7.3) features a reconfigurable factor M. The selection of M depends on the original tuning range (TR_o) of the NxM-stage RVCO. If M is selectable as M_1 or M_2 (M_2>M_1), TR_o should be larger than $2(M_2-M_1)/(M_2+M_1)$ to allow a certain overlap between the 2 output bands. Under M=5 or 7, the output tuning range at f_o can be roughly doubled (~70%) relative to TR_o (38%). Besides, M≥5 is adequate to reduce the f_{1/f^3} corner from 1MHz to ≤200kHz. Such a dual-mode operation widens the tuning range using a small V_{DD} range. A very low V_{DD} is unfavorable as it significantly degrades the PN due to limited current and voltage swings. Dominated by the device mismatch in the delay stages, the output period at 3.5GHz shows a mismatch of σ=0.8ps (0.3% of T_{out}) in schematic-level MC simulations, resulting in output spurs <-50dBc.

Three prototypes were fabricated in 65nm CMOS (Fig. 2.7.7) for comparison: a 35-stage dual-mode TI-RVCO, a 15-stage TI-RVCO and a typical 5-stage RVCO. All delay stages have the same CMOS inverters (PMOST: 14/0.18μm, NMOST: 7/0.18μm). The f_{1/f^3} corner of the dual-mode TI-RVCO is reduced by 6.2× (930kHz→150kHz) when compared with that of a typical RVCO (Fig. 2.7.4), which follows closely the prediction of 7× by the ISF theory. At ~3.3GHz carrier, f_{1/f^3} corner is 150kHz for the TI-RVCO, which is comparable to the state-of-the-art LC-VCOs [3] (120 to 240kHz) and [4] (60 to 100kHz) that already feature 1/f³-noise-reduction techniques. The output spurs within the frequency offset $f_o \pm 2f_o/7$ are <–43.1dBc at V_{DD}=1V, which are mainly limited by the deterministic mismatch in the 2D layout to balance the dual modes (Fig. 2.7.7), and can likely be resolved by delay compensation in TWPC. The PN and FOM between the dual-mode TI-RVCO and typical RVCO are compared in Figs. 2.7.5a and b. The former achieves better results from 10kHz to 1MHz offsets, and shows a 68.5% tuning range using only 30% of V_{DD} downscaling (1 to 0.7V) with an adequate overlap (130MHz) between the two modes. The power efficiency is ~0.5mW/GHz at 3GHz (Fig. 2.7.5c), which is ~1.5× of the 5-stage RVCO.

Benchmarking with a typical 5-stage RVCO (Fig. 2.7.6), the dual-mode TI-RVCO reduces the f_{1/f^3} by 6.2×, which results in an improvement of FoM@10kHz/100kHz/1MHz by 6.8/4.5/0.7dB, respectively. Likewise, when contrasted with the RVCO + N-path filter technique [6], our TI-RVCO achieves >40× lower f_{1/f^3}, 10dB better FoM@100kHz offset and 5× smaller die area. The TI-RVCO, inherently offering a div-by-M output and can benefit the type-I PLL [2] in terms of power and PN over a wide range of frequency offsets, resulting in a better overall jitter performance.

Acknowledgements:
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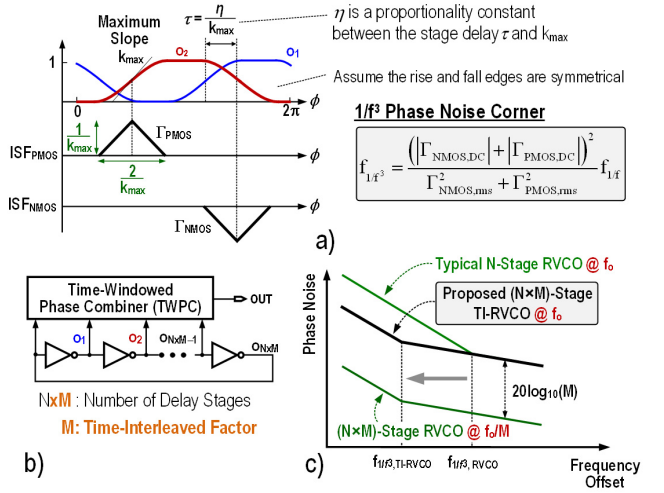

Figure 2.7.1: a) Predicted by the ISF, extending the number of delay stages in a RVCO can reduce the 1/f³ PN; b) TI-RVCO to achieve a smaller 1/f³ PN corner, as shown in c), while keeping a high f_0.

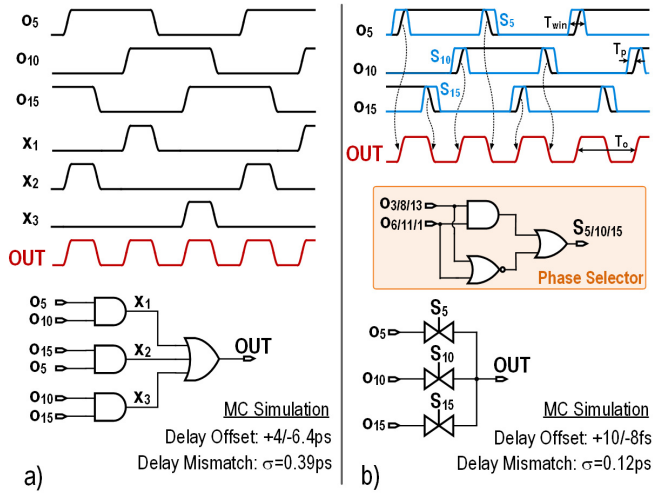

Figure 2.7.2: a) Typical logic-phase combiner [5] suffers from large delay offset and mismatch in the OR gate. b) Proposed TWPC nullifies the delay offset, and has 3.25× lower delay mismatch.

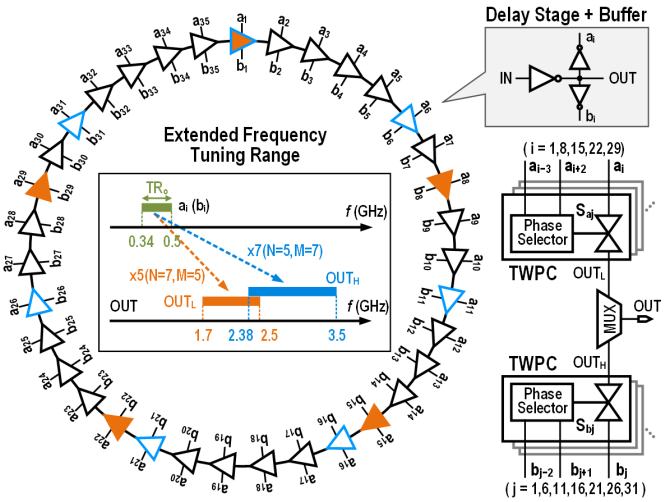

Figure 2.7.3: Proposed 35-stage dual-mode TI-RVCO. By properly combining the different output phases for high-band (×7) and low-band (×5) modes, the frequency tuning range can be extended.

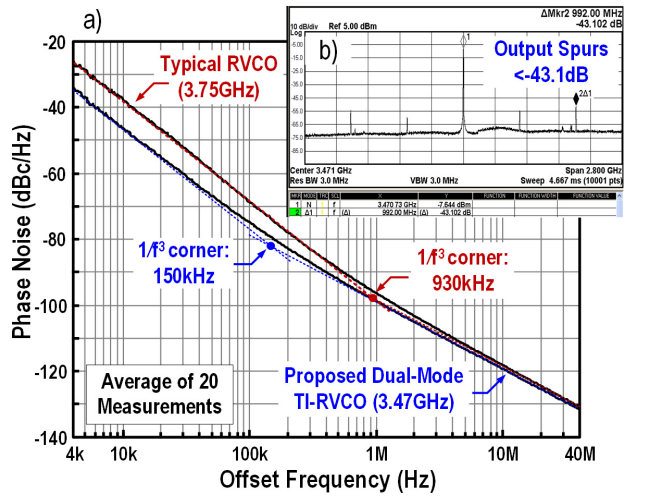

Figure 2.7.4: Measured a) PN of a typical RVCO and the proposed 35-stage dual-mode TI-RVCO; b) Mismatch-induced output spurs of the 35-stage dual-mode TI-RVCO.

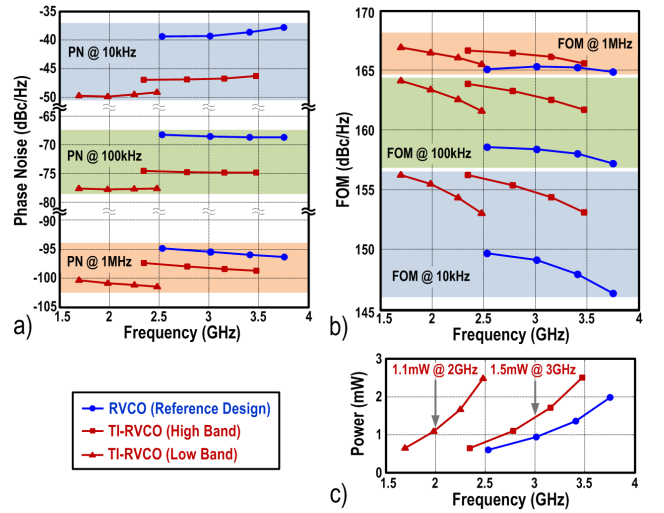

Figure 2.7.5: Measured a) PN; b) FOM; c) power consumption of the typical 5-stage RVCO and the proposed 35-stage dual-mode TI-RVCO in low- and high-band modes.

	3 Prototypes Fabricated in This Work				VLSI'14 [6]
Technique	35-Stage Dual-Mode TI-RVCO		15-Stage TI-RVCO	Typical 5-Stage RVCO	RVCO + N-Path Filter
Frequency Range (GHz)	1.7 to 3.47 (68.5%)		2.35 to 3.41 (36.8%)	2.53 to 3.75 (38.9%)	0.3 to 1.2 (120%)
Carrier (GHz) @V_{DD}	1.7 @ 0.7V	3.47 @ 1V	3.41 @ 1V	3.75 @ 1V	1.0 @ 1.2V
1/f³ Noise Corner (kHz)	90	150	340	930	6000 *
Power (mW)	0.65	2.51	2.25	1.99	4.7
PN @ 10kHz (dBc/Hz)	−49.7	−46.3	−43.7	−37.8	N/A
PN @ 100kHz (dBc/Hz)	−77.6	−74.9	−73.6	−68.7	−80*
PN @ 1MHz (dBc/Hz)	−100.4	−98.7	−98.9	−96.3	−110
FOM @ 10kHz (dBc/Hz)	156.2	153.1	150.8	146.3	N/A
FOM @ 100kHz (dBc/Hz)	164.1	161.7	160.7	157.2	153.3 *
FOM @ 1MHz (dBc/Hz)	166.9	165.6	166.0	164.8	163.3
Core Area (mm²)	0.003		0.00086	0.00024	0.015
CMOS Technology	65nm		65nm	65nm	65nm

* Estimated from PN plot $\quad FoM = -PN + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{DC}/1mW)$

Figure 2.7.6: Performance comparison.

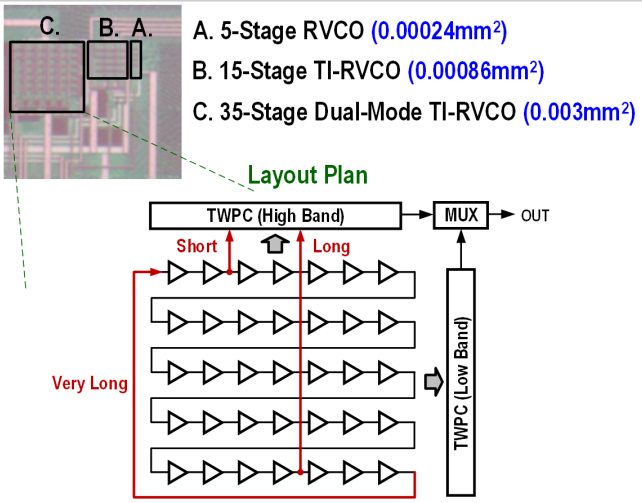

Figure 2.7.7: Die micrograph of the RVCO and TI-RCOs. The 35-stage dual-mode TI-RVCO has 5 rows each having 7 delay stages to be routed to the two TWPCs.

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