A Passive Excess-Loop-Delay Compensation Technique for Gm-C Based Continuous-Time ΣΔ Modulators

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***Abstract*— A method to compensate the Excess Loop Delay (ELD) in CT ΣΔ modulators using Gm-C loop filter is presented. The proposed circuit architecture uses a resistor in series with the integration capacitor to obtain a feed-forward adder in the Gm-C integrator. The proposed ELD compensation is based on the Proportional Integrating (PI) - element method for low power dissipation and simple implementation, and it is verified through the design of a 2nd order CT ΣΔ modulator which uses a Gm-C integrator as the 2nd stage of the loop filter. To further demonstrate the efficiency of the technique a Non-Return-to-Zero (NRZ) feedback is utilized due to its larger sensitivity to ELD. Simulation results show that a 68.9dB SNDR can be achieved with an ELD close to half clock period, while the system will be unstable without compensation for such an amount of the loop delay. These results confirm the effectiveness of the proposed ELD compensation method in Gm-C filter based CT ΣΔ modulators.**

I. INTRODUCTION

The Continuous-Time (CT) ΣΔ modulator is widely used in broadband telecommunication systems due to its large signal bandwidth, low power consumption, small area overhead, and also inherent anti-aliasing function. However, in contrast to its Discrete-Time (DT) counterpart, the CT ΣΔ modulator is very sensitive to clock jitter and Excess Loop Delay (ELD), that can degrade the system performance very seriously [1]. An effective option to reduce the clock jitter influence is the utilization of Non-Return-to-Zero (NRZ) feedback in the CT ΣΔ modulator. But, NRZ feedback is more sensitive to the ELD effect. Therefore, tradeoffs must be made between choosing feedback modes in the DAC topology and its performances.

ELD is normally induced by the nonzero switching time of the transistors in the quantizer and the DAC. It will shift a part of the feedback pulse into the next clock cycle. A certain amount shift of the feedback pulse will increase, mathematically, the order of the modulator, hence the loop stability may not be guaranteed under the ELD effect. Due to the serious effect of ELD in the CT ΣΔ modulator with NRZ feedback, several compensation methods have been proposed. However, most of them focus on CT ΣΔ modulators using an active RC loop filter. As one of the other most widely used integrators in the CT ΣΔ modulator, the Gm-C filter exhibits the benefits of inherent simplicity of the active elements with their open loop operation, which results in a high-speed potential and generally a small excess phase and power dissipation [2]. Thus, in this paper, a technique to compensate ELD in the CT ΣΔ modulator using Gm-C loop filter will be presented. The corresponding simulation results show that the ELD can be compensated up to half of a clock period.

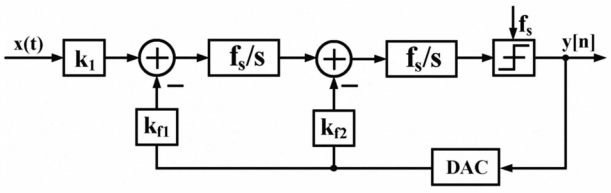

Fig. 1 An ideal 2nd order CT ΣΔ modulator with CIFB topology.

The effect of ELD in a CT ΣΔ modulator and several compensation methods will be analyzed in section II. Section III will introduce the proposed compensation technique for the CT ΣΔ modulator using a Gm-C loop filter. Section IV will show the simulation results verifying the effectiveness and advantage of the proposed technique. The conclusions will be drawn in section V.

II. ELD COMPENSATION FOR CT ΣΔ MODULATOR

Since ELD can significantly reduce the SNDR of a CT ΣΔ modulator its effect will be analyzed in detail in a 2nd order CT ΣΔ modulator. Fig. 1 shows the diagram of an ideal 2nd order CT ΣΔ modulator composed by a Cascade of Integrators in

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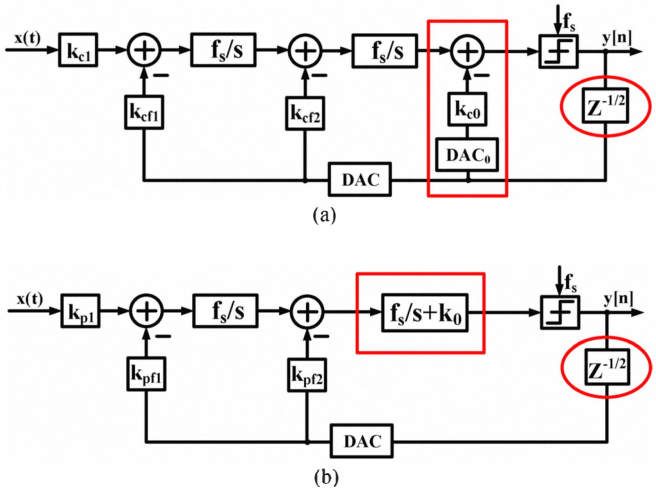

Fig.2 ELD compensation structures: (a) Classical (b) With PI-element.

Feedback (CIFB) [3]. CIFB topology has advantages over the Cascade of Integrators in Feedforward (CIFF) due to better intrinsic antialiasing and lower susceptibility to the peaking of signal transfer function (STF) [3].

The 2nd order modulator enjoys better stability when compared to higher order systems and its coefficients (shown in Fig. 1) can be obtained by transferring the corresponding DT coefficients into the z-domain. Besides, the standard form of its noise transfer function (NTF) is the following:

$$NTF = (1 - z^{-1})^2 \tag{1}$$

A. Classical ELD Compensation Method

Several methods have been proposed to compensate the ELD in CT ΣΔ modulators [2], [4]. A classical structure to compensate the ELD effect is represented in Fig.2 (a) which consists of a constant delay, equal to half of a clock cycle, placed before the feedback DAC and that can be implemented with a D Flip-Flop (DFF). The signal delay can be locked by the DFF within a certain time in order that smaller delay lengths could be contained within it. To analyze the compensation of the ELD effect the NTF of the classical structure (Fig. 2 (a)) is considered, theoretically, to be equal to (1). And, in terms of circuitry, with one adder and an extra DAC needed (highlighted in red), since the adder is obtained with an amplifier that will increase the power consumption.

B. ELD Compensation with PI-Element

For simplicity, another structure designated by Proportional-Integrating element (PI-element) has been introduced, illustrated in Fig.2 (b), which combines together the two inner loops of the previous topology [5]. Similarly, the NTF should be equal to (1). By matching the NTFs, the new coefficients of the system in Fig.2 (b) can be expressed in terms of k_{f1}, k_{f2} (Fig.1), and they will be given by (2).

Most previous works focus on the implementation of the ELD compensation in CT ΣΔ modulators with RC integrators, but, here, the proposed technique will concentrate in the design of an ELD compensation structure with PI-element

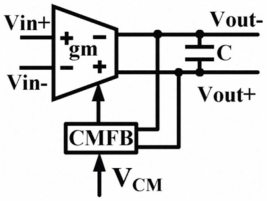

Fig. 3 Fully differential Gm-C loop filter with CMFB

utilizing Gm-C loop filters, due to the advantages previously mentioned and that will be further analyzed next.

$$k_{p1} = k_{pf1} = k_1$$

$$k_{pf2} = \frac{1}{2}k_{f2}\left(1 + \frac{1}{2}\frac{k_1}{k_{f2}} \pm \sqrt{1 - \frac{k_1}{k_{f2}} - \frac{1}{4}\frac{k_1^2}{k_{f2}^2}}\right) \tag{2}$$

$$k_0 = \frac{\frac{1}{4}k_{f2}\left(2 + \frac{1}{2}\frac{k_1}{k_{f2}}\right)}{k_{pf2}}$$

III. PI-Element Compensation with Gm-C Loop Filter

A. Proposed Technique with Gm-C Integrator

The proposed technique is based on the compensation theory shown in Fig. 2 (b) and utilizes at its core the Gm-C integrator. The general structure of such integrator is illustrated in Fig. 3, where the input voltage is transferred by the transconductor gm to the output current which is integrated in the capacitor producing a voltage drop. This operation principle can be described as here below:

$$\frac{V_o}{V_i} = \frac{g_m}{sC} = k\frac{f_s}{s} \tag{3}$$

Comparing this equation with the function presented in the red rectangular block shown in Fig. 2 (b) it can be found that the constant item k_0 should be generated in order to implement the PI-element with a Gm-C integrator. And, due to the definition of transconductance, if gm is multiplied by R then a constant will arise, which in circuit terms, to match with the theoretical diagram of Fig. 2 (b), can be achieved by the structure of Fig. 4 (a). Where, the corresponding voltage transfer function can be derived as:

$$\frac{V_o}{V_i} = \frac{g_{m1}}{sC}g_{m2}R + g_{m3}R \tag{4}$$

However, to implement the feedforward path two extra transconductors are needed, which will lead to additional power consumption due to its active circuit implementation. Hence, with this disadvantage, the circuit from Fig. 4 (a) is not the preferred choice to obtain the function $f_s/s+k_0$ from Fig. 2 (b) at circuit level, and a passive solution must be sought.

One possibility is illustrated in Fig. 4 (b) where the voltage transfer function is given by:

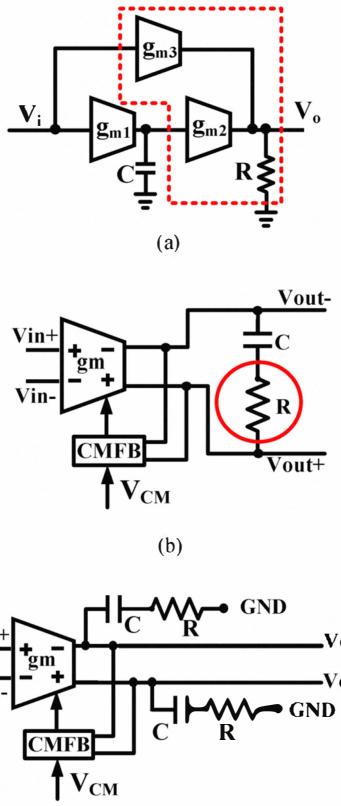

Fig. 4 ELD compensation with PI-element using Gm-C integrator: (a) Basic concept, (b) Proposed technique with passive implementation, (c) Modified improved structure.

$$\frac{V_o}{V_i} = \frac{g_m}{sC} + g_m \times R = k\frac{f_s}{s} + k_0 \qquad (5)$$

and it requires only one additional resistor to obtain the same NTF as in the classical structure, significantly reducing the circuit complexity. Traditionally, at least one adder and one extra DAC should be used (Fig. 2 (a)) which will complicate the circuit and increase the power consumption. Here, instead, the additional resistor R is used to realize the feedforward function and finally to have NTF equal to (1). Another benefit of this structure is the smaller loading at the output of the Gm-C integrator when compared with the original circuit from Fig. 4 (a), which can enhance the transconductor's speed and reduce the lower power consumption. A drawback of this passive structure is related with the parasitic capacitances that exist on the 2 terminals of the integrating capacitor. To overcome this, a modified improved structure is given in Fig. 4 (c). Here, the original C and R are separated into two identical branch elements connected in series between the 2 differential outputs of the transconductor and the ground.

This new modified Gm scheme, when introduced in a classical ELD compensation with Gm-C integrator (Fig. 5) [6], allows the removal of the transconductor Gm that operates as the adder and the additional feedback path, simplifying the whole circuit structure and reducing power consumption.

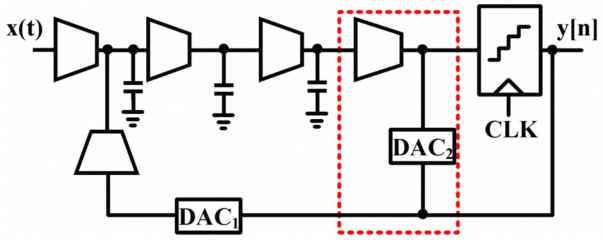

Fig. 5 Traditional ELD compensation with Gm-C integrator in CT ΣΔ modulator.

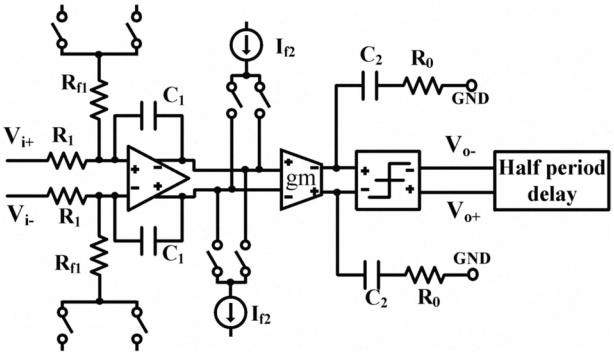

Fig. 6 Circuit schematic of the proposed ELD compensation structure with Gm-C integrator in a 2nd order, 1-bit, CT sigma-delta modulator with NRZ DAC.

Furthermore, extra elements can be realized by using only additional resistors.

B. Design Example of CT ΣΔ Modulator

In order to verify the proposed technique shown in Fig. 4 (c), a 2nd order, single-bit, low-pass CT ΣΔ modulator was designed based on the system diagram of Fig. 1, with a sampling rate of 250MS/s. The input bandwidth is 2MHz corresponding to the standard of 3G WCDMA receivers and the OSR is 64. NRZ feedback was chosen. The transformed CT coefficients were scaled down to guarantee that the signal swing will not reach the saturation level of the loop filter. The overall circuit schematic of the modulator is given in Fig. 6, which was implemented in 65nm CMOS with 1V supplied voltage. And, since the requirement of the second loop filter is released, a Gm-C loop filter can be used to save power, enhance the speed and simplify the circuit. Then, the circuit of Fig. 4 (c) was employed in the second loop filter to obtain the compensation with PI-element of Fig. 2 (b).

The calculation of the system coefficients with ELD compensation leads to: k_{p1}= 0.125, k_{pf1}= 0.125, k_{pf2}= 0.1692 and k_0= 0.646. Then, based on (5) and the working principle of RC integrator, the parameters of all the circuit elements in Fig. 6 can be obtained. Moreover, some considerations to get the value of resistors and capacitors can be made: the resistors can generate thermal noise; hence their values should not be too large. One the other hand, if the classical compensation method was used, the corresponding coefficients will be: k_{c1}= 0.125, k_{cf1}= 0.125, k_{cf2}= 0.25 and k_{c0}= 0.11. The values of the feedback coefficients are related to the power consumed by the feedback DAC. And, by comparing the feedback

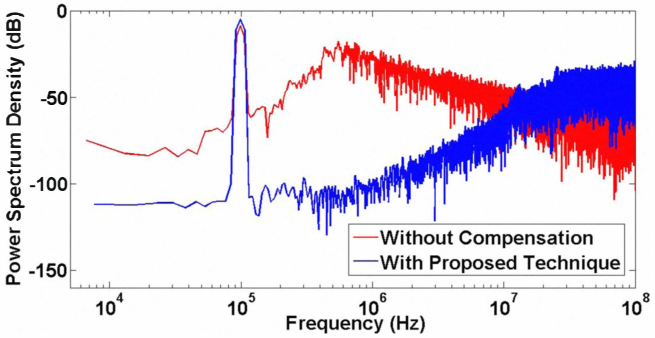

Fig. 7 Comparison of simulation results for 2 different cases when there is 50% Ts delay in the quantizer.

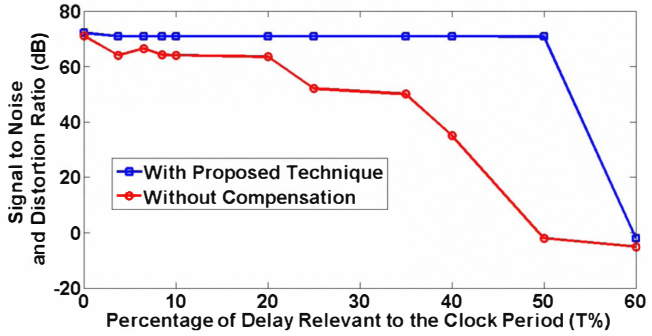

Fig. 8 Simulation results for system sensitive to ELD in a 2nd order CT ΣΔ modulator with proposed compensation technique and without compensation

coefficients in the two structures, it can be found that by using the proposed method the value of the feedback coefficients in the first stage is reduced from 0.25 to 0.1692, which will imply a power reduction of close to 32%.

IV. Simulation Results

The proposed compensation technique was implemented in a CT ΣΔ modulator and verified by transistor-level simulations. Fig. 7 shows the simulation results of the same modulator in two different cases, with and without ELD compensation. A value of 50% of T_S was added as delay in the system loop. The result exhibited by the red line shows the simulated PSD of the modulator without ELD compensation. It can be seen that its noise floor is much higher than that of the compensated system employing the proposed ELD technique (blue line); and also the noise shaping function has been distorted due to the change of the NTF. Basically, the system cannot work normally under 50% T_S loop delay without ELD compensation, in particular also because of the NRZ feedback. Then, the new circuit structure can achieve 68.9 dB SNDR which is close to an ideal case. The performance difference is mainly due to the differences between the noise-shaping curves. From the simulation results, for a general CT ΣΔ modulator, 50% Ts loop delay is large enough to imply the failure of the noise shaping function and destabilize the system. By contrast, after applying the proposed technique, the ELD effect can be compensated and the SNDR increases close to the ideal case. Theoretically, the proposed new scheme can compensate the loop delay if not larger than half clock period, as it can be see in Fig. 8, where the ELD tolerant ranges for the designed 2nd order CT ΣΔ modulator with and without the proposed ELD are provided.

V. Conclusions

This paper has proposed a novel compensation technique and its corresponding circuit scheme to the ELD effect in Gm-C integrator based CT ΣΔ modulators. The new structure uses a resistor, in series with the integration capacitor, which works as the adder creating a feedforward function. Half clock period of loop delay could be tolerated after employing the proposed compensation. Comparing it with existing solutions, this new method is simpler in terms of circuit implementation and consumes less power. Its behavior was verified through the design of a 2nd order CT ΣΔ modulator with NRZ feedback and a 2nd stage Gm-C integrator. Simulation results show that with a loop delay of 50% of Ts the CT ΣΔ modulator without ELD compensation was unstable; by contrast, the proposed modulator achieved 68.9dB SNDR which is close to the ideal case, further demonstrating the effectiveness of the new scheme.

Acknowledgment

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References

[1] J. A. Cherry and W. M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion.* Norwell, MA: Kluwer Academic, 2000.

[2] M. Ortmanns and F. Gerfers, *Continuous-Time Delta-Sigma A/D Conversion.* Springer, 2005.

[3] R. Schreier and G. C. Temes, *Understanding Delta–Sigma Data Converters.* Piscataway, NJ: IEEE Press, 2005.

[4] J. A. Cherry and W. M. Snelgrove, "Excess loop delay in continuous-time delta-sigma modulators," *IEEE Trans. Circuit Syst. II, Analog Digit. Signal Process.*, vol.46, no. 4, pp376-389, Apr. 1999.

[5] M.Vadipour, C. Chen, A. Yazdi, M. Nariman, T. Li, P. Kilcoyne, H. Darabi, " A 2.1 mW/3.2 mW Delay-Compensated GSM/WCDMA ΣΔ Analog-Digital Converter," in *Symposium on VLSI Circuits Digest of Technical Papers*, 2008

[6] R. Tortosa, A. Aceituno, J. M. Rosa, A. R. Vazquez, and F. V. Fernandez, "A 12-bit @ 40MS/s Gm-C Cascde 3-2 Continous-Time Sigma-Delta Modulator," in *Proc. IEEE International Symposium on Circuits and Systems - ISCAS*, 2007.