A Reconfigurable Low-Noise Dynamic Comparator with Offset Calibration in 90nm CMOS

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Abstract **- This paper presents a reconfigurable, low offset, low noise and high speed dynamic clocked-comparator for medium to high resolution Analog to Digital Converters (ADCs). The proposed comparator reduces the input referred noise by half and shows a better output driving capability when compared with the previous work. The offset, noise and power consumption can be controlled by a clock delay which allows simple reconfiguration. Moreover, the proposed offset calibration technique improves the offset voltage from 11.6mV to 533μV at 1 sigma. A prototype of the comparator is implemented in 90nm 1P8M CMOS with experimental results showing 320μV input referred noise at 1.5GHz with 1.2V supply.**

I. INTRODUCTION

Comparators are very important building blocks in Analog to Digital Converters (ADCs) since they are the components which transfer an analog difference to the digital logic. For the ADCs without intrinsic gain and error correction between each bit quantization, such as flash or successive approximation, the comparators have a stringent requirement imposing low noise, low power and high speed of operation. Single stage dynamic comparators [1] are widely adopted with the advantages of fast speed and zero static power consumption, but they combine the latch function with the input stage, which increases the number of cascading transistors from supply voltage to ground and limits the overdrive voltage of the input transistors. As a result, it restricts the period of the input transistors operating in saturation region and degrades the comparator's noise performance. Recently, a two stage dynamic comparator was presented [2] which achieved 3-fold noise improvement over conventional architectures [3]. However, the usage of PMOS output-latch stage reduces the driving current at the load and the limited duration for the input transistors to operate in the saturation region leaves room for further improvement of the noise performance.

Besides low noise, low offset is another critical concern in the design of ADCs. Usually, offset calibration with digital control is implemented to suppress the offset voltage by inserting unbalance capacitance at the comparator outputs [1] or adding an extra input pair of transistors [2]. But, these methods either degrade the speed of the comparator with extra output loads or increase its design complexity and area by adding extra bias voltage and capacitor for the calibration input transistors pair.

This paper presents a two stage dynamic comparator with offset calibration which exhibits low noise, low offset at high speed of operation. A variable delay between the clocks from the first and second stages of the comparator allows more time for the input transistors to operate in the saturation region while at the same time achieving reconfigurability over noise, offset and power performance. In addition, the proposed architecture improves comparator's noise and output-stage driving capability. On the other hand, an efficient offset calibration technique admits also a more compact design.

II. THE RECONFIGURABLE TWO-STAGE COMPARATOR

A. Circuit Implemetation

In order to suppress the comparator's noise, a large amplification of the input difference (ΔV_{in}) needs to be made at its input stage. As the gain of a dynamic amplifier is defined by $g_m t/C$ (g_m is the transconductance of the input transistors, t is the time for amplification and C the capacitance load), it is important to maintain the input transistors in saturation region ($g_m < g_{ds}$) for a giving time of amplification [4].

The enhanced version of two stage dynamic comparator's [2]

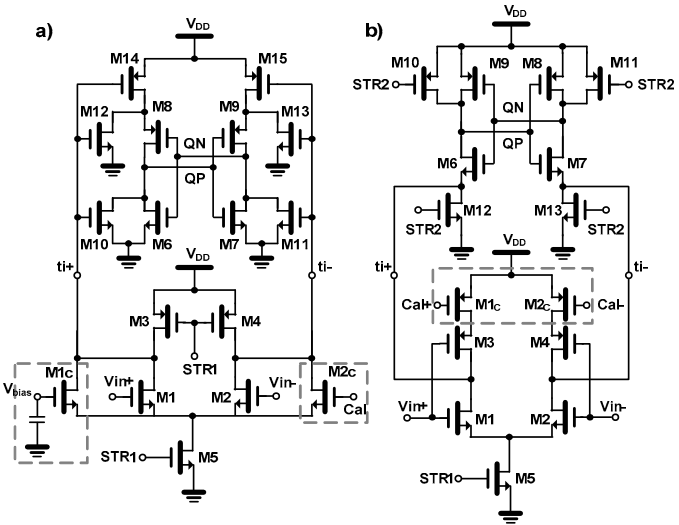

Fig. 1. Circuit schematic of two stage comparators (a) in [2] with three-fold noise improved from [3] and (b) the proposed.

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and proposed comparator's circuit architectures are shown in Fig. 1. The comparator in [2] uses an NMOS input stage with a PMOS output-latch, where the outputs of the first stage are applied to the output-latch as clock signals. On the contrary, the proposed comparator utilizes different clock signals for the first and second stages which can extend the time in saturation of the input transistors, and improve the speed sensitivity over the input voltage difference and noise performance. With NMOS transistor at the input and output-latch stages (M1-2 and M12-13), the proposed comparator also shows a better driving capability at the outputs when compared with the former work.

The signal behavior of the proposed comparator is shown in Fig. 2 and its operation details can be described as follows: during reset phase (STR1=0 and STR2=0) and voltages at Cal+ and Cal- close to ground, the intermediate nodes (ti+, ti-) and output nodes (QN, QP) are charged to V_{DD} through M3, M4 and M10, M11 which are turned on by the inputs at around common-mode voltage ; at phase 1 during comparison (STR1=1 and STR2=0), M5 is turned on and a current path from supply to ground through the dynamic inverter (M1~M4) is established. Furthermore, the intermediate nodes (ti+ and ti-) are discharged with a time difference (Δt) depending on the comparator's inputs and the skew rate of the dynamic inverters. During this period, M10 and M11 are still on and they provide other current paths to the first stage through M6 and M7, keeping the input transistor pair (M1, M2) saturated. After the phase 1 of the comparison, STR2 moves to V_{DD} and the back-to-back dynamic inverters (M6~9, M12, M13), in the second stage, regenerate the current difference from the first stage to a logic level V_{DD} or ground at QP and QN.

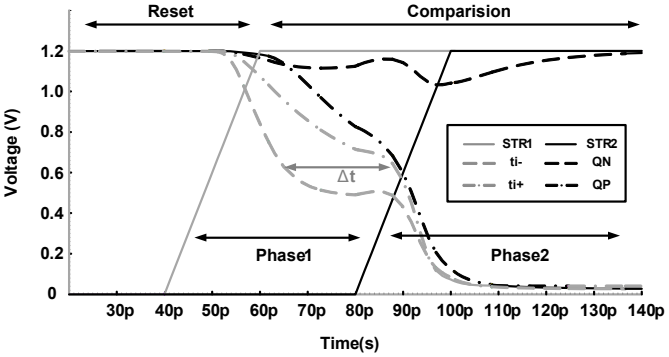

Fig. 2. Signal behavior of the proposed comparator.

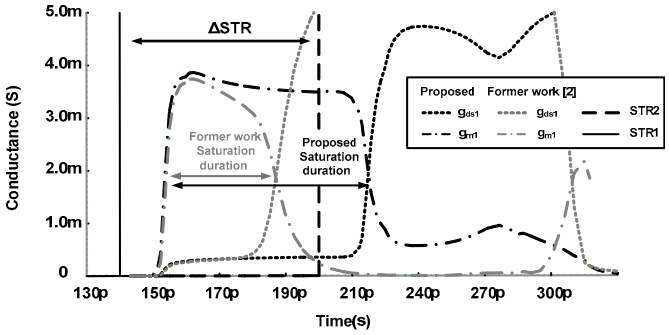

Fig 3. Small signal parameter behavior of former work in [2] and proposed comparators.

B. *Improvements from Previous Achitecture*

a) *Input Referred Noise Improvement*

Different from the previous work in [2] , the outputs of the first stage do not connect to any gate terminal of the second stage transistors. Instead, they connect to the source terminal of M6 and M7, respectively, which provides another current branch during phase 1 of the comparison and expands the saturation period of the input pair (M1 and M2). It is easier to identify the improved extension region comparing the small signal parameters of the proposed and former work, as illustrated in Fig. 3. The simulated waveform has been obtained from *Spectre* with same sizes of transistors used in the design of [2] and proposed architectures with a delay between STR1 and STR2 (ΔSTR) of 60ps. When $g_{m1} < g_{ds1}$, the input transistor M1 operates in saturation and it can be observed that the input transistors pair of the proposed comparator stay longer in saturation region than in the comparing one. In large signal behavior, the effect of extending the time in saturation in the proposed architecture implies a larger Δt, leading to 23ps which can be compared to the 11ps of the previous work.

Fig. 4(a) illustrates the simulated results of the comparator error probability under noise, with identical transistors sizing in [2] and the proposed comparators, ΔSTR is 60ps, the operating frequency is 2GHz with V_{DD} at 1.2V and common-mode input voltage V_{CM} at 0.6V. Without offset calibration in both comparators and fitting the results to Gaussian cumulative distribution as similar approach in [2], the proposed and the comparing comparators achieve 0.2mV and 0.41mV RMS equivalent input referred noise $V_{in}(\sigma)$ at 1 sigma, respectively. These results indicate that the input referred noise of the proposed comparator is half of the former design. Fig. 4(b) shows the noise performance of both comparators versus V_{CM}. The simulated results demonstrate that the proposed architecture has lower input referred noise in a wide range of input common-mode voltages.

b) *Reconfigurable Charateristic*

In the proposed circuit, transistors M12 and M13 are used for speeding up the regeneration time of the back-to-back inverter and the turn on time of these transistors control the power consumption, offset and noise performance of the overall comparator. During phase1 of the comparison, the regenerative inverter (M9, M6) stacks with M1 and M5 from V_{DD} to ground which limits the regeneration speed. In the meantime, the regeneration has begun depending on the comparator's inputs and this regeneration process is not reversible because of the positive feedback of the back-to-back inverters. Thus, it is possible to add an extra pull down path to shorten the regeneration time after the regeneration process begins. As a result, the delay between STR1 and STR2 can control the dynamic gain of the first stage, which affects the power consumption, resolution and offset of the comparator. Fig. 4(c) illustrates the error probability and power consumption ratio of the proposed comparator versus delay between STR1 and STR2 with input voltage difference at 0.2mV. With the same size of input transistors, the proposed architecture achieves better noise performance under the condition of ΔSTR larger than 10ps, with a power consumption around 77% of the design in [2]. Even when ΔSTR is zero, the noise performance of the proposed architecture is similar to the comparing one, thus it can be proved that the proposed circuit always has better noise performance if there is some delay between STR1 and STR2. Besides, these results show that the error of the comparator increases rapidly as the time delay is reduced and the power consumption is proportionally shrunk versus delay. The variation of the offset voltage with different ΔSTR will be presented next.

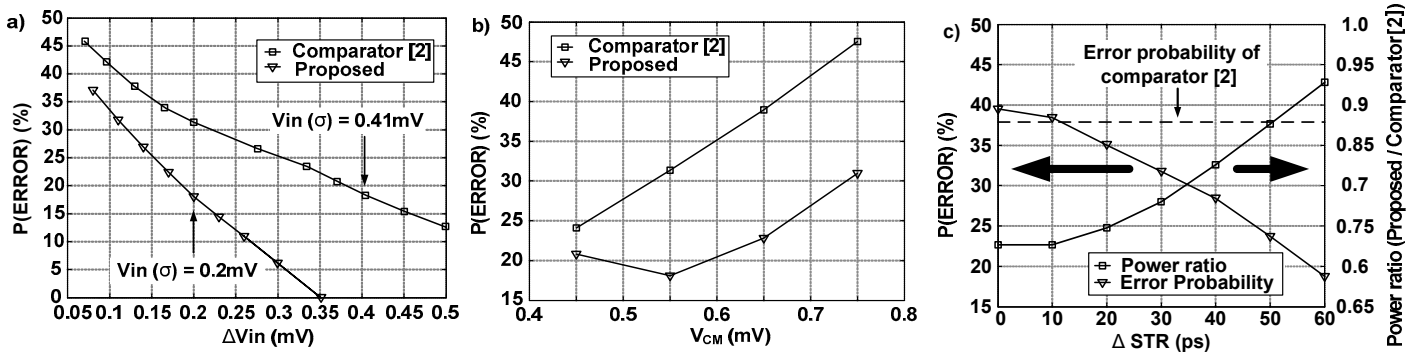

Fig 4. Simulated result of the conventional and proposed comparator (a) cumulative noise distribution (operated at 2GHz, ΔSTR = 60ps), (b) error probability vs. common mode voltage, and, (c) error probability and power ratio vs. ΔSTR.

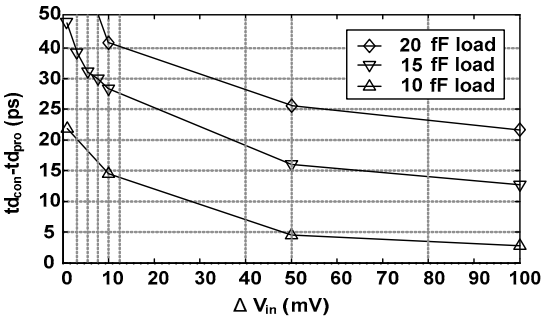

Fig 5. Simulated delay difference (td_{con} - td_{pro}) vs. $\Delta V_{in.}$

c) Speed and Sensitivity Improvements

Unlike the former design in [2], the proposed comparator can utilize NMOS input stage with NMOS output stage and the clock signal for the second stage does not depend on the input. Thus, it can be indicated that the delay of the proposed comparator is less sensitive to its inputs and it can drive larger loads at the outputs. Fig. 5 shows the simulation results of the delay difference at the output nodes between the comparing circuits and the proposed (td_{con} - td_{pro}) with different loads at the output. The delay is measured from 70% of the rising output edge for the comparator in [2] and 30% of falling edge output for the proposed. The delay/log(ΔV_{in}) (reflecting the delay sensitivity to the input) of both comparators, proposed and previous work, are 16ps/dec and 28ps/dec, respectively. Even with an additional 60ps delay between the clock signal of the first and second stages, the proposed comparator operates faster than the comparing architecture with 10fF, 15fF and 20fF loads.

III. OFFSET CALIBRATION

The circuit schematic of the proposed offset calibration is shown in Fig. 6. Instead of extra input transistors in [2], the proposed method adopts triode region load transistors (M1c, M2c) for current compensation and removes the extra bias circuits from the configuration in former design (Fig. 1), thus reducing the design complexity and chip area. Furthermore, widely adopted charge pump scheme is also utilized for controlling the calibration nodes voltages (Cal+, Cal-) which contributes as well for compact area and low power consumption. With little extra digital headroom (four multiplexers, two D-flip-flops and two Nand gates) the calibration is applied to both branches of the comparator to enlarge its calibration range.

The operation of the calibration can be described as follows: during calibration (CAL=V_{DD}), the common-mode voltage is applied to the inputs of the comparator and its outputs trigger one of the D-flip-flop which discharges its output (Off_N/Off_P) from V_{DD} to ground depending on the offset polarity. Then, the offset sign signal (Off_N, Off_P) determines which outputs of the comparator (QN, QP) and calibration nodes (Cal+, Cal-) are being connected to the charge pump circuit through multiplexers MUX1, MUX2 and MUX3, MUX4, respectively. At last, the charge pump circuit will investigate the calibration voltage from ground to V_{DD} and stops when the offset is adjusted to zero. With this scheme, the change of the calibration voltage varies the resistance of M1c or M2c, and compensates the current difference on both branches of the comparator. Since triode region load is adopted, one of the calibration nodes can be simply connected to ground rather than to the bias circuit as in [2]. Morever, the compensation offset voltage generated from M1c and M2c is divided by the gain of the comparator at first stage which increases the resolution and lowers the noise sensitivity of the whole calibration.

The offset voltage of 100 times Monte-Carlo simulation of the comparator in [2] and proposed with or without calibration are shown in Fig. 7. With different delays between STR1 and STR2 of the proposed comparator (0ps and 60ps), the offset voltage

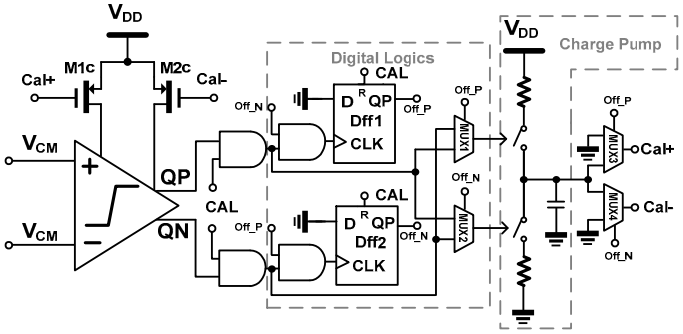

Fig. 6. Circuit schematic of the proposed offset calibration scheme.

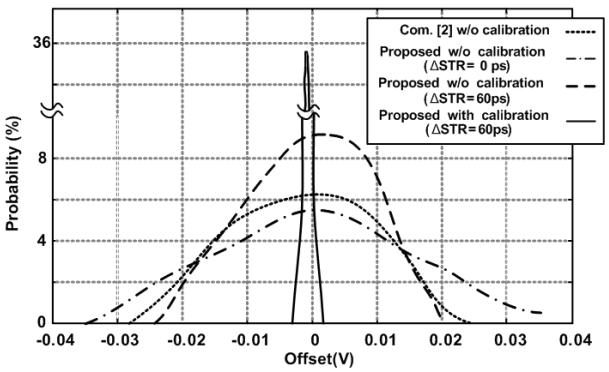

Fig 7. Simulated offset distribution of input offset voltage with noise.

distribution varied from 13.3mV to 8.5mV while with the comparing one is 10.2mV at 1 sigma. Furthermore, with the proposed comparator after calibration (ΔSTR=60ps) , the offset voltage is reduced to 420μV also at 1 sigma. Besides, it can be observed that the offset voltage is not very sensitive to the delay of STR1 and STR2 because it is mainly produced by the first stage of the comparator which is not affected by its own dynamic gain.

IV. Measurement Results

The proposed comparator has been implemented in 90nm CMOS process with 1.2V supply and the chip photo is shown in Fig 8. The area of clock generator and calibration logic, and comparator are 970μm^2 and 360μm^2, respectively. In the testing bench, the measurement of the input noise sigma was obtained by counting the bit error rate of the comparator output when a differential increasing step voltage is applied to its inputs with the same V_{CM}. The offset voltage is measured when the count of the comparator output is closed to 50% as an increasing step voltage is applied. Moreover, the ΔSTR is implemented with a PMOS voltage variable capacitance with off-chip voltage control placing between two inverters buffer and the typical delay of a buffer is around 23ps in the adopted technology.

The RMS offset voltage of the proposed comparator was measured in 16 chips (two comparators per chip) at 1GHz with the offset calibration performed before measurement. The measured results show that the offset voltage of the proposed comparator is 11.6mV and 533μV at 1 sigma before and after the calibration, respectively (ΔSTR in 30ps), as seen in Fig. 9. In addition, the input referred noise of the proposed comparator versus ΔV_{in} and ΔSTR is illustrated in Fig. 10. The ΔSTR is extracted from the experimental and post-layout simulation results from the off-chip control voltage. These results indicate that the input referred noise is reduced as ΔSTR increased, and the input referred noise of the proposed comparator is around 320μV when it operates at 1GHz with ΔSTR in 61ps and at 1.5GHz with ΔSTR in 79ps. Table I illustrates a benchmark of the state-of-the-art comparator architectures, comparing the current design with relevant works from [2], [3] and [5], showing the enhanced results of the proposed architecture. The measured power consumption of the proposed comparator is larger than [2] which mainly due to the rise of supply voltage in the adopted technology.

V. Conclusions

A low noise, low offset and high speed dynamic comparator with offset calibration has been proposed. The comparator utilizes different clock delays between the first and second stages to achieve reconfigurable capability. Measured results show that the input referred noise of the proposed comparator is 320μV at 1.5GHz which is better than what is obtained with the comparing architectures. In addition, the proposed circuit shows a better driving capability at the output-latch stage and its speed is less sensitive to the input, also when compared with previous work.

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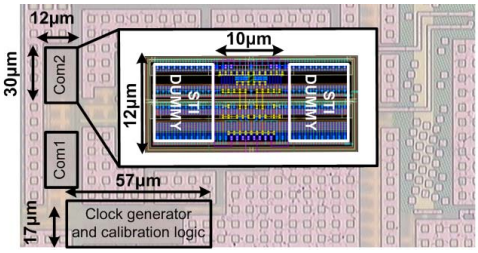

Fig. 8. Chip photo and layout of the proposed comparator.

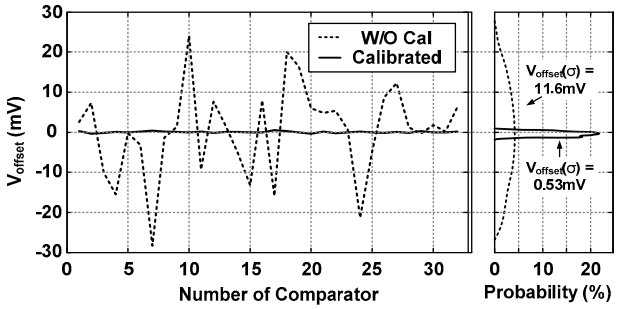

Fig. 9. Offset voltage of the comparators with and w/o calibration (ΔSTR = 30ps) – Measured.

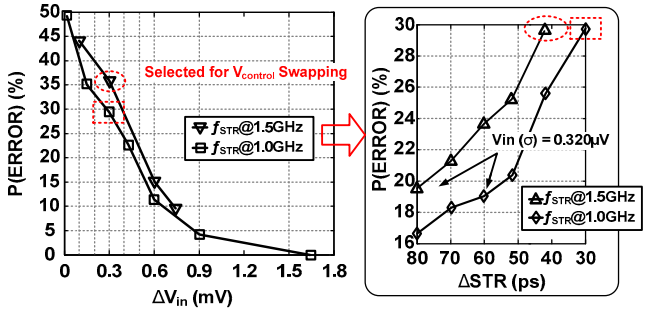

Fig. 10. Probability error vs. ΔV_{in} (left) and ΔSTR (right) at 1.5GHz and 1GHz operation frequency – Measured.

TABLE I
Benchmark of Comparator Architectures

	ESSCIRC'07[3]	A-SSCC'08[2]	A-SSCC'10[5]	This work
Technology	120nm (1.5V_{DD})	90nm (1.0V_{DD})	65nm (1.2V_{DD})	90nm (1.2V_{DD})
$V_{in}(\sigma)$ (mV)	3.9mV (@1.5GHz)	1mV(@1GHz)	40mV (@1.5GHz) 200mV (@7.2GHz)	320μV (@1.5GHz)
Delay/log(ΔV_{in})	N/A	24.3ps/dec	N/A	16ps/dec
Cal. offset	N/A	1.69mV	N/A	533μV
Power/f_{STR}	250μW/GHz	40μW/GHz	63μW/GHz	61μW/GHz

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