Design of Current Mode Instrumentation Amplifier for Portable Biosignal Acquisition System

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***Abstract*—This paper describes the design of current mode instrumentation amplifier (CMIA) for portable biosignal acquisition system. The CMIA topology is based on voltage mode operational amplifier (op amp) power supply current sensing technique. Op amp mismatch and precise current mirrors are two design challenges of this topology. A simulation analysis is conducted based on an implementation in a CMOS 0.35 µm technology. The CMIA consumes 20.22 µW under a 3 V DC power supply and has a continuous adjustable gain bandwidth product (GBW)-independent voltage gain via single resistor. The CMRR is higher than 120dB up to 1 Hz and more than 80 dB up to 100 Hz.**

I. Introduction

ELECTROCARDIOGRAM (ECG), electroencephalogram (EEG) and electromyogram (EMG) are common biopotential signals for practical clinic and health care applications. These signals have very low amplitudes and locate in very low frequency band as listed in Table I.

TABLE I
BIOPOTENTIAL SIGNALS [1] [2]

	ECG	EEG	EMG
Amplitude (µV)	1000-10000	10-50	50-5000
Frequency (Hz)	0.5-100	0.1-100	10-1000

In order to extract the small low frequency differential signals out from large common mode interference of human body, a well designed instrumentation amplifier (IA) is essential. The IA should issue low input noise, low harmonic distortion, controllable voltage gain and high common mode rejection ratio (CMRR). Moreover, for long term and portable monitoring application, the IA is also required to have low power consumption and small size [3][4]. Hence, the circuit is expected to be implemented in a modern integrated circuit technology.

Current mode instrumentation amplifier (CMIA) has many advantages compared with traditional voltage mode one, such as no complex resistor network, gain bandwidth product (GBW) independent voltage gain and high CMRR which is independent of differential gain. The CMIA topology involves operational amplifier (op amp) power supply current sensing technique is first reported by B. Wilson [5] as a second generation current conveyor (CCII) [6] in 1984 and then developed as a current mode amplifier [7] and an instrumentation amplifier [8] in 1989. Later and recently, this CMIA is further developed and reported by many works [9]-[13]. A comprehensive and detailed analysis of this CMIA is given in [14]; however, it only concerns effect on CMRR due to input op amp mismatch and gives measurement results of discrete circuit implementation. There is still lack of detailed design using this circuit topology.

This paper describes the design of such a CMIA in a CMOS 0.35µm technology. Both theoretical analysis and circuit design with simulation analysis are conducted.

The work presented in this paper is supported by the Research Committee of the University of Macau under Grants RG051/05-06S/VMI/FST, RG061/06-07S/VMI/FST, RG075/07-08S/VMI/FST and by The Science and Technology Development Fund of Macau under grant 014/2007/A1.

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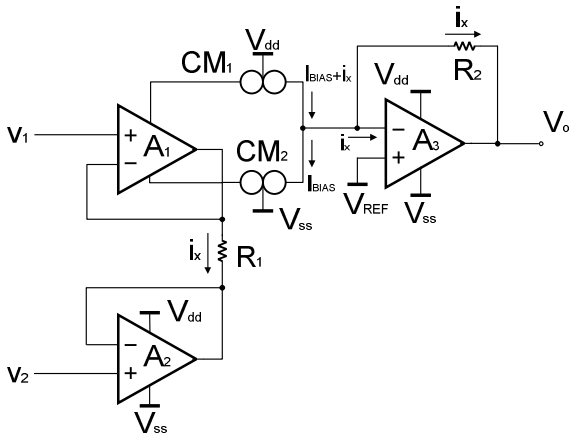

Fig. 1. Current mode instrumentation amplifier topology using op amp power supply current sensing technique.

II. Theoretical Analysis

A. Circuit Description

Fig. 1 shows the schematic of the proposed CMIA topology. This CMIA consists of two input op amps A_1 and A_2 and a resistor R_1 as the differential input stage. A_1 and A_2 are connected as unit gain buffers to convey the input voltages on resistor R_1. Since common mode voltages at the two terminals of R_1 is expected to be equal to each other, only differential current $i_x = (v_1 - v_2) / R_1$ flows through. By applying power supply current sensing technique, two current mirrors CM_1 and CM_2 are added to both positive and negative power supply terminals of A_1 and copy i_x precisely to the next stage. Op amp A_3 and resistor R_2 form the output stage of the CMIA. A_3 is connected as a transresistance amplifier to create a virtual ground at the outputs of CM_1 and CM_2 and convert i_x

into voltage via R_2. Once the differential current i_x flows through R_2, a differential output voltage $V_o = i_x R_2$ is induced at the output terminal of A_3. Hence, the overall differential gain is simply $G_d = R_2 / R_1$. Ideally, common mode input voltage induces zero differential current; hence an infinity CMRR is obtained.

B. CMRR Analysis

Assuming A_1, A_2 and A_3 have non-matched differential mode and common mode gains, say, $A_{d1, c1}$, $A_{d2, c2}$ and $A_{d3, c3}$ respectively. It is easy to find that the outputs of A_1 (v_{o1}) and A_2 (v_{o2}) are,

$$v_{o1} = \left(\frac{A_{d1} + A_{c1}/2}{A_{d1} - A_{c1}/2 + 1}\right) v_1 \quad (1a)$$

$$v_{o2} = \left(\frac{A_{d2} + A_{c2}/2}{A_{d2} - A_{c2}/2 + 1}\right) v_2 \quad (1b)$$

If the current mirrors CM_1 and CM_2 are ideal, differential current i_x generated by the input stage is $i_x = (v_{o1} - v_{o2}) / R_1$ and the corresponding output voltage of A_3 is $V_o = i_x R_2 + V_{REF}$. Hence the output voltage is,

$$V_o = V_{REF}\frac{A_{d3} + \frac{A_{c3}}{2}}{A_{d3} - \frac{A_{c3}}{2} + 1} + i_x R_2 \frac{\frac{A_{c3}}{2} - A_{d3}}{A_{d3} - \frac{A_{c3}}{2} + 1} \quad (2)$$

Where,

$$i_x = \frac{1}{R_1}\left(v_1 \frac{A_{d1} + \frac{A_{c1}}{2}}{A_{d1} - \frac{A_{c1}}{2} + 1} - v_2 \frac{A_{d2} + \frac{A_{c2}}{2}}{A_{d2} - \frac{A_{c2}}{2} + 1}\right) \quad (3)$$

Let G_d and G_c are the overall differential mode and common mode gains of the CMIA, $V_o = G_d (v_1 - v_2) + G_c (v_1 + v_2) / 2$. By applying (2) and (3), G_d and G_c can be expressed by,

$$G_d = \frac{R_2}{2R_1}\frac{2A_{d1}A_{d2} + A_{d1} - \frac{1}{2}A_{c1}A_{c2} + \frac{1}{2}A_{c1} + A_{d2} + \frac{1}{2}A_{c2}}{(A_{d1} - \frac{1}{2}A_{c1} + 1)(A_{d2} - \frac{1}{2}A_{c2} + 1)} \quad (4a)$$

$$G_c = \frac{R_2}{R_1}\frac{A_{d1} - A_{d1}A_{c2} + A_{c1}A_{d2} + \frac{1}{2}A_{c1} - A_{d2} - \frac{1}{2}A_{c2}}{(A_{d1} - \frac{1}{2}A_{c1} + 1)(A_{d2} - \frac{1}{2}A_{c2} + 1)} \quad (4b)$$

According to the definition of CMRR, $CMRR_{IA} = G_d / G_c$, from 4(a) and 4(b), the overall CMRR is,

$$CMRR_{IA} = \frac{1}{2}\frac{2A_{d1}A_{d2} + A_{d1} - \frac{1}{2}A_{c1}A_{c2} + \frac{1}{2}A_{c1} + A_{d2} + \frac{1}{2}A_{c2}}{A_{d1} - A_{d1}A_{c2} + A_{c1}A_{d2} + \frac{1}{2}A_{c1} - A_{d2} - \frac{1}{2}A_{c2}} \quad (5)$$

When the frequency is much lower than the corner frequencies of op amps, i.e. $A_d >> A_c$, (5) can be deduced to,

$$CMRR_{IA} \cong \frac{A_{d1}A_{d2}}{A_{d1} - A_{d1}A_{c2} + A_{c1}A_{d2} - A_{d2}} \quad (6)$$

$$\frac{1}{CMRR_{IA}} \cong \frac{1}{A_{d2}} - \frac{1}{A_{d1}} + \frac{1}{CMRR_1} - \frac{1}{CMRR_2} \quad (7)$$

Where, $CMRR_1 = A_{d1} / A_{c1}$ and $CMRR_2 = A_{d2} / A_{c2}$ are CMRRs of A_1 and A_2 respectively.

From (5), high CMRR requires either high differential gains or matched differential mode and common mode gains of input op amps. Since high gain op amp is not practical for modern CMOS technology and according to equation (7), well matched differential mode gains and CMRRs of A_1 and A_2 are dominative to the overall CMRR performance. Hence, differential mode gains should be matched very well in the first place. On the other hand, CMRR is the ratio of differential mode and common mode gains and easier to be adjusted than common mode gain. It is advisable to possibly make CMRRs of input op amps matched but not the common mode gains.

III. Circuit Implementation

A. Operational Amplifier (Op Amp)

The schematic of op amp is drawn from two-stage topology with miller-compensated capacitor. In Fig. 3, transistors M_1-M_{13}, M_{14}-M_{26} and M_{35}-M_{43} build up op amps A_1, A_2 and A_3 respectively. The current mirrors CM_1 and CM_2 are built on the output stages of them. The input pairs of all op amps are PMOS transistors in order to have a less 1/f noise. Table II shows the specifications of input op amps and Fig.2 is the simulated frequency response.

It is important to note that the output impedance should be designed carefully. Mismatch of this parameter also decreases the CMRR performance of the CMIA [14] and it is sensitive to the resistance of R_1.

TABLE II
OP AMP SPECIFICATIONS

Open loop gain	50 dB
3 dB frequency	600 Hz
GBW	185 KHz
Phase margin	65°
CMRR up to 3 KHz	100 dB
Power consumption under 3 V	4.9 μW

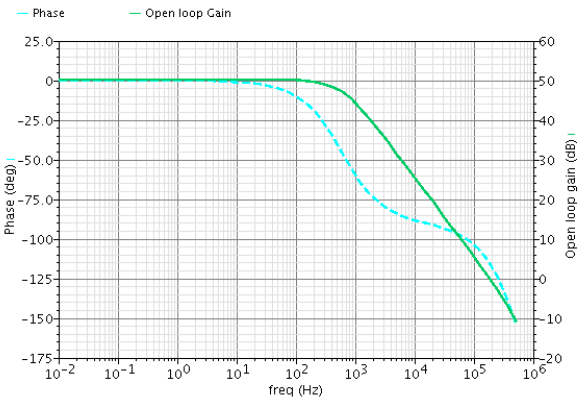

Fig. 2. Frequency response of input op amp.

B. Current Mirror

Although mismatch of input op amps is a serious problem of CMRR performance, current mirrors also play significant roles. From [14] it is observed that even the differential gains of two discrete input op amps have a difference up to 5% and an output impedance difference about 4%, the CMRR still can

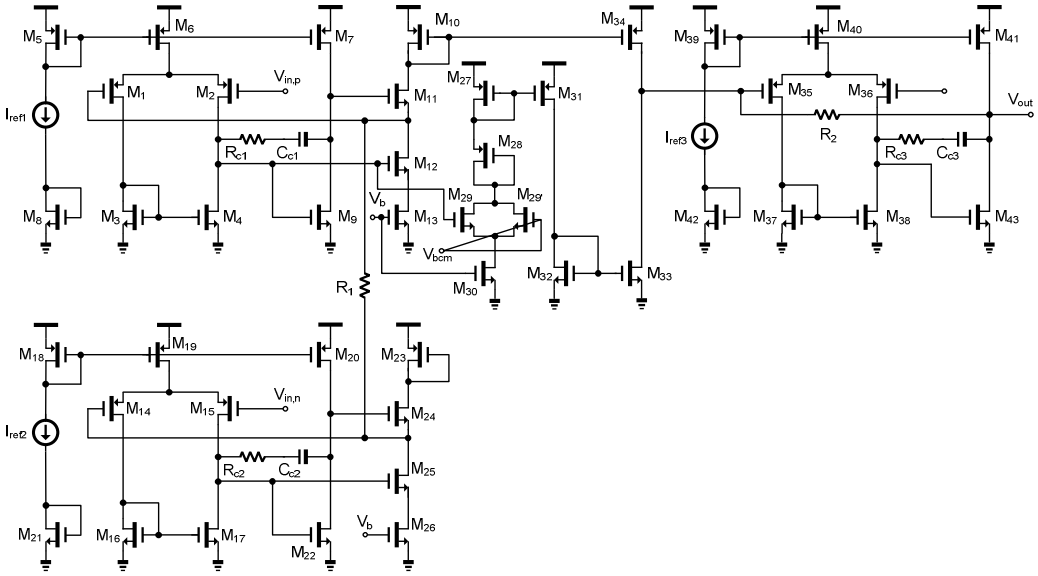

Fig. 3. Completed schematic of proposed CMIA

reach a high value, say, 92 dB in that case. Matching of integrated circuit implementation is much better than discrete one, so the CMRR is highly dependent on the accuracy of low power current mirrors.

Fig. 4 shows the schematics of current mirrors CM_1 (Fig. 4(a)) and CM_2 (Fig. 4 (b)). CM_1 is of the basic standard PMOS current mirror structure. Both transistors $M_{p,oa}$ and $M_{p,\ cm}$ operates in saturation region. Unlike CM_1, CM_2 copies the current with a zero-approaching ac component. Transistors $M_{n,ac}$ and $M_{n,dc}$ work in subthreshold regions. By using current division technique, this small ac component is copied separately from dc current by $M_{n,ac}$, which has a sufficient low transconductance g_m. The dc current is copied by $M_{n,dc}$ and further adjusted by transistors M_{c1} and M_{c2}. V_{bcm} is of the same DC voltage as V_{in}. It is noticed that the operation conditions of both current mirrors are different when the overall input voltage of the CMIA is fully differential or purely common mode. There is a tradeoff between the current mirrors' performance between the two different conditions. If the two input op amps are matched well, the poor CMRR is mainly due to the non-ideal characteristics of current mirrors under purely common mode input.

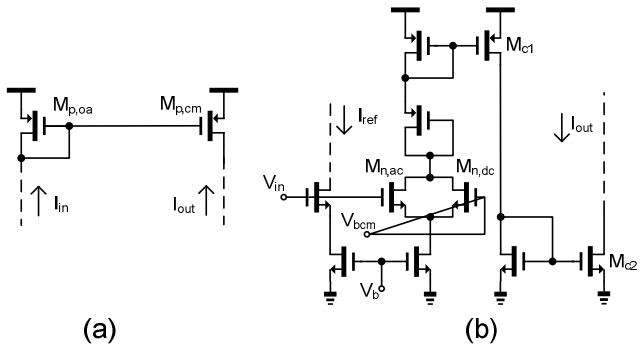

Fig. 4. Current Mirrors. (a) Schematic of CM_1. (b) Schematic of CM_2.

IV. Simulation Results

Fig. 5 shows the frequency response of CMIA and Fig. 6 shows the transient response to a 2 mV_{pp} differential input voltage. It is observed that the CMIA has GBW independent differential voltage gain whose value is precise adjusted via resistor R_2. The circuit has good THD value, i.e. 0.1% to a 2m V_{pp} differential input and 0.51% to a 5m V_{pp} differential input.

The CMRR performance is illustrated in Fig. 7. The CMIA achieves 120 dB CMRR up to 1 Hz. The most useful frequency band of biosignals for clinic practice is from 0.5 Hz to 100 Hz. The CMIA keeps a CMRR higher than 80 dB up to 100 Hz which satisfies the basic standard of medical instruments. It is not easy to have a wide band high CMRR with small current supply. The tradeoff between the current consumption and the bandwidth of CMRR should be concerned according to particular application requirement.

Fig. 8 shows the noise performance. For those applications concerning the signal band lower than 0.1 Hz, the chopping technique is required to further reduce the noise within this frequency band. Table III gives a summary of the simulation results.

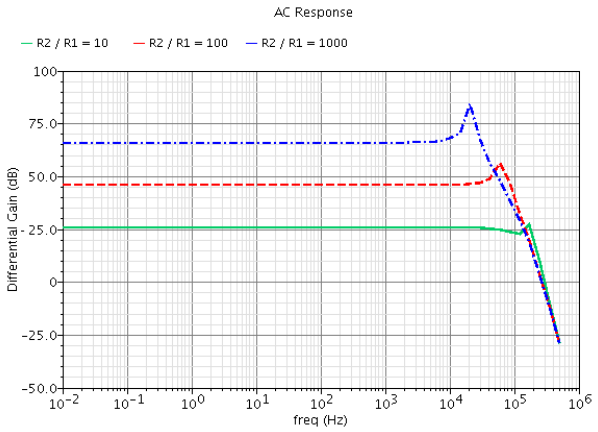

Fig. 5. Frequency response of the CMIA.

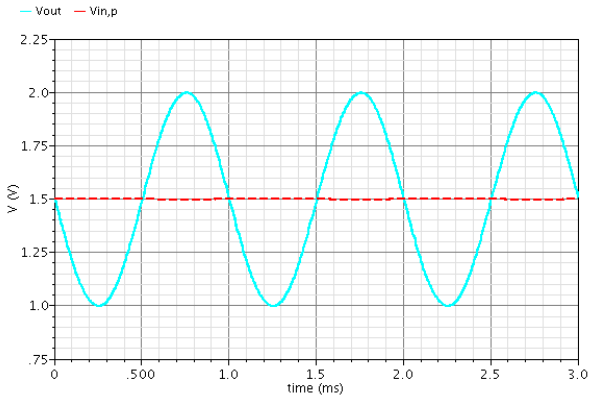

Fig. 6. Transient response to a 2m V_{pp} input differential voltage.

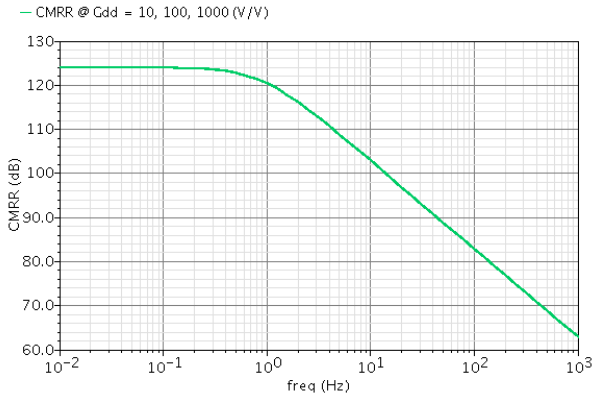

Fig. 7. CMRR frequency response.

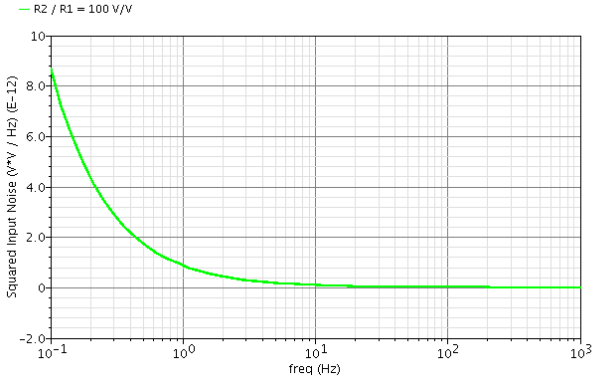

Fig. 8. Input noise voltage response.

TABLE III
PERFORMANCE SUMMARY OF PROPOSED CMIA

Supply Voltage	3 V
Power Consumption	20.22 µW
Continuous Gain Adjustment	Via R_2
Gain Bandwidth Product	260 KHz
Input referred Voltage Noise Density	170 nV_{rms} / √Hz
THD (@ 2m V_{pp})	0.1 %
THD (@ 5m V_{pp}	0.51 %
CMRR (below 1 Hz)	> 120 dB
CMRR (from 1 Hz to 100 Hz)	> 80 dB
CMOS Technology	0.35 µm

V. CONCLUSION

A current mode instrumentation amplifier using op amp power supply current sensing technique for portable biosignal acquisition system is implemented and analyzed in a CMOS 0.35µm technology. Simulation results show that the CMIA demonstrates continuous GBW-independent gain adjustment function and good signal distortion performance. The circuit has 120 dB CMRR up to 1 Hz and keeps a value higher than 80 dB up to 100 Hz. Chopping technique is required to further reduce input noise voltage lower than 0.1 Hz. The CMIA consumes only 20.22 µW under a 3 V dc supply voltage which is suitable for portable application.

The circuit does not require advanced op amp design but the matching between op amps plays an important role in layout phase. The accurate current mirror is the main challenge in schematic phase for higher CMRR and better signal quality.

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