A 0.4 V 6.4 µW 3.3 MHz CMOS Bootstrapped Relaxation Oscillator with ±0.71% Frequency Deviation over -30 to 100 °C for Wearable and Sensing Applications

Ka-Meng Lei [1,2], Pui-In Mak [1], R. P. Martins [1,3]

1 – State-Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macau, China
2 – Also with Harvard University, Cambridge, MA
3 – On leave from Instituto Superior Técnico, Universidade de Lisboa, Portugal
(E-mail: pimak@umac.mo)

***Abstract*—Wearable and sensing electronics are evolving towards energy harvesting from the environment (e.g. thermal and solar energy). Ultra-low-voltage (ULV) circuits that allow direct-powering by sub-0.5 V energy sources can maximize the power efficiency. This work is a 0.4 V 65 nm CMOS relaxation oscillator with bootstrapped logic gates and outputs. The bootstrapped logic gates enable an output swing of 1.15 V surmounting the adverse effect of ULV digital circuits without extra voltage source. The ULV comparator with bulk-driven-inputs shows an 18 dB gain with 3 cascaded stages. Also, featuring a background delay-time cancellation scheme, the 3.3 MHz relaxation oscillator with built-in calibration exhibits a frequency deviation of ±0.71% and ±0.57% against temperature (-30 to 100 °C) and voltage (0.36 to 0.44 V) variations, respectively, from Monte-Carlo simulations (N=30). The simulated power consumption is 6.4 µW, resulting in an energy efficiency of 1.9 pJ per cycle.**

Keywords—CMOS; relaxation oscillator (RxO); bootstrap; bulk-driven amplifier; ultra-low-voltage (ULV); wearable devices.

I. INTRODUCTION

The relaxation oscillator (RxO), which principle is to repetitively charge and discharge a capacitor and compare its voltage level, exhibits promising characteristics for oscillation in the kHz-to-MHz frequency (f_0). Unlike the crystal oscillator that requires an external crystal component, RxO supports full integration apt for wearable and sensing applications. Further, it is capable to provide a clock signal with relatively good stability against temperature and voltage variations, when compared with the inverter-based ring oscillator, as ideally f_0 only depends on the time constant (TC) of the RC-unit. Thus, it is apposite for utilization where extreme frequency stability (overall variation < 100 ppm) is not required, i.e. clock signal of the chopper and charge pump. There are multifarious RxOs reported [1-4]. Yet, they either required extensive calibrations to safeguard the frequency stability, or were designed for standard I/O voltages. As it is desired to power up the devices without battery to enhance the system's mobility, the existing topologies cannot be directly powered by the energy harvesting sources (e.g., solar and thermoelectric energy) with voltage of hundreds of mV [5-9]. This demands an additional voltage converter, impeding size and power miniaturization of the systems [10].

This paper proposes an ultra-low-voltage (ULV) RxO with V_{DD} down to 0.4 V, for self-powered wearable and sensing applications and prolonging its endurance. To circumvent this low V_{DD}, circuit techniques such as the bulk-driven amplifier and bootstrapped logic gates are applied to the RxO. Further, ascribed to the delays of the comparator and the digital circuits which emerge in a sub-0.5 V design and greatly degrades the frequency stability, the frequency against temperature and voltage variation is guaranteed by a t_{delay}-cancellation scheme in the background.

II. PROPOSED BOOTSTRAP RELAXATION OSCILLATOR

The proposed RxO is overviewed in Fig. 1(a). It consists of three modules: A) a swing-boosted RC-network with t_{delay}-cancellation to boost the voltage swing across the capacitor and soothe the frequency variation brought by the delay of the comparator and the logic gates; B) a comparator with bulk-driven first stage to accommodate the ULV design; C) Bootstrapped logic gates to enlarge the output swing and properly drive the switches. Their designs are detailed next.

A. Swing-Boosted RC-Networks with t_{delay}-Cancellation

The f_0 of an RxO is primarily determined by the charging and discharging time of the capacitor. The charge and discharge can be achieved either with an RC-unit [1, 2] or a constant current source [3,4]. Generally, a delicately designed current source and voltage reference can offer an excellent temperature and voltage stability of the f_0 [11]. Yet, it is challenging to implement a current reference with low temperature coefficient for V_{DD}<0.5 V. Thus, an RC-unit circumventing voltage and current regulation and insensitive to V_{DD} fluctuation is chosen as the charge/discharge module in this ULV design. To tackle the low-voltage swing on the capacitor, a differential swing-boosting scheme is adopted here [1]. This act not only offers a differential charge/discharge signal, but also boosts up the voltage swing on the capacitors, improving the performance of the RxO.

Ideally, f_0 only depends on the TC of the RC-unit. For the swing-boosting scheme, f_0 is equal to $1/2RC\ln(3)$. Yet, the delay between the crossing on the signals of the capacitors and the actual switching of the *CLK* (t_{delay}), which is attributed to the delay of the comparator, buffers, and the ensuing logic gates, accrues an error on f_0 [Fig. 1(b)]. To achieve sub-0.5 V operation, t_{delay} may contribute with a considerable error to the

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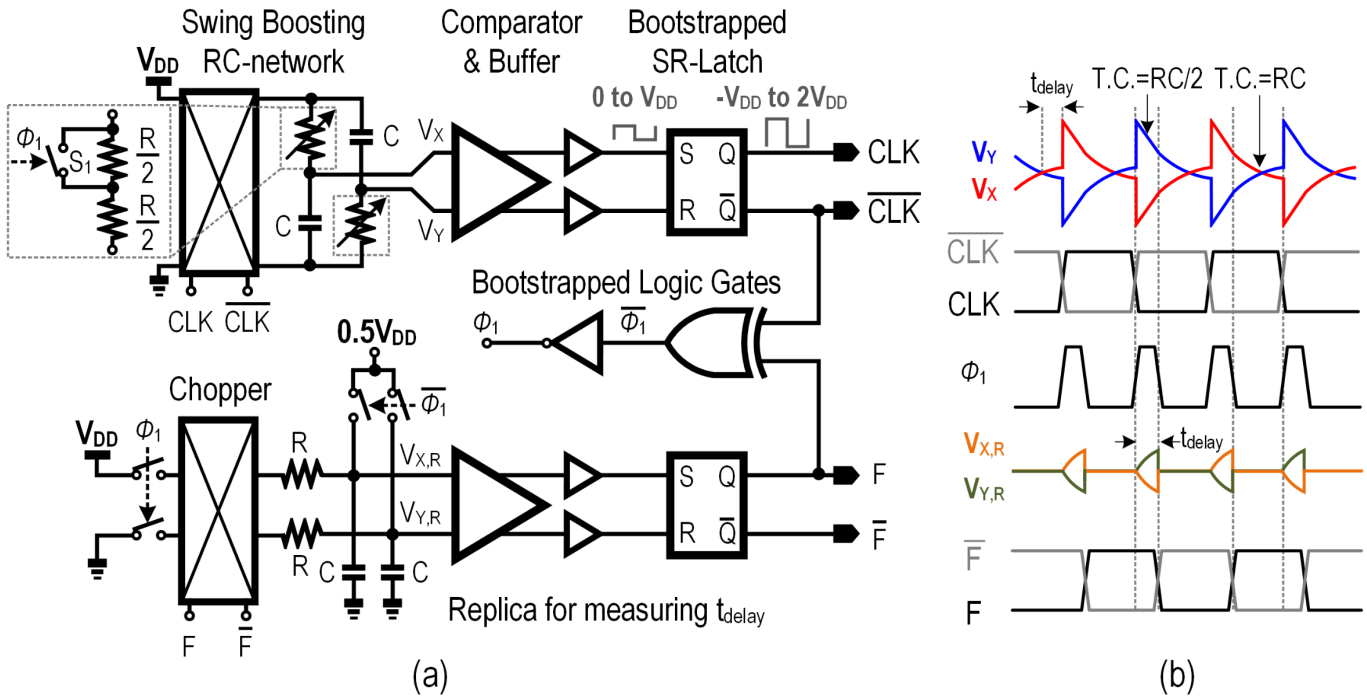

Fig. 1 Proposed RxO. (a) Schematic. (b) Timing diagram.

system. More importantly, t_{delay} is PVT-sensitive which exacerbates the variation of f_0. To this end, a t_{delay}-replica is employed to cancel this effect [3]. Like the main branch, the replica has an identical comparator, buffers and logic gates, thus it can duplicate t_{delay} against PVT variations. When Φ_1=0, both capacitors of the replica are discharged to $0.5V_{DD}$. When transition on *CLK* happens, Φ_1 goes high and $V_{X,R}$ ($V_{Y,R}$) starts to charge to V_{DD} (ground). Meanwhile, V_X and V_Y from the main branch charge with half the nominal TC *RC*/2. The output of the replica (*F*) will be flipped after t_{delay} driving Φ_1 to the low level again. Thus, the period of the RxO is balanced and compensated even with the inevitable t_{delay}.

B. ULV Comparator with a Bulk-Driven Input Stage

The comparator of the RxO should be implemented with fully-differential architecture to resist external noise (i.e., EMI and power supply noise). A critical design criterion of the comparator, especially for the sub-0.5 V circuit, is the common-mode (CM) input voltage, which is only half V_{DD} (0.2 V) here. Such low input voltages from the RC-networks hinder the use of the typical differential amplifier, where V_X and V_Y are applied to the gate of the input pair. Herein, a differential amplifier with bulk-driven input pair ($M_{1,2}$) is adopted as the input stage of the comparator [12] (Fig. 2). This bulk-driven amplifier can tolerate a wide input CM level, at the expense of a lower gain and noisier output. The input signals are applied to the body of $M_{1,2}$ ($V_{in,P}$ and $V_{in,N}$). Since the V_{GS} of the transistors is less sensitive to the bulk voltage when compared with the gate voltage, this bulk-driven amplifier can be operated with a flexible input CM voltage. The bias current of the amplifier is controlled by V_{BIAS}, which is generated by the current mirror with current I_{BIAS}. Consequently, the gate of $M_{1,2}$ is biased by V_{CM}, which is expressed as:

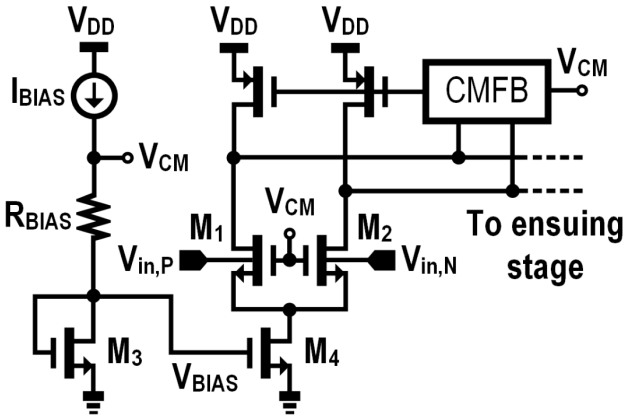

Fig. 2 Schematic of the bulk-driven amplifier as the input stage of the ULV comparator.

$$V_{CM} = V_{BIAS} + I_{BIAS}R_{BIAS} \quad (1)$$

From (1), V_{CM} is directly proportional to V_{BIAS}, with an offset of $I_{BIAS}R_{BIAS}$. The offset here determines the bias point for $M_{1,2}$ thus the operating headroom of M_4 ($V_{DS,4}$). This links V_{CM} with V_{BIAS}, and assures a proper bias condition of the amplifier against PVT variations. The PMOS loads of the amplifier are driven by the common-mode feedback (CMFB) circuit, which is set to provide an output level of V_{CM}. Again, this safeguards $M_{1,2}$ operating in the subthreshold region as $V_{GD}<V_{TH}$ for all conditions. The output of this bulk-driven amplifier will be applied to the ensuing amplifier with typical gate-driven input which provides a higher gain. Further, the input CM voltage of the subsequent stage is also pinned to the output CM voltage of the previous stage, ensuring the bias condition of the whole comparator. In this design, 3 amplifying stages are cascaded to provide a total gain of 18 dB (unity gain bandwidth: 77 MHz).

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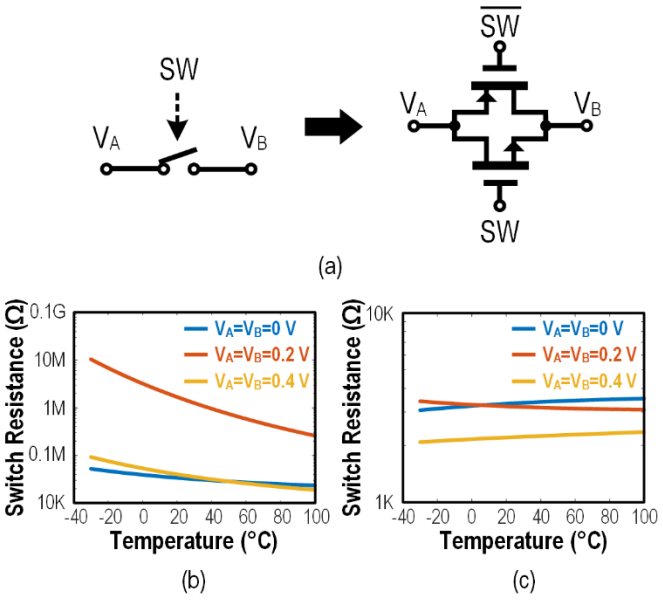

Fig. 3 (a) A switch and its schematic. (b) On-resistance of the switch against temperature with typical driving voltage (0.4 V/0 V for SW/$\overline{SW}$). (c) On-resistance of the switch against temperature with boosted driving voltage from the bootstrapped output (0.8 V/-0.4 V for SW/$\overline{SW}$).

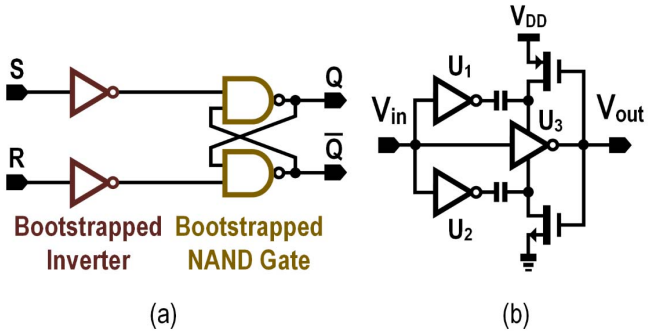

Fig. 4 (a) Bootstrapped SR-latch. (b) Circuit diagram of the bootstrapped inverter.

C. Bootstrapped Output and Logic Gates

After the signals have been amplified to a sufficient level, they are connected to the logic gates for providing a digital output signal and driving the switches and logic gates within the RxO. Yet, for V_{DD}=0.4 V, the complementary switch formed by NMOS and PMOS [Fig. 3(a)] with typical size (W_n/L_n: 200 nm/60 nm, W_p/L_p: 800 nm/60 nm) and driving voltage (0.4 V/0 V for $SW/\overline{SW}$) has a large on-resistance (R_{ON}). Illustrated in Fig. 3(b), R_{ON} can reach up to 10 MΩ with temperature of -30 °C and V_A=V_B=0.2 V. Also, its value can change above an order of magnitude from -30 to 100 °C attributed to the low overdrive voltage. This degrades the performance of the overall RxO. For instance, when Φ_1 goes high, S_1 (in Fig. 1) should be closed and have an ideal R_{ON} of 0 Ω, charging the capacitors with a TC of $RC/2$. Yet, the non-zero R_{ON} affects the charging TC, which is changed to $[(R_{ON} + 0.5R)C]$. If the magnitude of R_{ON} is comparable to R, f_0 is altered and deteriorated in terms of stability against PVT variations.

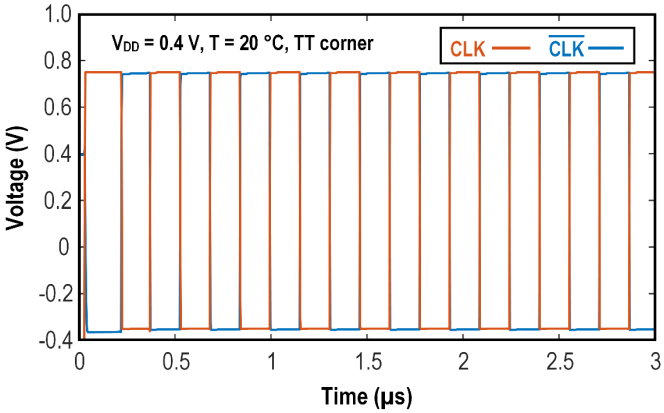

Fig. 5 Simulated output waveforms of the RxO.

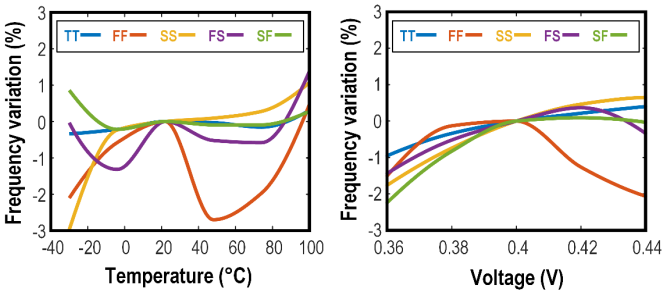

Fig. 6 Frequency deviation of the RxO at different process corner against (a) temperature and (b) supply voltage referenced to 20 °C and 0.4 V respectively.

While the typical logic gates only offer an output voltage level between ground and V_{DD}, a bootstrapped logic gate can deliver an output voltage between -V_{DD} and 2V_{DD} [13]. Such large voltage swing is advantageous for driving the switches and logic gates, as well as other external circuit blocks. The SR-latch which guarantees an output signal with a duty cycle ~50% is implemented with bootstrapped logic gates and illustrated in Fig. 4(a). The schematic of the bootstrapped inverter is revealed in Fig. 4(b). Other bootstrapped logic gates (XOR and NAND) have similar structures, with the core logic elements $U_{1\text{-}3}$ replaced by the corresponding logic elements. With a driving voltage of 0.8 V/-0.4 V for SW/$\overline{SW}$, the R_{ON} of the switch is greatly reduced. It is <4kΩ with V_A=V_B between 0 V and 0.4 V and temperature from -30 °C to 100 °C, which is much smaller than R (~400 kΩ) [Fig. 3(b)]. The variation of R_{ON} originated from temperature variation is also reduced to <14% ascribed to the larger overdrive voltage.

III. Simulation Results

The proposed 0.4 V RxO is designed and simulated in 65 nm CMOS with all circuit components implemented with practical on-chip elements. The designed f_0 of the RxO is 3.3 MHz. The simulated outputs of the RxO are revealed in Fig. 5. At 0.4 V, the RxO is capable to deliver a differential output swing of 1.15 V on each output ($CLK/\overline{CLK}$), benefitting from

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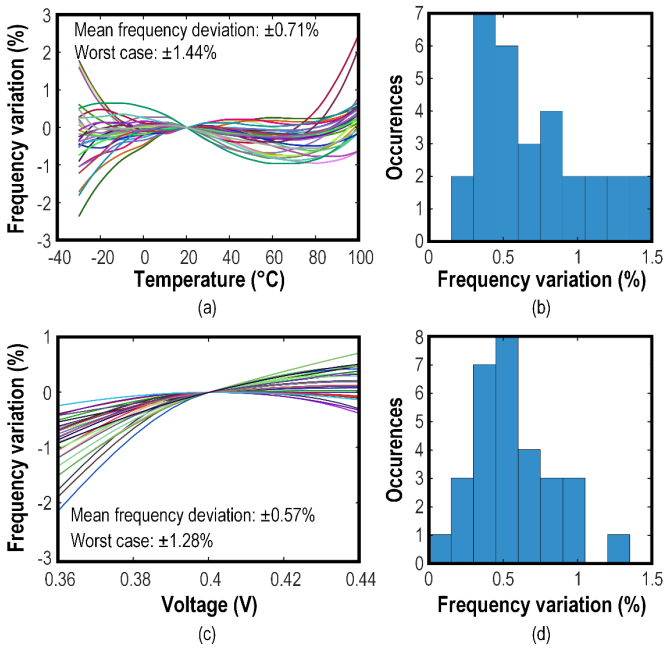

Fig. 7 (a) Monte-Carlo simulation (N=30) of the f_0 deviation against temperature variation from -30 to 100 °C referenced to 20 °C. (b) Histogram of the corresponding f_0 variation from (a). (c) Monte-Carlo simulation (N=30) of the f_0 deviation against V_{DD} variation from 0.36 to 0.44 V referenced to 0.4 V. (d) Histogram of the corresponding f_0 variation from (c).

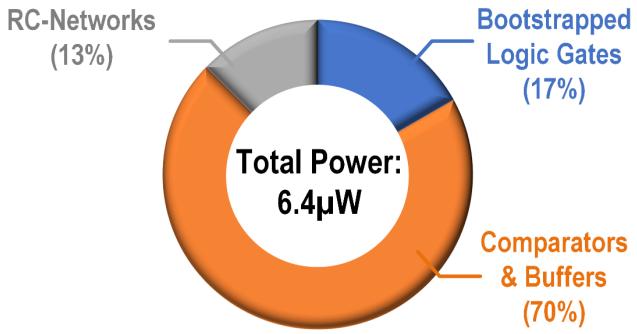

Fig. 8 Power consumption and its breakdown of the proposed RxO.

the bootstrapped logic gates. The swing is smaller than the theoretical $3V_{DD}$ due to the charge-sharing effect, which can be improved by enlarging the bootstrap capacitors [13]. The duty-cycle of the output is 49.2%. The RxO can be immediately started after enabling it with a single cycle to compensate the t_{delay} error [3].

The process corner has a large effect on f_0 (as much as ±50%), which is anticipated by the variation on the RC-unit that is not compensated. This process variation can be improved with a single trimming after fabrication. Fig. 6(a) and (b) plot the f_0 deviation attributed to temperature and voltage variations. With TT corner the deviations on f_0 caused by temperature (-30 to 100 °C) and voltage (0.36 to 0.44 V) variation are restrained to ±0.3% and ±0.7%, respectively. The performances are worsened with different process corners. To characterize the performance of the RxO with the presence of process variation as well as the mismatch between the devices, Monte-Carlo simulations with 30 iterations was performed [Fig. 7(a)-(d)].

TABLE I.
SUMMARY AND PERFOMANCE COMPARISONS.

	This work*	ISSCC '16 [1]	VLSI '12 [3]	A-SSCC '13 [4]
Technology (nm)	65	180	90	40
V_{DD} (V)	**0.4**	1.4	0.8	3.4/0.85
Frequency (MHz)	3.3	10.5	0.1	10
Power (µW)	6.4	219.8	0.28	20
Variation with Temp.	**Avg. ±0.71% (N=30) @ -30 to 100 °C**	137 ppm/°C @ -40 to 125 °C	±0.68% @ -40 to 90 °C	N/A
Variation with V_{DD}	**Avg. ±0.57% (N=30) @ 0.36 to 0.44 V**	0.44%/0.1 V @ 1.4 to 2 V	±0.82% @ 0.725 to 0.9 V	1.1% @3-4.1 V
Energy per cycle (pJ)	**1.9**	20.9	2.8	2
Calibration	**Built-in**	No	Built-in	Built-in

*Simulation Results

The mean f_0 deviation across -30 to 100 °C is ±0.71%, with a worst case of ±1.44%. Similarly, the mean f_0 deviation across V_{DD} of 0.36 V to 0.44 V is ±0.57%, with a worst case of ±1.28%.

The RxO consumes 6.4 µW, corresponding to an energy efficiency (i.e. power/frequency) of 1.9 pJ per cycle. Most of the power (70%) is consumed by the comparators and buffers since three cascaded stages are entailed to compensate the low gain from the bulk-driven input stage, as illustrated in Fig. 8. The RMS cycle-to-cycle jitter and long-term jitter are 44.4 ps and 399 ps respectively (from 100 Hz to 100 kHz).

Table I summarizes the performances of the RxO and benchmarks it with recent arts. This work successfully implemented an RxO at an ULV V_{DD} of 0.4 V, by exploiting a comparator with bulk-driven input stage and bootstrapped logic gates, while achieving a comparable f_0 stability against temperature and voltage variations. The frequency stabilization is achieved in the background continuously, lowering the complexity and enhancing the autonomy of the RxO.

IV. CONCLUSIONS

This paper proposed a 0.4 V 6.4 µW 3.3 MHz CMOS RxO in 65 nm CMOS. To confront with the ULV supply, a swing-boosted RC-network and an ULV comparator with bulk-driven input stage are employed, enabling a high voltage swing across the capacitors, and ensuring the functionality of the comparator even at a 0.2 V input CM voltage. The bootstrapped logic gates boost the output swing to 1.15 V, and facilitate the driving of the logic gates and switches. Further, a t_{delay}-cancellation scheme alleviates the delay time of the comparator and logic gates, by duplicating the t_{delay} and raise the charging speed of the RC-network correspondingly. From Monte-Carlo simulations (N=30), our RxO achieves f_0 deviations of ±0.71% and ±0.57% against temperature and voltage variations, respectively. The energy efficiency is 1.9 pJ per cycle. These results render our RxO as a promising clock solution with moderate precision for low-voltage wearable devices directly powered by energy-harvesting sources.

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