A LOW-IF/ZERO-IF RECONFIGURABLE RECEIVER WITH TWO-STEP CHANNEL SELECTION TECHNIQUE FOR MULTISTANDARD APPLICATIONS

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ABSTRACT

This paper presents a low-IF/zero-IF reconfigurable receiver for multistandard applications based on a two-step channel selection (2-SCS) technique. Such technique is mainly implemented by a reconfigurable sampling scheme, which can perform either programmable Analog-Double Quadrature Sampling (A-DQS) or Analog-Baseband Sampling (A-BS) to, first relax the front-end PLL-frequency synthesizer (PLL-FS) locking time and phase noise requirements, and second allow a low-IF architecture to be transformable to a zero-IF one with small overheads. In this way, the receiver can operate in low-IF mode for narrowband standards avoiding 1/*f* noise and DC offset, and alternatively, for wideband ones it can be reconfigured seamlessly in zero-IF mode to minimize image interference. The operating principles, design considerations and circuit implementation of such scheme for multistandard applications, that include Bluetooth, HomeRF and IEEE 802.11FH, will demonstrate the flexibility of such topology.

1. INTRODUCTION

The high discrepancy in frequency band locations and channel bandwidths of distinct communication standards drives the design of multistandard transceivers into a tremendous challenge. Recently reported receiver analog front-ends (AFEs) utilize simple zero-IF (direct-conversion) architecture to support the GSM with WCDMA and DECT [1] or GSM, DCS, PCS with WCDMA [2]. Such approach is appropriate for solving image problem and highly matches WCDMA and DECT standards, given that their channel bandwidths are relatively large, thus relatively insusceptible to 1/*f* noise and DC offset corruptions. Differently, in narrowband GSM-like applications, impractical ac-coupling circuit (for example) will be mandated to eliminate 1/*f* noise and DC-offset while still keeping low bit error rate (BER). In general, low-IF receiver is more appropriate for narrowband applications like GSM [3]. Therefore, very recent research work starts to propose dual-mode transceiver to process IEEE 802.11b WLANs (wideband) in zero-IF mode, and low-IF mode for Bluetooth (narrowband) [4]. A remaining imperfection in such architecture is related with the utilization of a fractional-*N* PLL frequency synthesizer (PLL-FS), instead of a simple integer-*N* one, to perform the channel selection. It is well-known that fractional-*N* PLL-FS suffers from the serious fractional spurs problem, when the synthesized division ratio is close to an integer multiple of the phase detector frequency [5].

This paper proposes a novel low-IF/zero-IF reconfigurable receiver as shown in Fig. 1, which embed the recently proposed 2-SCS technique [6] to allow the relaxation of phase noise and settling time requirements of the PLL-FS through partitioning the channel selection from the RF-AFE to the IF one. Thus, channel selection can be accomplished corporately by a simple integer-*N* PLL-FS (step-1) and the proposed reconfigurable IF-sampling

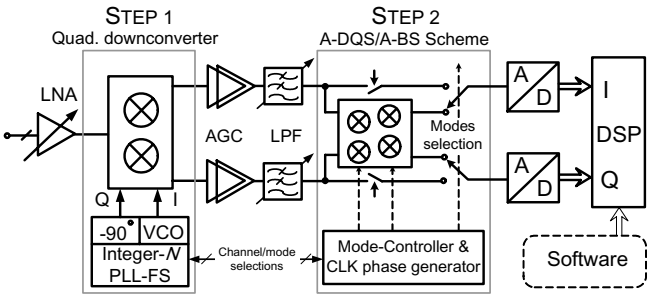


Fig. 1. Proposed low-IF/zero-IF reconfigurable receiver.

scheme (step-2). Such scheme can perform either A-DQS in low-IF mode for both frequency downconversion [7] and IF channel-selection [6], or simply A-BS in zero-IF mode.

2. 2-SCS TECHNIQUE FOR LOW- AND ZERO-IF MODES

2.1. Low-IF mode

Fig. 2(a)-(g) show the hierarchical spectra-flow illustrations of the proposed receiver that is shown in Fig. 1. Starting from Fig. 2(a), suppose that the pre-selected RF input, $x_{RF}(t)$, consists of a couple of in-band channels (labeled C_N, C_{N+1}, C_{N+2} and C_{N+3}, for $N=1, 2, 3\ldots$) which are firstly amplified by a low noise amplifier (LNA). Then, assuming that the desired radio channels at this step are C_N and C_{N+1} **(STEP-1 OF 2-SCS)**

$$x_{RF}(t) = C_N(t)\cos[2\pi f_N t + \varphi_N(t)] + C_{N+1}(t)\cos[2\pi f_{N+1} t + \varphi_{N+1}(t)] + C_{N+2}\cdots \quad (1)$$

In this downconversion, the possible local oscillator (LO) frequency f_{LO} is selected from the *two* channels bandwidth as,

$$f_{LO} = \frac{f_N + f_{N+1}}{2} \qquad N = 1,3,5,... \quad (2)$$

which imposes the selected IF corresponds to half-channel spacing, $f_{IF}=(f_{N+1} - f_N)/2$, and also implying channel C_N will be the image of C_{N+1} or vice versa [Fig. 2(b)]. After lower sideband frequency downconversion, channels C_N (located at $-f_{IF}$) and C_{N+1} (located at f_{IF}) will be filtered by the channel-select lowpass filters (LPFs) and properly amplified by G_{AGC} through the automatic gain control (AGC) block (the bandwidth of the filter is designed to be tunable, as it will be shared with zero-IF mode in wideband applications). After those mentioned operations, the $x_{IF}(t)$, expressed in in-phase (I) and quadrature (Q), is obtained

$$x_{IF}(t) = x_I(t) + jx_Q(t) = G_{AGC} \cdot LPF\{x_{RF}(t)e^{-j2\pi f_{LO}t}\} \quad (3)$$

Next, the $x_{IF}(t)$ as shown in Fig. 2(c), will face a controllable A-DQS operation **(STEP-2 OF 2-SCS)** that will result in an either forward (FS) or backward (BS) frequency shifting as illustrated in Fig. 2(d). These two complex sampling spectra can be described with the help of the A-DQS model, and their time- and frequency-

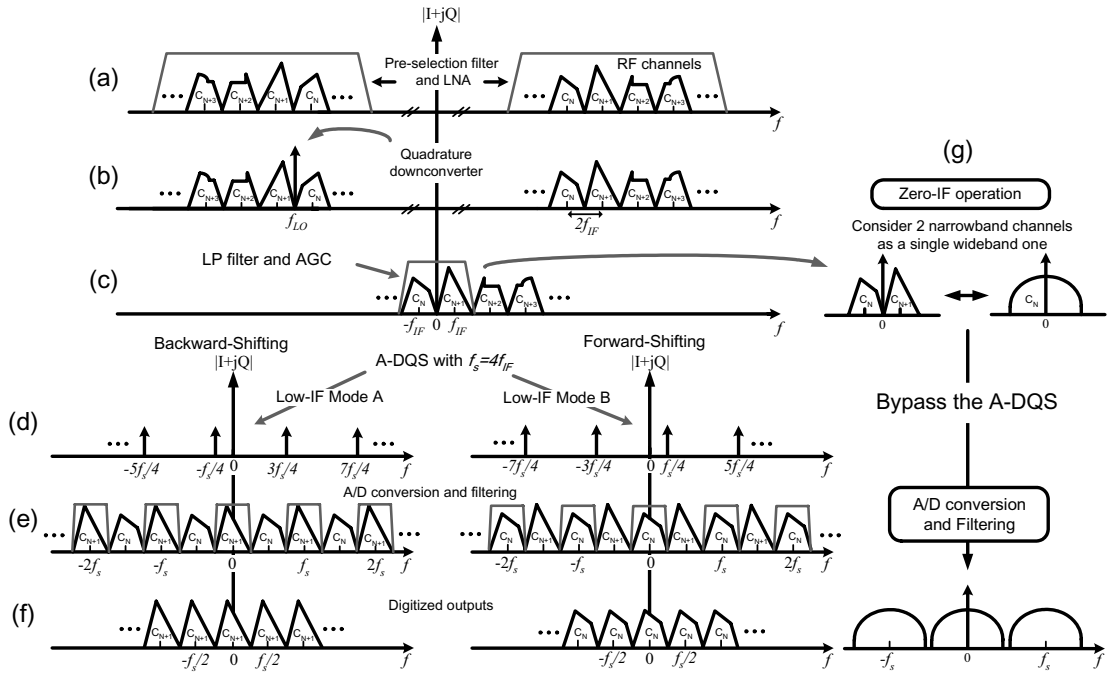


Fig. 2(a)-(g). Hierarchical spectra-flow illustration of the proposed receiver in low-IF mode **A** and **B**, and zero-IF one.

domain illustrations are shown in Fig. 3(a)-(b). The inputs $x_I(t)$ and $x_Q(t)$ are sampled by $P_I(t)$ and $P_Q(t)$[‡] with sampling frequency f_s $(1/T_s)$ equals to four times the f_{IF} to simplify the mixing to integer-weighted sampling [$\cos(n\pi/2)$=1, 0, -1, 0 and $\pm\sin(n\pi/2)$=0, 1, 0, -1 or 0, -1, 0, 1 for $n=0, 1, 2...$] as given by

$$\begin{aligned} P(t) &= P_I(t) + jP_Q(t) \\ &= \sum_{n=-\infty}^{\infty} [\delta(t-nT_s) - \delta(t-nT_s-T_s/2)] + \\ &\quad j\sum_{n=-\infty}^{\infty} [\pm\delta(t-nT_s-T_s/4) \mp \delta(t-nT_s+T_s/4)] \end{aligned} \tag{4}$$

and taking the Fourier transform of $P(t)$, it will lead to

$$\begin{aligned} P(j\omega) &= \sum_{k=-\infty}^{\infty} 2\pi\, a_k \delta(\omega - k\omega_{IF}) + j\sum_{k=-\infty}^{\infty} 2\pi\, b_k \delta(\omega - k\omega_{IF}) \\ &= \sum_{k=-\infty}^{\infty} 2\pi\, c_k \delta(\omega - k\omega_{IF}) \end{aligned} \tag{5}$$

$$a_k = \begin{cases} \frac{2}{T} & \text{for } k = 2n+1 \\ 0 & \text{otherwise} \end{cases}, \quad b_k = \begin{cases} \frac{2}{T} e^{\mp jk\pi/2} & \text{for } k = 2n+1 \\ 0 & \text{otherwise} \end{cases}$$

$$\begin{aligned} c_k &= a_k + jb_k \\ &= \begin{cases} 4/T & \text{for } k = 4n \pm 1 \\ 0 & \text{otherwise} \end{cases} \qquad for \quad n = 0, \pm1, \pm2, ... \end{aligned} \tag{6a-c}$$

where a_k and b_k are the real Fourier coefficients, whereas c_k is the corresponding complex sum (with $\omega_s=2\pi f_s$). Those expressions are equivalent to the sampling spectra shown in Fig. 2(d) [also Fig. 3(a) and (b)]. As a result, the output $y(nT)$ is multiplied by a controllable complex term, $\cos(n\pi/2)\pm j\sin(n\pi/2)$ for $n=0, 1, 2...$ leading to the sampled-output as given by [Fig. 2(e)]

$$\begin{aligned} y(nT) &= [x_I(nT)\cos(n\pi/2) \mp x_Q(nT)\sin(n\pi/2)] \\ &\quad + j[x_Q(nT)\cos(n\pi/2) \pm x_I(nT)\sin(n\pi/2)] \end{aligned} \tag{7}$$

In other words, A-DQS selectively downconverts either the desired channel or its adjacent one (image) to the baseband in a discrete-time mixing approach. In low-IF mode **A**, channel C_{N+1} is obtained at $\pm nf_s$ for $n=0, 1, 2...$whereas channel C_N (image of C_{N+1}) is shifted to $\pm nf_s/2$ for $n=1, 3, 5...$ Similar results could be obtained for forward shifting in low-IF mode **B**, in which the role of channel C_{N+1} and C_N are reversed. Both cases do not suffer from the problematic DC offset and 1/f noise, since they are now shifted to $\pm nf_s/4$, for $n=1, 3, 5....$ Then, the $y(nT)$ can be digitized by two Nyquist A/D converters. The final I and Q data at a rate $f_s/2$ can be obtained after digital filtering and decimation by two, as shown in Fig. 2(e) and (f) respectively. This demonstrates the entire channel selection approach in both low-IF mode **A** and **B**.

2.2. Zero-IF mode

In zero-IF mode, two narrowband channels will be considered as one wideband channel, as shown in Fig. 2(g), which means that the LO's frequency are selected with the same frequency value of the channels' carrier (i.e., a zero-IF operation). As a result, the mixers, AGCs, lowpass filters and A/D converters can all be reused in both modes. Only the A-DQS operation is replaced by the A-BS one as shown in Fig. 3(c), which is a nominal sampling with the deactivation of $P_Q(t)$. Therefore, after sampling and A/D conversion, the desired channel is at DC for both low and zero-IF modes. The succeeding decimation, zero-IF [8] or coherent demodulations can be implemented in the DSP to allow programmability by software, and low-cost implementation in CMOS.

3. DESIGN CONSIDERATIONS AND IMPROVEMENTS

Some imperative design considerations will be addressed to quantify the improvements and practicability of the proposed receiver, especially in multistandard applications. The standards considered here are IEEE 802.11FH, Bluetooth and HomeRF, as briefly summarized in Table 1.

[‡]For forward FS consider the equations (4, 6a-c and 7) with the upper sign whereas the lower sign corresponds to backward FS.

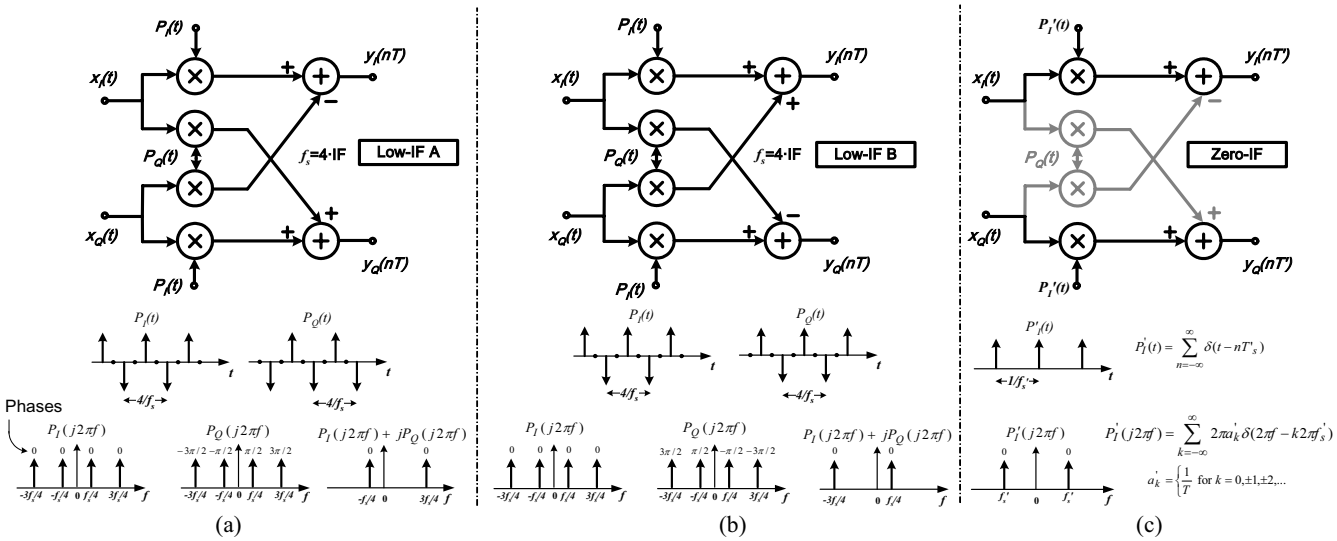


Fig. 3. A-DQS and A-BS models and their corresponding time- and frequency-domain illustrations. (a) A-DQS in low-IF mode-**A**. (b) A-DQS in low-IF mode-**B**. (c) A-BS in zero-IF mode.

Obviously, the RF-AFE including the antenna, pre-selection filter, LNA, LO, mixers and AGCs can be all shared as they all operate in the same frequency band. Moreover, A/D converters with sampling frequency greater than 10 MHz can be utilized for digitization. The main design challenges would be related with the design of the channel-select filter and the PLL-FS, as the channel spacing ranges from 1 MHz to 5 MHz and frequency-hopping operation requires fast settling of the PLL. By utilizing the proposed receiver architecture in low-IF mode for Bluetooth and IEEE 802.11FH, and in zero-IF mode for HomeRF, two significant improvements can be observed.

1. Simplified channel-select filter design - for Bluetooth and 802.11FH, the sought channel is downconverted to IF=0.5 MHz first, whereas the IF is set to zero for HomeRF. Thus, the required image-rejection and power dissipation of the blocks that will follow the filter would be minimized. Moreover, the original required bandpass or complex bandpass channel-select filter could be replaced by a simple ac-coupling circuit cascading with a baseband lowpass filter, which has a cut-off frequency range from 1 to 5 MHz. This structure balances better the design trade-offs between channel selection, and 1/*f* noise and DC-offset eliminations in low-IF modes as the desired channel is not directly corrupted by them.

2. Improved performances of the front-end PLL-FS - the benefit is indeed exhibited by the characteristics of the RF-FS, presented in Fig. 4(a). The circumstances of channel selection are compared in Fig. 4(b) and 4(c) for low- and zero-IF modes, respectively. In low-IF mode, Fig. 4(b) shows that the step-size of the FS is doubled, and therefore if a type-II integer-*N* PLL-FS is used for channel selection, the reference frequency that must be equal to the step-size can also be doubled, while the division ratio (named as modulus) in the PLL-FS is halved. As a result, the reference frequency can be doubled to reduce the PLL settling time by 50%, to enlarge the loop bandwidth of the PLL, to suppress the voltage control oscillator (VCO) phase noise and increase the damping ratio of the PLL to improve the stability. Moreover, considering that the division ratio is proportional to the close-in phase noise, halving the division ratio also reduces the power of the close-in phase noise by a factor of 4 and simplifies the frequency divider structure as it only has halved number of locking positions [5]. Conversely, in zero-IF mode for HomeRF [Fig. 4(c)], only a simple 2/5 frequency divider is needed in between the phase-frequency detector (PFD) and the modulus to match with the 2-MHz reference frequency.

Table 1. Brief summary of certain 2.4-GHz ISM band standards.

Standard	Multiple Access	Frequency range	Channel spacing	Modulation scheme	Data rate
802.11FH	FHSS	2.4GHz	1MHz	GFSK	1,2Mbps
Bluetooth	FHSS	2.4GHz	1MHz	GFSK	1Mbps
HomeRF	FHSS	2.4GHz	5MHz	GFSK	5,10Mbps

4. IMPLEMENTATION OF THE A-DQS/A-BS SCHEME

The A-DQS/A-BS scheme is the key functional block to implement the proposed receiver. Following the principles and proposed application requirements, the topology of the entire scheme is illustrated in Fig. 5(a). It can be observed that when the receiver operates in low-IF modes **A** and **B**, alternating the sampling sequences between *2* and *4* is needed to obtain either the upper- or lower- sidebands in A-DQS operation. Moreover, the A-DQS also requires differential circuit implementation to provide both positive and negative input values. Fig. 5(b) shows the circuit implementation of the A-DQS/A-BS scheme, which can be elegantly embedded in a sample-and-hold (S/H) pair. The operation of changing the sampling sequence between clock phases *2* and *4*, and the function of mode selection, are performed by a 2-bit-input digital controller [Fig. 5(c)], that allows the definition of the three operation modes: A-DQS operation for low-

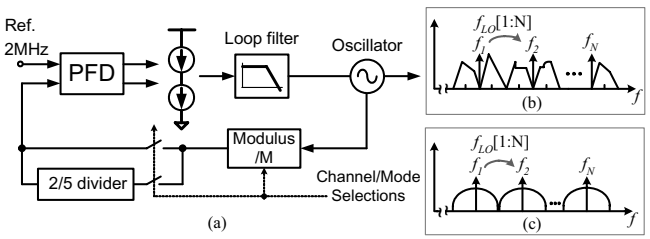
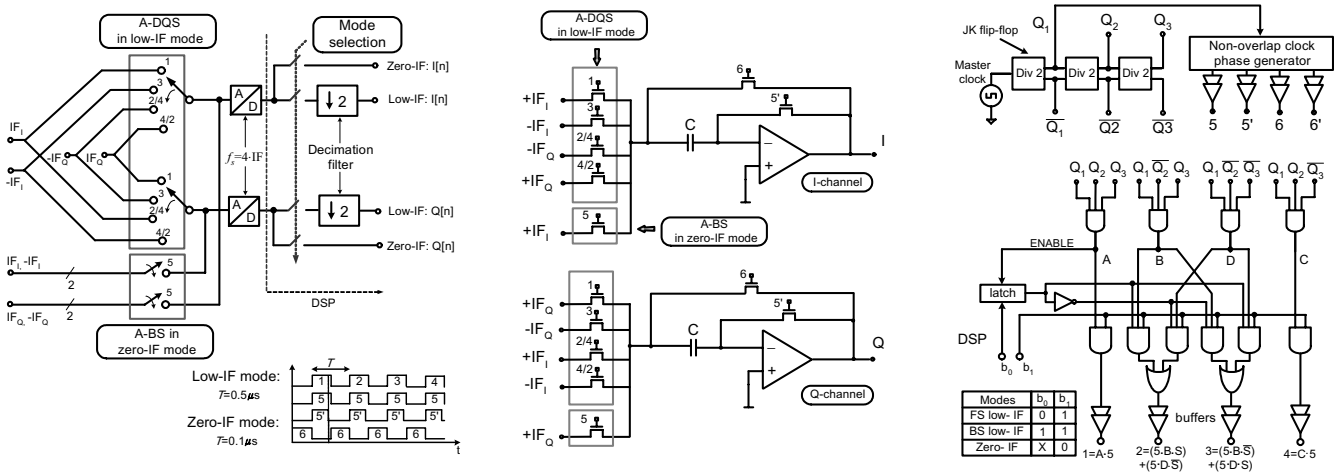


Fig. 4. (a) Proposed dual-mode integer-*N* PLL-FS. (b) Locking positions of the LO in low-IF mode (c) and in zero-IF mode.



(a) (b) (c)

Fig. 5. A-DQS/A-BS scheme. (a) Topology. (b) Single-ended schematic. (c) Channel/mode selections embedded clock phase generator.

IF modes **A** and **B**, and A-BS for zero-IF. Such controller is embedded in the clock phase generator, thus the channel selection can be enabled in every phase *A* [Fig. 5(c)], thus leading to the necessary time for channel selection comprising only four sampling periods. Moreover, since channel selection acts in the control paths only, it results no transient effect over the signal paths. Such advantageous features are not possible to obtain in conventional continuous-time mixing approaches.

For simplicity, only the simulation result of A-DQS for low-IF mode **B** will be presented. The simulated complex Fast Fourier transform – FFT $|I+jQ|$ is shown in Fig. 6. To verify the functionality, a 1-MHz single tone is applied to the S/H, which works with f_s=10 MHz. Such input actually can be considered as one positive 1-MHz and one negative 1-MHz tones in the two-sided spectrum. Thus, after being sampled and frequency shifted by the A-DQS S/H, those tones will be frequency shifted by 2.5 MHz ($f_s/4$), and they will be located at $\pm nf_s$ + (1+2.5) MHz and $\pm nf_s$ + (-1+2.5) MHz for *n=1, 2, 3*...The attenuation in their magnitudes is due to the *sinc* response of the S/H.

Due to the complex nature of the A-DQS, the other performances are characterized in A-BS mode. The THD counted up to the 5th harmonics is close to –68.6 dB with 1-V_{pp} full-scale. The SFDR is 73.2 dB. The image rejection ratios (IRRs) achieve 41 dB, 50 dB, 76 dB for 2% gain, 0.5° phase and 2% capacitance mismatches between the *I* and *Q* channels, respectively [9].

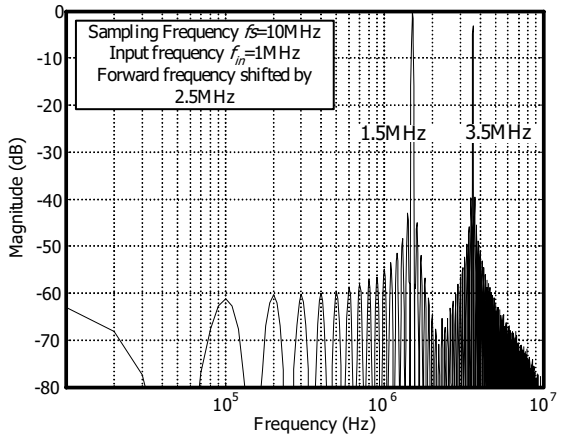


Fig. 6. Simulated complex FFT $|I+jQ|$.

5. CONCLUSION

A novel low-IF/zero-IF reconfigurable receiver architecture has been proposed for narrowband/wideband-mixed multistandard systems. Such architecture embedded a 2-SCS technique implemented by a digital-control A-DQS/A-BS scheme. The overheads are simple digital circuitry and analog switches associated in the S/H circuits of the A/D converters. However, most of the functional blocks in the receiver chain can be fully reused for both low- and zero-IF modes, while the A/D conversion and demodulation is still keep at DC in both modes. Moreover, such 2-SCS technique also significantly relaxes the PLL-FS phase noise and settling time requirements by partitioning the channel selection from the RF-AFE to the IF one.

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REFERENCES

[1] X. Li and M. Ismail, "A single-chip CMOS front-end receiver architecture for multistandard wireless applications," in *Proc. of ISCAS,* pp. 374 – 377, May 2001.

[2] J. Ryynänen, *et al.*, "A single-chip multimode receiver for GSM900, DCS1800, PCS1900, and WCDMA," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 4, April 2003.

[3] M. Steyaert, *et al.*, "A single-chip CMOS transceiver for DCS-1800 wireless communications," in *IEEE ISSCC, Digest of Tech. Papers*, pp. 48 – 49, Feb. 1998.

[4] T. Cho, *et al.*, "A 2.4GHz dual-mode 0.18μm CMOS transceiver for bluetooth and 802.11b," in *IEEE ISSCC, Digest of Tech. Papers*, pp. 88 – 89, Feb. 2003.

[5] B. Razavi, *RF Microelectronics*. Prentice Hall, Inc, 1998.

[6] P. -I. Mak, S. -P. U and R. P. Martins, "Two-step channel selection technique by programmable digital-double quadrature sampling for complex low-IF receivers," *IEE Electronics Letters*, vol. 39, no. 11, pp. 825 – 827, May 2003.

[7] K. -P. Pun, J. E. Franca, C. A. Leme and R. Reis, "Quadrature sampling schemes with improved image rejection," *IEEE Trans. on Circuits and Syst.-II*, vol. 50 , no. 9, pp. 641-648, Sept. 2003.

[8] S. Samadian, R. Hayashi and A. A. Abidi, "Low power phase quantizing demodulators for a zero-IF Bluetooth receiver," in *IEEE Symposium on RFICs*, pp. 49 – 52, Jun. 2003.

[9] P. -I. Mak, C. -S. Sou, S. -P. U and R. P. Martins, "A frequency-downconversion and channel-selection A-DQS sample-and-hold pair for two-step-channel-select low-IF receiver," in *Proc. of ICECS*, pp. 479 – 482, Dec. 2003.