A FPGA-Based Power Electronics Controller for Hybrid Active Power Filters

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***Abstract*—In this paper, a power electronics controller implemented on one field-programmable gate array (FPGA) chip is proposed. The FPGA-based power electronics controller integrates the whole signal processing system including synchronous reference frame (SRF) algorithm, decoupled double synchronous reference frame phase-locked loop (DDSRF-PLL) and hysteresis pulse-width modulation (PWM). It is applicable to three-phase four-wire hybrid active power filters (HAPFs), which use four-leg voltage source inverters (VSIs). Different from the conventional controller using instantaneous reactive power theory, the proposed controller could work when source voltages are unbalanced. The bit width and I/O ports of the FPGA-based controller are user-defined. Hence, the proposed FPGA-based controller is more flexible than those using digital signal processors (DSPs). Parallel processing in FPGA could also achieve a faster control. The prototype of a three-phase HAPF is built and the proposed FPGA-based controller is adopted. Experimental results are provided to show its validity.**

I. INTRODUCTION

Compared with DSP, FPGA has flexibilities in defining bit-widths and I/O ports. Short bit width saves hardware resource and processing time. Long bit width guarantees accuracy. Rich I/O ports mean FPGA-based system can be developed to control power electronics device requires more switching signals since one switching signal is generated by one port. Parallel processing makes FPGA have high process efficiency. The design in FPGA is mapped into actual circuit and the processing is clock triggered. Precision will be better.

The work of this paper is implementing a FPGA-based power electronics controller and applying it in a prototype of three-phase four-wire HAPF. The compensation using FPGA-based power electronics controller is applicable when source voltages are unbalanced, because the compensation current detection algorithm is modified. Many theories have been developed since the concept of instantaneous reactive power theory for calculating compensation currents was established. Generalized instantaneous reactive power theory [1][2] and compensation by using pq theory [3] are only applicable when source voltages are balanced without harmonics. Compensation by using pqr theory [4] and SRF theory [5] with conventional SRF-PLL can provide accurate compensation currents only when source voltages are balanced with or without harmonics. However, these typical theories cannot calculate accurate compensation currents when source voltages are unbalanced and distorted. DDSRF-PLL [6] is used to replace SRF-PLL in SRF algorithm so that the compensation currents obtained are accurate no matter source voltages are balanced or unbalanced and distorted. In this paper, the operation principles of the control system is introduced in section Ⅱ. Its implementation on FPGA is discussed in section Ⅲ. Experimental results in section Ⅳ are provided to show the validity.

II. OPERATION PRINCIPLES

Figure 1 shows the configuration of compensation system using three-phase four-wire HAPF. The main circuit of the HAPF is a two-level four-leg VSI. The block diagram of signal processing system in FPGA is given in Figure 2. The source voltages (v_{sa}, v_{sb}, v_{sc}), load currents (i_{la}, i_{lb}, i_{lc}) and injected currents (i_{ca}^*, i_{cb}^*, i_{cc}^*) should be detected from circuit.

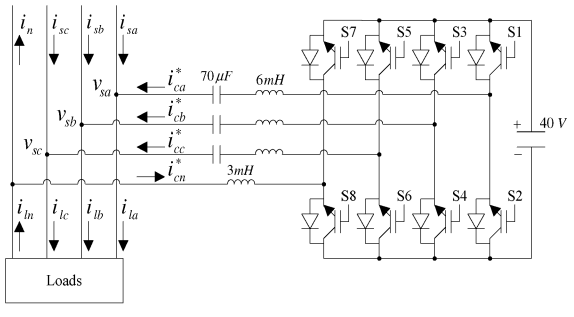

Figure 1. Block diagram of a three-phase four-wire system with HAPF

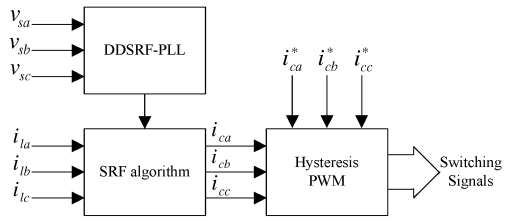

Figure 2. Block diagram of signal processing system in FPGA

SRF algorithm is used for calculating compensation currents. The d and q components of the load currents in the block diagram of SRF algorithm [5] can be obtained by

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = [T][C] \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix}. \tag{1}$$

Where

$$[C] = \begin{bmatrix} \sqrt{2/3} & -\sqrt{1/6} & -\sqrt{1/6} \\ 0 & \sqrt{1/2} & -\sqrt{1/2} \end{bmatrix}, \tag{2}$$

$$[T] = \begin{bmatrix} cos(\theta) & sin(\theta) \\ -sin(\theta) & cos(\theta) \end{bmatrix}. \tag{3}$$

When the imbalance, reactive power and harmonics in a three-phase system with or without the neutral current should be fully compensated, the three-phase compensation currents are expressed as

$$\begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} = \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} - [C]^T [T] \begin{bmatrix} \bar{i}_d \\ 0 \end{bmatrix}. \tag{4}$$

The compensation current of the neutral is equal to

$$i_{cn} = -i_{ca} - i_{cb} - i_{cc}. \tag{5}$$

Based on (1)-(5), the accuracy of the compensation currents are determined by the phase angle provided. DDSRF-PLL can provide instantaneous phase angle of positive sequence under unbalanced and distorted case. It is applied for SRF algorithm. The accuracy of the compensation currents will be not affected by source voltages.

In order to control the inverter output current tracking with reference one, hysteresis PWM [7] is used to obtain the switching signals by comparing the compensation current to the tolerance bands. Thus, the switching signals are obtained.

III. Design And Implementation

The whole signal processing system is implemented on XILINX XC3SD1800A Spartan-3A DSP FPGA. It has 1800K system gates or 37440 equivalent logic cells and 519 maximum user I/O ports. The FPGA control board used is XtremeDSP Starter Platform. The clock period adopted is 200 ns which is generated by 125 MHz oscillator. An analog-to-digital converter (ADC) embedded on TDS2812EVMB is employed to detect 9-channel signals from the circuit and transfer the signals to FPGA. The sample period is equal to 50 μs. The FPGA-based power electronics controller adopted 16 input ports to receive signals and 8 output ports to generate switching signals for the HAPF.

A. *Communication from DSP to FPGA*

The communication from DSP to FPGA is transmitting the 9-channel signals. And serial transmission is adopted. In order to identify the 9-channel signals, 4-bit address is also transmitted. Since each channel signal is expressed by 12 bits, DSP transmits 16 bits every time including 12-bit data and 4-bit address by 16 GPIO ports. The 16 GPIO ports hold each signal 1400 ns. When the transmission is over, the states of 16 GPIO ports hold low voltages. 16 ports of FPGA are defined to receive the 12-bit data and 4-bit address. They sample the signals of GPIO ports every 200 ns. The 12-bit data is ensured to be correct if only the 5 sequential samples of the 4-bit address are identical. FPGA will achieve series to parallel conversion of the 9-channel signals for further parallel processing. Moreover, the 9-channel signals are expressed by 16 bits with Q15 format in FPGA.

B. *SRF Algorithm*

All the constants or variables in SRF algorithm are expressed by 16 bits with Q15 format. Parallel processing is carried out, so the three-phase and neutral compensation currents are obtained at the same time.

In SRF algorithm, the dc component is extracted by a second-order low-pass filter (LPF). It is cascaded by 2 identical first-order butterworth infinite impulse response (IIR) LPF which cut-off frequency is 40 Hz. Its transfer function is

$$H(z) = \frac{0.0062 + 0.0062z^{-1}}{1 - 0.9875z^{-1}}. \tag{6}$$

C. *DDSRF-PLL*

FPGA exhibits the flexibility in arranging bit width herein although most constants and variables in DDSRF-PLL can be expressed by 16 bits with Q15 format. LPF, loop filter (LF), voltage-controlled oscillator (VCO) and look-up table (LUT) in the block diagram of DDSRF-PLL shown in Figure 3 are introduced and emphasized.

In the decoupling network of DDSRF-PLL, 4 LPFs are required. And the first-order LPF introduced in SRF algorithm is applied in decoupling network. All filters' parameters are expressed by 16 bits with Q15 format.

LF is a proportional-integral control. The integral operation is approximated by

$$Tz/(z-1). \tag{7}$$

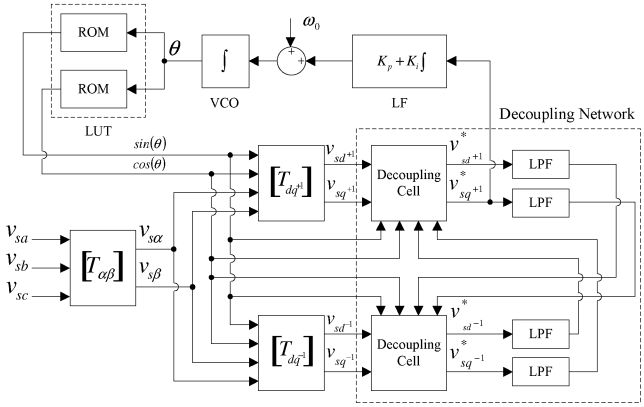

Figure 3. Block diagram of DDSRF-PLL

T is the sample period. Besides, the constants K_i and K_p in LF satisfies

$$\xi = 0.5K_p \Big/ \sqrt{K_i} \approx 0.707 \cdot \tag{8}$$

Low K_i improves the performance of noise rejection, but dynamic response would be weakened [8]. Constants Ki= $(40\pi)^2$ and Kp=1.414×40π are chosen in the design. In order to avoid overflow happens, the processing result in the parallel path of proportional-integral control is expressed by more than 16 bits. The processing result of proportional-integral control is expressed by 24 bits and Q15 format.

VCO is also an integral operation in digital system. And its output is phase angle. VCO will be reset once its output is equal to or larger than 2π. Thus, overflow is avoided. And its output is expressed by 18 bits and Q15 format.

LUT with 16384 values is adopted to retrieve the corresponding sine or cosine value from a memory address. All the values in LUT are expressed by 16 bits with Q15 format. They are created by MATLAB and stored in the ROMs.

D. *Hysteresis PWM*

In hysteresis PWM, current is compared with two tolerance bands. If the actual compensation current is larger than the upper band, the upper switch in Figure 1 is turned off. If the actual compensation current is less than the lower band, the upper switch in Figure 1 is turned on. Furthermore, the state of corresponding lower switch is always reverse with the state of the upper switch. It is not difficult to implement hysteresis PWM by comparison operation. And 8 ports are used for generating switching signals. Since FPGA has rich I/O ports, the FPGA-based power electronics controller can be further developed to control multi-level VSIs with more switches.

Dead-time should be provided in practice for protection. The dead-time in the design is 8 μs. The dead-time is held when the state of the switch is changed. Once the 2 sequential states of the same switch are different, dead-time operation is triggered.

IV. EXPERIMENTAL RESULTS

The main circuit of the HAPF is a four-leg IGBT VSI in experiment. The configuration of compensation system using three-phase four-wire HAPF in experiment is the same as Figure 1.

A. *Source Voltages Are Balanced*

The waveforms of three-phase source voltages and three-phase source currents before and after compensation in experiment are both shown in Figures 4 and 5, respectively. Experimental results listed in Table Ⅰ indicate power factor (PF) of three phases (A, B, C), total harmonic distortion (THD) of three phases (A, B, C) and root mean square (RMS) value of neutral current are improved obviously.

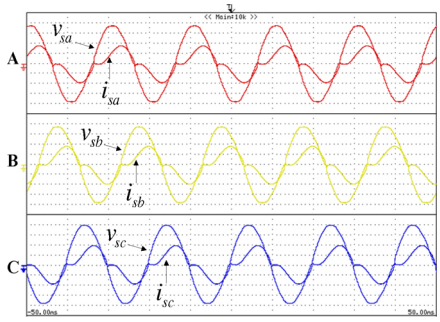

Figure 4. Waveforms of three-phase source voltages and three-phase source currents before compensatoin

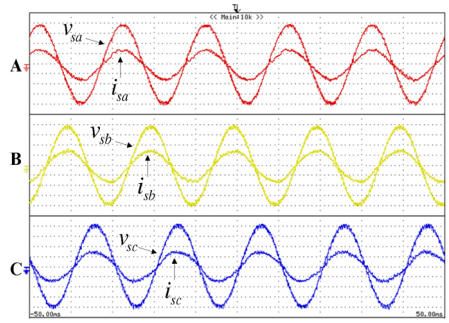

Figure 5. Waveforms of three-phase source voltages and three-phase source currents after compensatoin

TABLE I. EXPERIMENTAL RESULTS

		Source Currents Before Compensation	Source Currents After Compensation
PF	***A***	0.83	1.00
	B	0.86	0.99
	C	0.83	0.99
THD	***A***	23.4%	7.0%
	B	22.4%	6.0%
	C	23.7%	7.2%
Neutral		1.54443 A	372.544 mA

B. *Source Voltages Are Unbalanced and Distorted*

The imbalance and harmonics result from a resistor cascaded at the source side of phase A. The voltage drop in phase A is 30%. Besides, the maximum THD of source voltages is 9.7% in experiment. The waveforms of three-phase source voltages and three-phase source currents before and after compensation in experiment are shown in Figures 6 and 7, respectively. Experimental results listed in Table Ⅱ indicate PF of three phases (A, B, C), THD of three phases (A, B, C), current unbalance and RMS value of neutral current are improved.

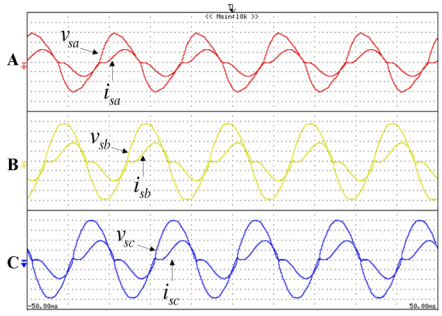

Figure 6. Waveforms of three-phase source voltages and three-phase source currents before compensatoin

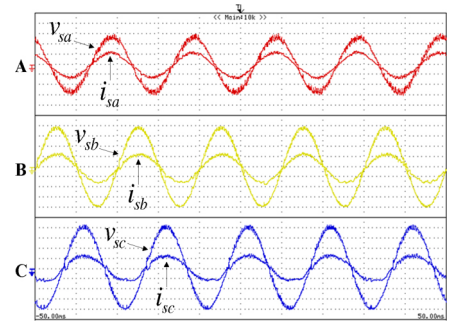

Figure 7. Waveforms of three-phase source voltages and three-phase source currents after compensatoin

TABLE II. EXPERIMENTAL RESULTS

		Source Currents Before Compensation	Source Currents After Compensation
PF	***A***	0.84	0.99
	B	0.86	1.00
	C	0.83	0.99
THD	***A***	18.6%	5.0%
	B	22.5%	5.7%
	C	23.4%	9.8%
Current Unbalance		18.18%	9.74%
Neutral		1.50406 A	357.348 mA

V. CONCLUSION

In this paper, a FPGA-based power electronics controller is implemented on XILINX XC3SD1800A Spartan-3A DSP FPGA. Design and implementation are introduced. The application of DDSRF-PLL makes compensation currents obtained by SRF algorithm be accurate no matter source voltages are balanced or unbalanced, with or without harmonics. The validity is proved by experimental results. Moreover, the FPGA-based design possesses many advantages. Bit width for variables or constants is optimized on the basis of accuracy and efficiency. 24 I/O ports are occupied. 16 input ports are used for receiving signals detected from circuit and 8 output ports are used for generating 8 switching signals. Parallel processing is also widely adopted in the design. The proposed controller can generate switching signals within half a sample period 50 μs. FPGA is an advisable choice for power electronics applications.

ACKNOWLEDGMENT

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REFERENCES

[1] Fang Zheng Peng; Ott, G. W., Jr.; Adams, D. J., "Harmonic and reactive power compensation based on the generalized instantaneous reactive power theory for three-phase four-wire systems," IEEE Transactions on Power Electronics, vol. 13, no. 6, pp. 1174–1181, November 1998.

[2] Fang Zheng Peng and Jih-Sheng Lai, "Generalized instantaneous reactive power theory for three-phase power systems," IEEE Transactions on Instrumentation and Measurement, vol. 45, no. 1, pp. 293–297, February 1996.

[3] Aredes, M.; Akagi, H.; Watanabe, E.H.; Vergara Salgado, E.; Encarnacao, L.F., "Comparisons Between the p-q and p-q-r Theories in Three-Phase Four-Wire Systems," IEEE Transactions on Power Electronics, vol. 24, no. 4, pp. 924–933, April 2009.

[4] Hyosung Kim; Blaabjerg, F.; Bak-Jensen, B and Jaeho Choi, "Instantaneous power compensatoin in three-phase systems by using p-q-r theory," IEEE Transactions on Power Electronics, vol. 17, no. 5, pp. 701–710, September 2002.

[5] da Silva, S.A.O.; Donoso-Garcia, P.F.; Cortizo, P.C.; Seixas, P.F., "A Three-Phase Line-Interactive UPS System Implementation With Series-Parallel Active Power-Line Conditioning Capabilities", IEEE Transactions on Industrial Applications, vol. 38, no. 6, pp. 1581-1590, November/December 2002

[6] Rodriguez, P.; Pou, J.; Bergas, J.; Candela, J.I.; Burgos, R.P. and Boroyevich, D., "Decoupled Doubled Synchronous Reference Frame PLL for Power Converters Control," IEEE Transactions on Power Electronics, vol. 22, no. 2, pp. 584–592, March 2007

[7] Le-Huy, H.; Dessaint, L.A., "An Adaptive Current Control Scheme for PWM Synchronous Motor Drives: Analysis and Simulation", IEEE Transactions on Power Electronics, vol. 4, no. 4, pp. 486–495, October 1989

[8] L Rolim, L.G.B.; da Costa, D.R.; Aredes, M., "Analysis and Software Implementation of a Robust Synchronizing PLL Circuit Based on the pq Theory", IEEE Transactions on Industrial Electronics, vol. 53, no. 6, pp. 1919-1926, December 2006

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