A Power-Efficient Capacitor Structure for High-Speed Charge Recycling SAR ADCs

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Abstract— **A novel Capacitor array structure for Successive Approximation Register (SAR) ADC is proposed. This circuit efficiently utilizes charge recycling to achieve high-speed of operation and it can be applied to low-to-medium-resolution, high-speed SAR ADC's. The parasitic effects of the proposed structure are analyzed theoretically and behavioral simulations are presented to verify the circuit's performance under those non-idealities. The simulation results show that the proposed capacitor array structure can reduce the average power consumed in the capacitor array by 90% when compared to the binary-weighted splitting capacitor method.**

I. Introduction

The SAR ADC is widely used in many communication systems, such as ultra-wideband (UWB) and wireless sensor networks which require low power consumption and low-to-medium-resolution converters. Traditional SAR ADCs are difficult to be applied in high-speed, however, the improvement of technologies and design methods have allowed the implementation of high-speed, low-power SAR ADCs that become consequently more attractive for a wide variety of applications [1], [2].

The power dissipation in a SAR converter is dominated by the reference ladder of the DAC capacitor array. Recently, a capacitor splitting technique has been presented, which was proven to use 31% less power from the reference voltage supply[3]. The total power consumption of a 5b binary-weighted split capacitor array is 6mW, and often this does not take into account the reference ladder [1]. Moreover, as the resolution increases, the total number of input capacitance in the binary-scaled capacitive DAC will cause an exponential increase in power dissipation, as well as a limitation in speed, due to a large charging time-constant. Therefore, a small capacitance spread in the DAC capacitor array is highly desirable for high speed SAR ADCs [4].

This paper presents a novel structure of a split capacitor array to optimize the power efficiency and the speed of SAR ADC's. Due to the series combination of the split capacitor array, smaller values of the capacitor ratios and a more power-efficient charge recycling approach in the DAC capacitor array can be achieved, simultaneously, leading to fast DAC settling time and low power dissipation in the SAR ADC. The parasitic effects and the position of the attenuation capacitor in the proposed structure will be theoretically discussed and behavioral simulations will be performed. The design and simulations of an 8b 180-MS/s SAR ADC in 1.2-V supply voltage are presented in 90nm CMOS exhibiting a Signal-to-Noise-and-Distortion Ratio (SNDR) of 48 dB, with the total power consumption of 14mW, which demonstrates the feasibility of the proposed circuit.

II. The Overall SAR ADC Operation

The architecture of a SAR ADC is shown in Fig.1, consisting of a series structure of a capacitive DAC, a comparator and successive approximation (SA) control logic. The SA control logic includes shift registers and switch drivers which control the DAC operation by performing the binary-scaled feedback during the successive approximation. The DAC capacitor array is the basic structure of the SAR ADC and it serves both to sample the input signal and as a DAC for creating and subtracting the reference voltage.

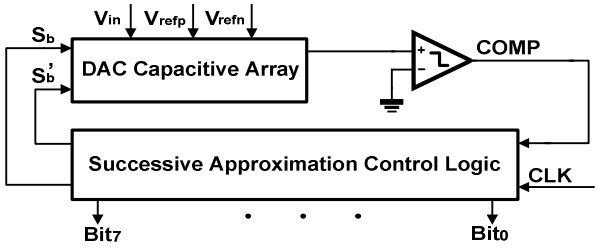

Fig. 1: Simplified block diagram of a SAR ADC architecture.

III. Capacitor Array Analysys

A. Capacitor Structure Design

The major speed limitation of the SA converter is often related with the RC time composed by the capacitor array, reference ladder resistance and the respective switches. For a binary-weighted split capacitor array [1], the sum of the total capacitance rises exponentially with the resolution in terms of numbers of bits, which causes large RC settling time, thus limiting the speed of the overall SAR ADC. To solve this problem, a series split capacitor array structure is designed, as shown in Fig.2, where an attenuation capacitor C_{atten} and split capacitor arrays are utilized. The attenuation capacitor is used to separate the split capacitive array into b_M bits MSB and b_L bits LSB array. According to the division ratio of the SAR algorithm, the attenuation capacitor can be calculated as:

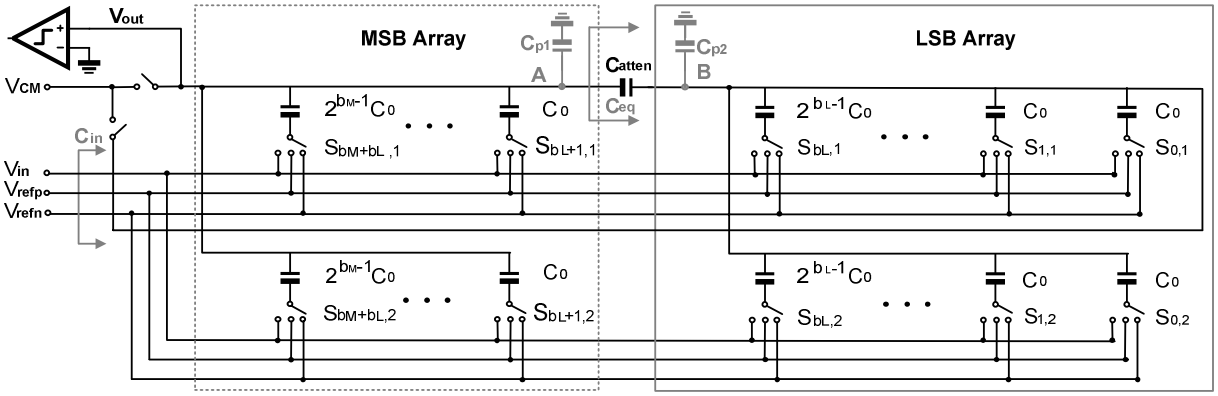

Fig. 2: (b_M + b_L+1)-bit series split capacitor array.

$$C_{atten} = C_{sumLSB} /(C_{sumLSB} / 2 - 1) \tag{1}$$

where

$$C_{sumLSB} = 2^{b_L+1} C_0 \tag{2}$$

is the sum of capacitance in LSB array. Then, the equivalent capacitance C_{eq} at the right side of LSB array can be calculated as:

$$C_{eq} = C_{atten} // C_{sumLSB} = 2C_0. \tag{3}$$

The C_{eq} can then be seen as two split unit capacitors C_0 attached to the right side of MSB array to maintain the capacitive ratio as 2^{bM-1}:…:2:1:1. Therefore, the charge-recycling methodology in each section can perform binary-scaled feedback during the successive approximation.

B. Charge Recycling Implementation

In the proposed implementation, the series split capacitor array is designed to achieve charge recycling for the n (n=b_M+b_L+1) bit capacitive DAC, as shown in Fig.2. During the global sampling phase, the voltage V_{in} is stored in the entire capacitor array. Then, the algorithmic conversion begins by switching all upper capacitor arrays to V_{ref} and the lower to $-V_{ref}$, respectively, instead of switching only the MSB capacitor to V_{ref} and others to $-V_{ref}$. This implies that in the conversion phase 1 (corresponding to MSB capacitor conversion) V_{out} settles to (considering only differential node voltage)

$$V_{out}[1] = -V_{in} + V_{ref} / 2 - V_{ref} / 2 = -V_{in} \tag{4}$$

and the comparator output will be

$$D_1 = \begin{cases} -1 & V_{in} > 0 \\ 1 & V_{in} < 0 \end{cases}. \tag{5}$$

The comparator output will decide the switching logic of $S_{bM+bL,1}$ and $S_{bM+bL,2}$. If D_1 is low, $S_{bM+bL,1}$ is switched to -V_{ref}, dropping the voltage at $V_{out}[2]$ to -V_{in}-V_{ref}/2. If D_1 is high, $S_{bM+bL,2}$ is switched to V_{ref}, raising the voltage at $V_{out}[2]$ to -V_{in}+V_{ref}/2. The above process is repeated for n-1 cycles.

As $S_{bM+bL,1}$ is switched from V_{ref} to $-V_{ref}$ (bit decision back from "1" to "0") the switches, from $S_{0,1}$ to $S_{bM+bL-1,1}$, are kept connected to V_{ref} and drive $V_{out}[1]$ to $V_{out}[2]$. The initial charge, supplied by V_{ref} in phase 1, is kept stored in the capacitors which will connect to V_{ref} at phase 1, instead of being redistributed, so the charge formed at phase 1 can be recycled in the next n-1 phases. However, the conventional switching method, that discharges MSB capacitor and charges the MSB/2 capacitor, will cause charge redistribution in the capacitor array and thus consuming more power.

C. Linearity Performance

One potential issue with this series split capacitor array structure is the parasitic capacitance C_{p1} and C_{p2} on the nodes A and B, which will deteriorate the desired voltage division ratio and result in poor linearity. Note that the parasitic effects are caused by the bottom- and top-plate parasitic capacitance of C_{atten} and the top-plate parasitic capacitance of MSB and LSB array which can be calculated as:

$$C_{p1} = \alpha \cdot C_{atten} + \beta \cdot C_{sumMSB} \tag{6}$$

$$C_{p2} = \beta \cdot C_{atten} + \beta \cdot C_{sumLSB} \tag{7}$$

where α and β represent the percentage of bottom- and top-plate parasitic capacitance of each capacitor, respectively. The linearity of a SAR ADC is limited by the accuracy of the DAC output which is calculated here for the case of zero initial charge on the array (V_{in}=0). For a given DAC digital input X, the analog output $V_{out}(X)$ can be calculated as:

$$V_{out}(X) = \frac{C_{atten}(\sum_{n=1}^{b_L}\sum_{n'=1}^{2} D_{n,n'} 2^{n-1} C_0 + \sum_{n=1}^{b_M}\sum_{b'=1}^{2} D_{n,n'} 2^{n-1} C_0) + (C_{sumLSB}+C_{p2})\sum_{n=1}^{b_M}\sum_{n'=1}^{2} D_{n,n'} 2^{n-1} C_0}{C_{atten}(C_{sumLSB}+C_{sumMSB}+C_{p1}+C_{p2}) + (C_{sumLSB}+C_{p2})(C_{sumMSB}+C_{p1})} V_{ref} \tag{8}$$

where

$$C_{sumMSB} = 2\sum_{n=1}^{b_M} 2^{n-1} C_0 \tag{9}$$

is the sum of capacitance in the MSB array and $D_{n,n'}$ equal to "1" or "-1" represents the ADC decision for bit n. From (8) the parasitic capacitances C_{p1} and C_{p2} in the denominator are completely uncorrelated for the bit decisions, which can only cause a gain error and has no effect in the linearity performance. However, the parasitic capacitance C_{p2} in the numerator contributes with a code dependent error, which degrades the linearity of the conversion performance. Subtracting the nominal value the error term will become

$$V_{error}(X) = \frac{C_{p2}\sum_{n=1}^{b_M}\sum_{n'=1}^{2} D_{n,n'} 2^{n-1} C_0}{C_{atten}(C_{sumLSB}+C_{sumMSB}+C_{p1}+C_{p2}) + (C_{sumLSB}+C_{p2})(C_{sumMSB}+C_{p1})} V_{ref}. \tag{10}$$

The parasitic capacitance C_{p2} is composed of the parasitic capacitance of C_{atten} and C_{sumLSB}. By reducing the number of bits in the LSB array, the size of C_{sumLSB} can be minimized, thus the nonlinearity effect can be alleviated. But this will enlarge the capacitor spread in MSB array, thus the distribution of bits in both MSB and LSB array should consider the trade-off between linearity tolerance and capacitor spread limitation.

To analyze the linearity of the series split capacitor array, each of the capacitors is modeled as the sum of the nominal capacitance value and the error term:

$$C_{n,1} = 2^{n-1} C_0 + \delta_{n,1} \quad (11)$$

$$C_{n,2} = 2^{n-1} C_0 + \delta_{n,2} \quad (12)$$

considering the case where all the errors are in the unit capacitors, whose values are independent-identically-distributed Gaussian random variables with variance

$$E[\delta_{n,1}^2] = E[\delta_{n,2}^2] = 2^{n-1} \sigma_0^2 \quad (13)$$

where σ_0 is the standard deviation of the unit capacitor.

Two behavioral simulations of a SAR ADC were performed where the values of the unit and attenuation capacitors are Gaussian random variables with standard deviation of 1% (σ_0 / C_0=0.01), 5% top-plate and 10% bottom-plate parasitic capacitances for Mrtal-Insulator-Metal (MIM) capacitor, whereas the ADC is otherwise ideal. Fig.3 shows the result of 1000 Monte Carlo runs, where the SNDR are plotted versus different distribution of bits in the MSB and LSB array at the 8-bit level. Comparing the SNDR shown in Fig.3, and as expected, a larger number of bits in the LSB array will cause poor linearity. Although MSB:LSB=5:2 can achieve the best SNDR, since larger capacitor ratios will both reduce the conversion speed and increase the power dissipation, MSB:LSB=4:3 will be adopted for circuit implementation in the next Section due to both good linearity performance and smaller capacitor ratios. Fig.4 illustrates the result of 1000 Monte Carlo runs, where the SNDR are plotted versus the percentage of the top-plate parasitic capacitance β at the 6 to 12 bit level with proper bits distribution of the LSB and MSB arrays. As C_{p2} increases the parasitic capacitance will degrade the conversion performance. But with a variance of β approximately equal to ±5%, a good linearity performance of a SAR ADC can still be achieved.

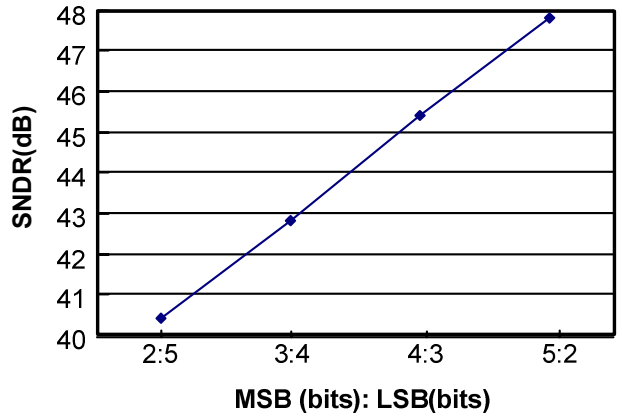

Fig. 3: Behavioral simulation of 1000 Monte Carlo SNDR versus the different bits distribution of MSB and LSB array.

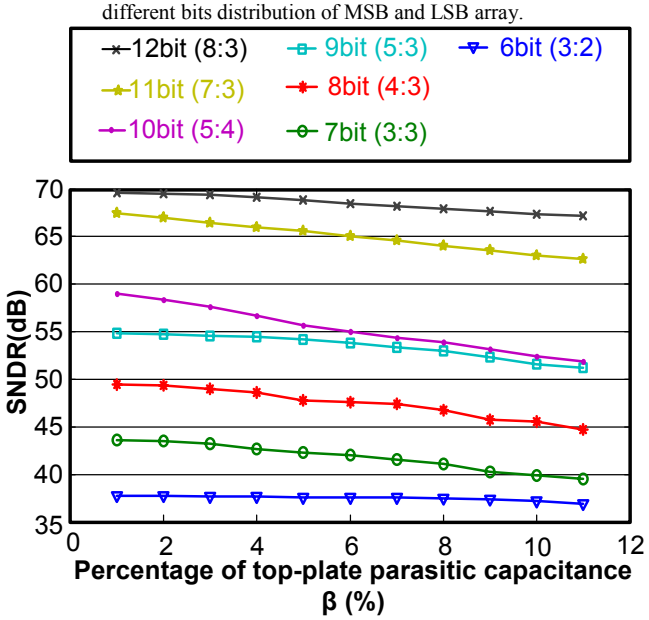

Fig. 4: Behavioral simulation of 1000 Monte Carlo SNDR versus the percentage of the top-plate parasitic capacitance β of series split capacitor array at 6 to 12 bit level.

D. *Power Consumption Analysis*

The power consumption of the SAR converter is dominated by the DAC capacitor array, the comparator and the switches' drivers. The array's power is proportional to the sum of the array total capacitance C_{total} of which the bottom-plate is connected to the reference voltage supply and can be calculated as:

$$P_{array} = C_{total} V_{ref} V_{FS} \quad (14)$$

where V_{FS} is the full-scale input voltage, assuming that V_{FS} has been fully sampled on to the capacitor array and the charge is all supplied by the reference voltage V_{ref} [1]. In a 8 bit case, the C_{total} of the proposed structure is $46C_0$ (with MSB:LSB=4:3), but for a binary-weighted capacitor array the C_{total} is $256C_0$, which can consume 5 times more power than the proposed structure. The series combination allows a significant reduction of the largest capacitor ratio. For example in an 8 bit case, the largest capacitor C_{max} of the series split and binary-weighted split capacitor array structure is $8C_0$ and $64C_0$, respectively, which decreases the DAC settling time and speeds up the conversion. The total input capacitance of the proposed structure is not completely dependent on the number of bits of the ADC, and can be calculated as:

$$C_{in} = C_{sumMSB} + 2C_0. \quad (15)$$

The power consumptions of the comparator and switch drivers are also proportional to the equivalent input capacitance C_{in}. Therefore, smaller C_{total}, C_{max} and C_{in} will imply an increase in efficiency of the overall conversion performance.

IV. Circuit Implementation Details

A high-speed SAR converter imposes a stringent requirement in the clock generation, e.g. an 8b 180-MS/s SAR ADC requires an internal master clock of over 1.62 GHz. To generate such a high frequency clock pulse the generator will consume even more power

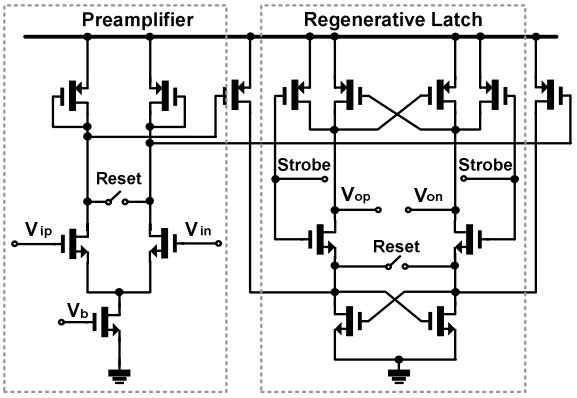

Fig. 5: Circuit schematic of the dynamic comparator.

than the ADC itself. Due to the power limitations of the clock generator in a synchronous SA design an asynchronous SAR processing technique [4] will be adopted here, where only a master clock of 180MHz is required.

The dynamic comparator [5] used in this ADC is shown in Fig. 5 and it is composed of a preamplifier and a regenerative latch. The preamplifier can provide sufficient gain to suppress the relatively high input referred offset voltage of the latch. Also, the kickback noise of the latch can be isolated by the current mirror between the two stages. The dynamic operation of this circuit is divided into a reset phase and a regeneration phase. During the reset phase, the two outputs (V_{op} and V_{on}) are pulled up to V_{DD}. After the input stage has settled, the voltage difference is then amplified to a full swing during the regeneration phase. The differential output can generate a data ready signal to indicate the completion of the comparison, which will be used to trigger a sequence of shift registers and the switch drivers to perform asynchronous conversion [4]. Dynamic logic circuits are also utilized instead of traditional static logic to release the limitation of digital feedback propagation delay in the SA loop.

V. Simulation Of a 8-bit 180MS/s SAR ADC

To verify the proposed capacitor structure of the capacitive DAC, a 1.2 V, 8b, 180-MS/s SAR ADC was designed using a 90 nm CMOS process with MIM capacitor option. The SAR ADC is implemented in fully-differential architecture with a full-scale differential input range $1.2V_{PP}$. Considering the parasitic capacitances β that will reduce the linearity of the ADC, 5% top-plate and 10% bottom-plate parasitic capacitance have been introduced in the simulations according with recommendations from the foundry.

Fig. 6 shows a spectrum plot of the SAR ADC through a Monte-Carlo simulation with an input signal of 76MHz leading to an SNDR of 48dB, which clearly demonstrates the tolerance of the parasitic effects caused by the C_{p2}. Fig. 7 illustrates the corresponding 30-time Monte-Carlo mismatch simulations where the ADC achieves a mean SNDR of 49dB with the input signal of 76MHz. Fig. 8 exhibits the comparison between the SNDR of the proposed ($C_{max}=8C_0$, $C_{total}=46C_0$) and binary-weighted capacitor array ($C_{max}=64C_0$, $C_{total}=256C_0$) structure versus the power consumption of the reference ladder, which demonstrates that the binary-weighted capacitor array leads to poor SNDR, due to the large RC settling time. To reach the same conversion performance the binary-weighted capacitor array consumes 10 times more power than the proposed structure. Table I summarizes the overall performance of the SAR ADC with a total power consumption of 14mW only and a FOM of 0.35pJ/conversion-step, clearly proving the low power dissipation feature of the proposed technique.

VI. Conclusions

A novel series structure for a charge recycling capacitive DAC has been proposed which can be applied to high-speed SAR ADCs. The series combination of the split capacitor array can both feature charge recycling and small input capacitance. The reduction of the maximum ratio and sum of the total capacitance can lead to silicon area savings and power efficiency, which allows the SAR converter to work at high-speed and low power consumption. Simulation results of a 1.2V, 8b, 180-MS/s SAR ADC were presented exhibiting an SNDR of 48dB for a 76MHz input with a total power consumption of 14mW thus certifying the power efficiency of the novel circuit structure.

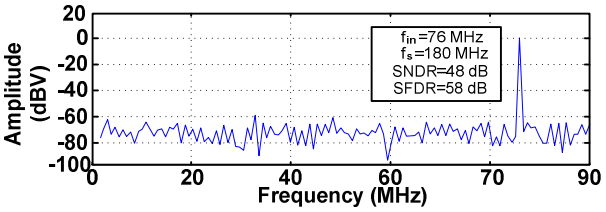

Fig. 6: Simulated FFT spectrum of the ADC.

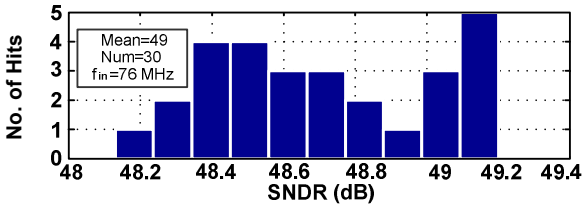

Fig. 7: 30-time Monte-Carlo SNDR simulations (8b SAR).

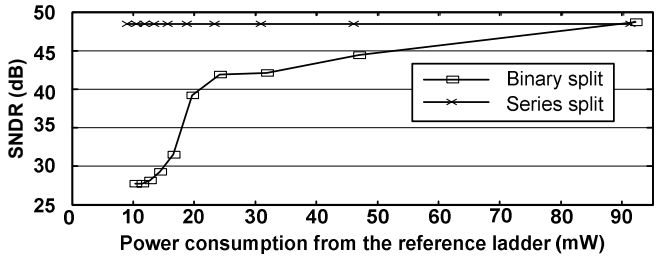

Fig. 8: Simulated SNDR versus power consumption from the reference ladder for series split and binary-weighted split capacitor array.

TABLE I. Performance Summey Of The SAR ADC

Technology	90-nm CMOS with MIM	ENOB (@f_{in}=76MHz)	7.7 bit
Resolution	8 bit	FOM	0.35pJ/conversion step
Sampling Rate	180 MS/s	Power Consumption	
Supply Voltage	1.2 V	Anolog	2.4 mW
Full Scale Analog Input	1.2 Vpp differential	Digital	2.3 mW
SNDR (@f_{in}=76MHz)	48 dB	Reference ladder	9.3 mW
SFDR (@f_{in}=76MHz)	58 dB	Total	14 mW

Acknowledgment

This work was financially supported by University of Macau under the Research Grant with Ref no: RG058/06-07S/MR/FST.

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