A sub-1V BJT-based CMOS temperature sensor from -55 °C to 125 °C

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***Abstract*—In this paper, a smart temperature sensor working at a supply voltage as low as 0.9V over the full military temperature range is presented. Low voltage operation is achieved by biasing the front-end BJT pairs with different emitter currents for two different sensing ranges, from -55°C to 30°C and from 20°C to 125°C, respectively. A second-order inverter-based $\Sigma\Delta$ADC with dynamic element matching (DEM) and input signal chopping to control the conversion error to within 0.2°C is used for digital readout. Front-end bias currents are selected during the design stage to minimize the induced sensing error. The proposed sensor is implemented using the TSMC 0.18μm 1P6M process. Simulation result shows that a $+1$°C$/-0.1$°C sensing error using one-point calibration can be achieved from -55°C to 125°C. At a sampling speed of 20 samples/s, the sensor consumes 3.4μA and 4.7μA in the low temperature range and the high temperature range, respectively.**

I. Introduction

CMOS temperature sensors are widely used in applications including ambient temperature detection, micro-controller thermal management and many more. With the possibility of integrating temperature sensors in the same substrate with microprocessors and/or DSP, enhanced system reliability with much reduced cost can be accomplished. Recently, the integration of temperature sensors in wireless platforms such as RFID tag systems has also been reported. For these applications, ultra-low power consumption is required for longer lifespan or wider operating range [1].

Several on-chip temperature sensors utilizing different sensing mechanisms have been reported. With the use of two delay lines, Chen et. al. [2] designed a time-domain temperature sensor with a low cost time-to-digital converter, and Law et. al. [3] further implemented a fully differential time-domain temperature sensor with improved SNR. However, the above designs are prone to process, voltage and temperature (PVT) variations and generally require two-point calibration to achieve moderate inaccuracy, making them cost ineffective. Kashmiri et. al. [4] designed a process spread and packaging stress independent temperature sensor with high linearity by exploiting the thermal diffusivity of silicon, but is comparatively power inefficient. BJT-based temperature sensor, as reported by Pertijs, et. al. [5], requires only one-point calibration to achieve high accuracy with moderate power consumption, and is therefore a popular choice in temperature sensor implementations.

Meanwhile, technology scaling calls for lower system supply voltage to reduce power consumption and enhance system reliability. However, BJT-based temperature sensors are limited by its intrinsic bandgap voltage, and supply voltage scaling would definitely narrow down its effective sensing range. The minimum required supply voltage can easily exceed 1.2V for military temperature range sensing [6]. The lowest ever reported power supply for BJT-based temperature sensor is 1.05V, with a sensing range from -10°C to 110°C [7]. A CMOS temperature sensor that is capable of operating at an even lower supply voltage is needed for further technology scaling as well as lower power consumption, without sacrificing the sensing range.

In this paper, we present a BJT-based temperature sensor that can operate at a supply voltage as low as 0.9V and is capable of performing military range temperature sensing from -55°C to 125°C. By using the proposed dual-range sensing methodology, both low supply voltage operation and wide sensing range can be accomplished at the same time. An inverter based $\Sigma\Delta$ADC [8] is utilized for digital readout. Only one-point calibration is required by calibrating at an overlapping temperature for the two ranges. Simulation results show that the proposed sensor can achieve $+1$°C$/-0.1$°C sensing inaccuracy after one-point calibration at room temperature.

This paper is organized as follows. Section II demonstrates the operation principle of the dual-range temperature sensing scheme and the BJT-core bias current selection criteria. Section III describes the temperature sensor front-end and the inverter based $\Sigma\Delta$ ADC readout circuitry design. System simulation results are given in section IV and the conclusion is provided in section V.

II. Operation Principle

A. Dual-range Sensing

Base-emitter voltage V_{be} of a PNP bipolar transistor with emitter bias current I_e can be described by

$$I_c = I_e(1-\frac{1}{\beta});\quad V_{be}(T) = \frac{kT}{q}\ln\frac{I_c}{I_s(T)}\quad (I_c \gg I_s) \quad (1)$$

where I_c is the BJT collector current, β is the BJT common emitter current gain, k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, and I_s is the BJT saturation current. For a diode-connected PNP based temperature sensor, the minimum required supply voltage equals to the sum of V_{be} and the current source headroom. The current source headroom is generally fixed to ensure safe operation during the design stage. In order to achieve

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low supply voltage operation, the V_{be} amplitude needs to be reduced at the lower bound of the military temperature range (i.e. -55°C). From Eq.(1), by appropriately lowering I_e, the V_{be} amplitude can be reduced accordingly. However, small I_e will narrow down the sensing range due to signal distortion in V_{be} at high temperatures. A possible solution is to apply a larger I_e at high temperature so that the V_{be} amplitude can be increased. With such a dual-range sensing scheme, both low voltage operation and wide sensing range can be achieved simultaneously.

A BJT device is subjected to shot noise, thermal noise, flicker noise and burst noise. Flicker noise and burst noise mainly lie within the low frequency range [9]. The diode shot noise is linearly dependent on the bias current I_e, while the diode thermal noise is temperature dependent. Despite the noise from the BJT devices, the noise from the current sources (i.e. MOSFET flicker noise and thermal noise) will also contribute to the total noise content in the sensor front-end. In our system, chopping technique is utilized to modulate the temperature signal to higher frequency, and the low frequency noise (i.e. flicker and burst noise) can be suppressed through filtering. Notice that at low temperature, the system has lower thermal noise. As a consequence, the system SNR will not be sacrificed even if lower biasing current is used in the proposed system.

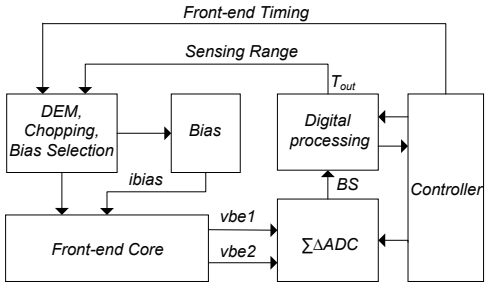

Fig. 1. Architecture of the proposed dual-range temperature sensor.

Fig.1 shows the architecture of the dual-range temperature sensor. Two diode-connected PNP transistors in the front-end core are used to generate the temperature signals, V_{be1} and V_{be2}, which are combined to produce a digital temperature representation by the subsequent readout circuitry (ADC). Meanwhile, output temperature reading T_{out} is reused to determine the front-end bias condition based on the sensor operating range.

B. Bias Current Selection

In order to achieve dual-range temperature sensing, two different BJT bias currents, I_{biasL} for the low temperature range (range L) to guarantee low supply operation and I_{biasH} for the high temperature range (range H) to maintain wide sensing range, are required. As stated in section II.A, the system SNR can be satisfied even if lower bias current is used in range L due to the simultaneous reduction in the thermal noise content. In this design, the bias currents I_{biasL} and I_{biasH} are optimized based on three factors: (i) $I_c \gg I_s$ as required in Eq.(1); (ii) the BJT current gain variation; and (iii) the allowable V_{be} signal amplitude. Sensor calibration is performed at room temperature so that no temperature controlled environment is required. An overlapping temperature for range L and range H (from 20°C to 30°C) is selected in order to achieve this.

As $I_s(T)$ increases exponentially with respect to temperature and can be in the order of pA at the upper bound of military temperature range (i.e. 125°C), an increase in I_c is required so that $I_c \gg I_s$ required by Eq. (1) holds. As a consequence, a large I_{biasH} is needed. On the contrary, I_s can be in the order fA at low temperature (i.e. -55°C), and a small I_{biasL} should suffice to ensure the same condition. The ratio I_{biasH}/I_{biasL} in the range of one to several hundred will not affect the V_{be} expression in Eq.(1) for the two sensing ranges.

As the PNP BJT is biased at the emitter side, a constant current gain β is required to guarantee the linearity of V_{be} [5]. To avoid non-uniform electron injection induced current gain variation, the bias current should neither exceed nor below certain values. Fig.2(a) shows the simulated current gain β of a diode-connected PNP transistor with respect to the emitter bias current I_e using the TSMC 0.18μm 1P6M technology. A $\leq \pm 10\%$ current gain variation (corresponding to ± 0.05°C sensing error after calibration) can be achieved with an emitter current ranges between $65pA \sim 230uA$.

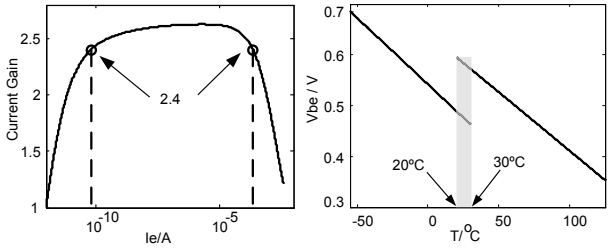

Fig. 2. (a) BJT current gain β w.r.t. I_e. (b) V_{be} dual-range signal w.r.t. temperature.

For the V_{be} amplitude limitation, the maximum V_{be} value is designed to be around 0.7V at -55°C so that a supply voltage of 0.9V can be achieved with consideration of the current source headroom. This corresponds to a $2nA$ emitter bias current I_{biasL}. Even though further scaling of I_{biasL} for even lower supply voltage is possible, the setting of V_{be} becomes a bottleneck if dynamic circuit technique in the front-end is utilized. For range H, I_{biasH} is selected based on the $I_c \gg I_s$ requirement, V_{be} signal distortion as well as overall system power optimization. Based on the the above considerations and the simulation result, a $125nA$ emitter bias I_{biasH} is selected. Notice that other bias current combinations should also be applicable based on different considerations. Fig.2(b) shows the simulated V_{be} dual-range signal under the chosen bias condition.

C. Ratio-metric Readout

From Eq.(1), the difference in base-emitter voltage ΔV_{be} between two BJTs operating at $n/1$ emitter current ratio and with $1/m$ emitter area ratio is

$$\Delta V_{be}(T) = \frac{kT}{q} \ln(m \cdot n), \tag{2}$$

which is a proportional-to-absolute-temperature (PTAT) and process independent signal. In this design, a current ratio of $n = 8$ is selected to enlarge the signal amplitude, while an emitter area ratio of $m = 1$ is used for better matching. By adding $V_{be}(T)$ with a scaled $\Delta V_{be}(T)$ ($\alpha \cdot \Delta V_{be}(T)$), a temperature independent bandgap reference voltage V_{bg} can be obtained and used as a pseudo reference to generate the digital representation of the sensed temperature. From simulation, $\alpha \approx 14.5$ is required for range L, and $\alpha \approx 13$ for range H. A charge balancing scheme using $\Sigma\Delta$ADC as shown in Fig.5 is adopted to perform temperature signal conversion for its moderate power consumption and achievable high resolution.

D. Calibration

The bias resistor R_{bias}, the BJT saturation current I_s and the current gain β are prone to PVT errors. Eq.(1) is rewritten as below considering these process variation effects:

$$V_{be}(T) \approx \frac{kT}{q} \ln[\frac{V_{bias} \cdot (\alpha_F + \Delta\alpha_F)}{(R_{bias} + \Delta R_{bias})(I_s + \Delta I_s)}] \approx \frac{kT}{q} \ln \frac{\alpha_F \cdot V_{bias}}{R_{bias} \cdot I_s} + \frac{kT}{q} \cdot (\frac{\Delta\alpha_F}{\alpha_F} - \frac{\Delta R_{bias}}{R_{bias}} - \frac{\Delta I_s}{I_s}) \quad (3)$$

where $\alpha_F = 1 - 1/\beta$ is the BJT common-base current gain; R_{bias} and V_{bias} are shown in Fig.3. From Eq.(3), these process variation effects will contribute to a PTAT error, which can be calibrated out at one temperature point [5]. As shown in Fig.2(b), sensor calibration is performed at room temperature. The sensor's operating range is initially controlled externally, and the two sensing ranges are calibrated separately at room temperature. After calibration, the sensor can select its operating range automatically by comparing its processed digital output with a preset T_{pre} value in the controller.

III. Temperature Sensor Implementation

A. Front-end Circuitry

With a 1/8 emitter current ratio, the ΔV_{be} signal has a constant slope of $175\mu V/°$C for TSMC 0.18μm 1P6M process. Current dynamic matching technique is adopted to meet the required $\pm 0.047\%$ current mirror matching accuracy, which contributes to a sensing error of $\pm 0.05°$C. However, due to the small I_{biasL} in range L, the V_{be} signal cannot settle within a sample period after a DEM event. A replica bipolar pair is thus implemented to meet the settling requirement with the two BJT pairs are alternatively used during conversion. Notice that our implementation can average out mismatch errors between the two BJT pairs as well. In range H, the replica BJT pair is turned off to save power. Signal up-conversion through chopping is performed at the two output voltage branches instead of at the bias currents due to settling considerations. The gain compensation current source and the sensor front-end circuitry with DEM are shown in Fig.3 and Fig.4, respectively. The total front-end current overhead is about $1.75\mu A$ for range L and $3.1\mu A$ for range H under 0.9V supply. Notice that most of the front-end power is consumed by the opamp ($\sim 1.5\mu A$).

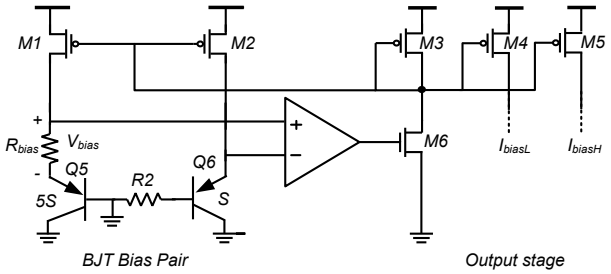

Fig. 3. Simplified BJT-core bias generation circuitry (start-up not shown).

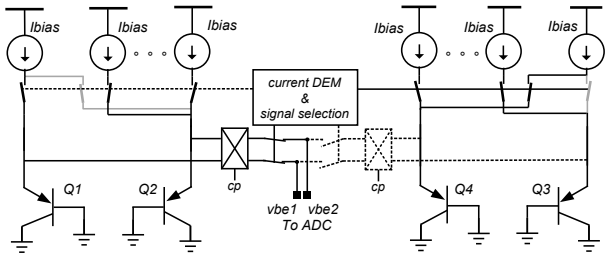

Fig. 4. (a) Front-end BJT pair with current DEM and signal chopping. (b) Front-end replica with different DEM timing.

B. $\Sigma\Delta$-based Readout Circuitry

1) Topology and Functionality: Comparing with other works using traditional sigma-delta modulator that requires high gain and power-hungry amplifier [5][6][7], this work adopts a class-C inverter based $\Sigma\Delta$ modulator [8] instead. Large signal-dependent current only flows during signal transitions, which lowers the overall static current of this modulator. Also, the inverter gain is increased at low supply voltage, improving the performance of the inverter based modulator. A second-order topology is selected to relieve ADC sampling speed and to reduce power overhead.

As shown in Fig.5, the modulator is reset to a known state before each conversion event, then one sampling and comparison event are executed. Based on comparator's digital output BS, the modulator decides to subtract V_{be} or not at the next sampling phase. If BS is low, only ΔV_{be} is integrated. If BS is high, $\Delta V_{be} - V_{be}$ is integrated. The internal feedback loop guarantees equivalent positive and negative charge integration to achieve charge balancing. The modulator output after decimation and gain compensation is

$$T_{out} = \frac{\Delta V_{be}}{(V_{be1} + V_{be2})/2};\ T_{compensated} = \frac{T_{out}}{1 + \alpha \cdot T_{out}} \quad (4)$$

2) Sigma-delta SC Implementation : Limited by the inverter voltage gain induced charge leakage, inverter-based $\Sigma\Delta$ADC topology cannot achieve very high resolution, and tradeoff must be made between conversion error and power consumption. Yet, a 12-bit resolution (corresponding to $\leq 0.2°$C quantization error) is still archievable. Using behavioral level simulation, a 76dB SNDR can be achieved with an oversampling ratio of 256 and a DC gain of 42dB for the two gain stages. Such gain requirement can be easily achieved using inverters with 0.9V supply. In circuit implementation, the input sampling capacitor is set to $1pF$ for $\frac{kT}{C}$ noise consideration. The sampling capacitor for the second integrator is reduced to $0.5pF$ to minimize chip area. Both the first and the second

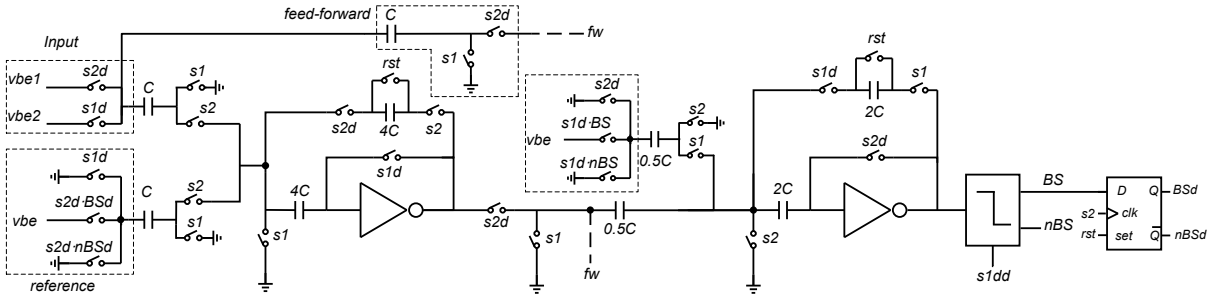

Fig. 5. Simplified inverter based 2nd-order $\Sigma\Delta$ ADC architecture (DEM switches not shown).

TABLE I
PERFORMANCE COMPARISON WITH THE PREVIOUSLY REPORTED IMPLEMENTATIONS.

Ref.	Technology	Supply voltage	Temperature range	Inaccuracy	Supply current	Sampling speed	Calibration
[5]*	0.7μm	2.5V $\sim$ 5.5V	-55°C$\sim$125°C	$\pm$0.1°C	75μA	10 Sa/s	1-point
[6]*	65nm	1.2V $\sim$ 1.3V	-70°C$\sim$125°C	$\pm$0.2°C	8.3μA	2.2 Sa/s	1-point
[7]*	32nm	1.05V	-10°C$\sim$110°C	$\leq$ 5°C	1.6mA	1k Sa/s	no-calibration
[10]*	0.16μm	1.5V $\sim$ 2V	-40°C$\sim$125°C	$\pm$0.25°C	6μA	10 Sa/s	1-point
This work#	0.18μm	0.9V	-55°C$\sim$125°C	$+1$°C/ $-$ 0.1°C	3.4μA/4.7μA	20 Sa/s	1-point

Note: *-measurement results; #-simulation results.

integrator gain is set to 0.25. A feed-forward architecture is adopted to maintain system stability and to relax the DC gain and output swing requirements for the inverter. Feed-forward gain is set to 0.5 to reduce the conversion time required for 12-bit resolution. DEM technique is adopted among the sampling capacitors to meet the 0.0219% matching accuracy required to limit temperature error resulting from capacitor mismatch to $\pm$0.05°C. All switches are controlled by boosted control signals for complete charge transfer. The readout block consumes an averaged current of 1.61μA during conversion. The sampling frequency is 128kHz and the conversion speed is 20 samples/s.

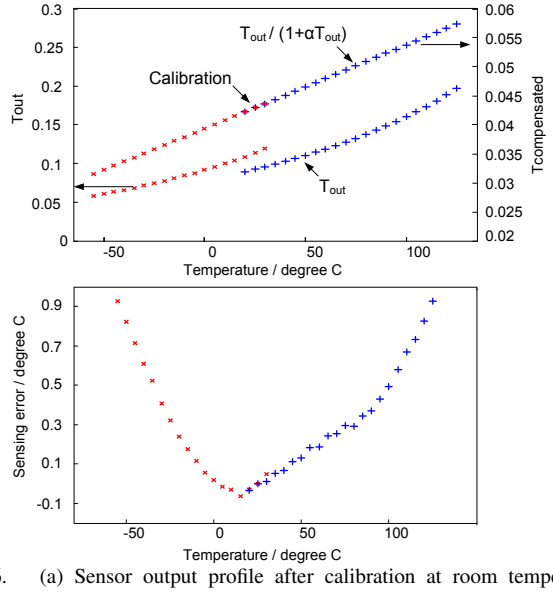

Fig. 6. (a) Sensor output profile after calibration at room temperature; (b) Sensing error within the full military range.

IV. Simulation Results

Fig.6 shows the simulated sensor system output from -55°C to 30°C and from 20°C to 125°C after decimation with a step of 5°C. The recovered temperature signal exhibits high linearity after gain compensation. After one-point calibration at 25°C, an error of $+1/-0.1$°C is achieved. The sensor consumes 3.4μA and 4.7μA in range L and range H, respectively. Table I presents the comparison of this work against the previously reported sensors.

V. Conclusion

A low-voltage low-power temperature sensor system is proposed in this work. A supply voltage of as low as 0.9V is achieved by adopting a dual-range sensing scheme together with a power efficient inverter-based $\Sigma\Delta$ modulator. An sensing inaccuracy of $+1/-0.1$°C is achieved over the full military range from -55°C to 125°C. Our design is suitable for wireless sensing applications such as multi-sensing platform, where ultra-low power consumption is of utmost importance.

References

[1] M. K. Law, A. Bermak, Howard C. Luong, "A Sub-μW Embedded CMOS Temperature Sensor for RFID Food Monitoring Application," *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 6, pp.1246 - 1255, Jun. 2010.

[2] P. Chen, C. Chen, C. Tsai, W. Lu, "A Time-to-Digital-Converter-Based CMOS Smart Temperature Sensor," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 8, pp.1642 - 1648, Aug. 2005.

[3] M. K. Law, A. Bermak, "A 405-nW CMOS Temperature Sensor Based on Linear MOS Operation," *IEEE Transactions on Circuits and Systems*, Vol. 56, No. 12, pp. 891 - 895, Dec. 2009

[4] S. Mahdi Kashmiri, M. A. P. Pertijs, K. A. A. Makinwa, "A Thermal-Diffusivity-Based Frequency Reference in Standard CMOS With an Absolute Inaccuracy of $\pm$ 0.1% From -55°C to 125°C," *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 12, pp. 2510 - 2520, Dec. 2010

[5] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS Smart Temperature Sensor with a 3σ Inaccuracy of 0.1°C from -55°C to 125°C, " *IEEE Journal of Solid-State Circuits*, Vol.40, No.12, pp. 2805 - 2815, Dec. 2005.

[6] Fabio Sebastiano, et al., "A 1.2V 10µW NPN-Based Temperature Sensor in 65-nm CMOS With an Inaccuracy of 0.2°C (3σ) From -70°C to 125°C," *IEEE Journal of Solid-State Circuits*, Vol.45, No.12, pp. 2591 - 2601, Dec. 2010.

[7] Y. W. Li, H. Lakdawala, et al. , "A 1.05V 1.6mW 0.45°C 3σ-resolution $\Sigma\Delta$-based temperature sensor with parasitic-resistance compensation in 32nm CMOS," *ISSCC*, pp.340 - 341,341a, Feb. 2009.

[8] Youngcheol Chae, Gunhee Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator," *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 2, pp.458 - 472, Feb. 2009.

[9] Richard Charles Jaeger, 1969. Low Frequncy Noise Sourcs In Bipolar Junction Transistors, Thesis (PhD). University of Florida.

[10] Kamran Souri, et al., "A CMOS Temperature Sensor with an Energy-Efficient Zoom ADC and an Inaccuracy of $\pm$0.25°C (3σ) from -40°C to 125°C," *ISSCC*, pp.309-311, Feb. 2010.