A 26.3 dBm 2.5 to 6 GHz Wideband Class-D Switched-Capacitor Power Amplifier with 40% Peak PAE

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***Abstract*—This paper describes a wideband class-D RF power amplifier (PA) featuring switched-capacitor (SC) modulation, a high-order LC-matching network (MN) and a reliability-aware supply-voltage boosting technique. Simulated in 65-nm CMOS at an elevated 3.2-V supply, the rms voltage stressed on each device is managed to be well within the reliability limits. The broadband coverage is from 2.5 to 6 GHz with peak power-added efficiency (PAE) of 40% at 26.4 dBm output power. After digital predistortion, the EVM is controlled <6.8% under the 16-QAM modulated test signals.**

I. INTRODUCTION

Power amplifier (PA) is the most power-consuming block in most RF systems. The power added efficiency (PAE) of the PA strongly affects the battery lifetime of mobile devices. Due to the ever-increment of data rate for modern wireless communications such as cellular and WLAN, the needs of larger RF bandwidth and higher peak-to-average power ratio (PAPR) PAs are growing. To transmit a high PAPR signal, the PA must operate in the back-off region to restore the linearity, which however results in lower output power and PAE. Moreover, wideband PAs are highly demanded for emerging software-defined radios that can be reconfigured easily support a wide range of applications in different bands [1]. Hence, the back-off PAE, peak output power and output bandwidth become the critical concerns of emerging PAs.

To address those issues, a number of circuit techniques were reported, e.g., pulse-width modulation PA [2], supply modulation PA [3] and switched-capacitor PA (SCPA) [4]. The back-off PAE of pulse-width modulated PA is not well-addressed due to the non-zero voltage switching characteristic of class-E PAs, and the supply modulation either requires multiple supplies with large current capability, or a bulky off-chip supply-noise filter. Among them, the SCPA should be more promising to achieve a high PAE and wideband linear output with proper matching network (MN) for high PAPR signals. Nevertheless, the power of the SCPA can be voltage-limited by the reliability concern of the devices.

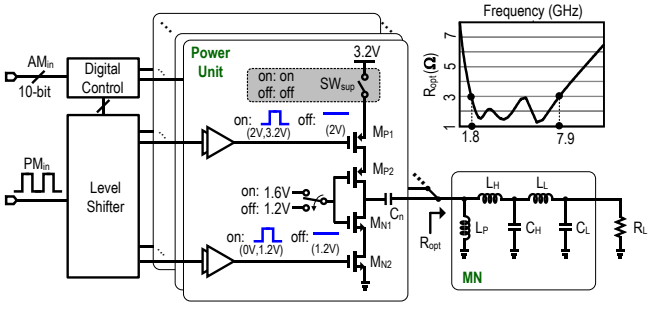

Fig. 1 Proposed wideband class-D SCPA with reliability-aware supply-voltage boosting technique applied to the power units. The bandwidth coverage is widened by adopting a 3rd-order LC MN. The input data is separated with 10-bit amplitude (AM_{in}) and phase (PM_{in}).

This paper describes techniques to surmount the reliability issues of SCPA such that the output power can be boosted by 98.34% (theoretically). We also address the design of a MN to extend the output bandwidth for broadband operation.

II. DESIGN CONSIDERATIONS OF SCPA

A. Conventional SCPA [4]

A typical SCPA uses a capacitor array (N) to modulate the output voltage amplitude by switching a number of (n) capacitors between the ground (V_{GND}) and supply (V_{DD}). The output voltage amplitude (V_{out}) is linearly modulated by the number of selected capacitors as:

$$V_{out} = \frac{2}{\pi}\left(\frac{n}{N}\right)V_{DD} \tag{1}$$

Thus, the output power (P_{out}) is given by,

$$P_{out} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{V_{DD}^2}{R_{opt}} \tag{2}$$

where R_{opt} is an optimal impedance transformed from 50Ω by the MN. The maximum power efficiency is fundamentally limited by the finite Q of the passive devices (e.g., inductors), the parasitics of CMOS devices and the switching loss of the power units.

According to (2), to improve P_{out}, one can reduce R_{opt} by enlarging the transform ratio but penalizing the PAE. Another way is to elevate the supply voltage, but it will be limited by the transistor reliability limits.

B. Proposed SCPA

For the proposed cascode class-D SCPA as shown in Fig. 1, it is engineered to withstand a high supply voltage of 3.2 V (maximum is 3.38 V). Theoretically, P_{out} can be improved by 98.34% under the same integrated size of transistors as the voltage of conventional solutions is limited to $2xV_{DD}$ (2.4 V in

1.2-V 65-nm CMOS). The circuit principle is detailed as follows. In the conventional SCPA, M_{N1} and M_{N2} are grounded during the off state, rendering the supply voltage directly stressing on M_{P1} and M_{P2}. Thus, the supply should not exceed $2xV_{DD}$ for reliability. Here, an extra switch SW_{sup} is added to divide the voltage stress on M_{P1} and M_{P2}. During the on state, the gate voltage of M_{P1} and M_{N2} are maintained at nominal value for preserving the gate-drain reliability. By switching the gate biases of M_{P2} and M_{N1} to different levels at different states, reliable operation of the SCPA is achieved.

For wideband operation, the SCPA employs a 3rd-order LC MN that can transform the optimal impedance R_{opt} within 1 to 3 Ω between 2.4 to 6 GHz. The pairs of L_HC_H and L_LC_L work as a wideband impedance converter that can keep a small R_{opt} in the covered band. To minimize the inductor's parasitic loss, a small inductance L_H should be chosen at the high-current path, while a large inductance L_L befits the low-current path. For impedance down-stepping, the high-current paths should be located at the source side. Thus, comparing with L_H, L_L is placed closer to the power units. Together with the capacitor array C_n, the inductor L_P transforms the load impedance to R_{opt} at lower frequency range (2.5 to 3 GHz).

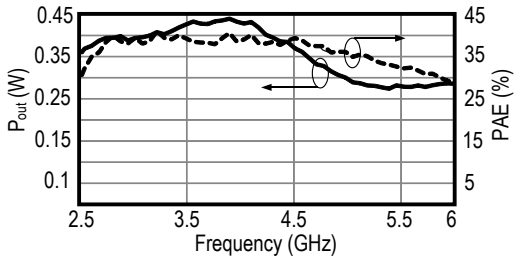

Fig. 2 Simulated PAE and P_{out} from 2.5 to 6 GHz.

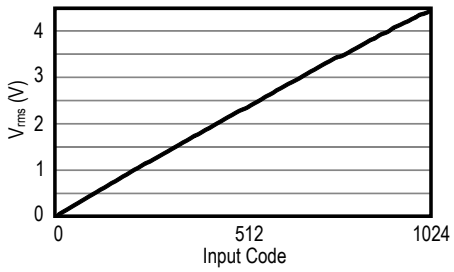

Fig. 3 Output V_{rms} versus input codes at 3.8 GHz.

III. SIMULATION RESULTS

The proposed wideband class-D SCPA is designed single-endedly in a 1.2-V 65-nm CMOS process. The simulated P_{out} and PAE from 2.5 to 6 GHz are shown in Fig. 2. At 3.8 GHz and at a 3.2-V V_{DD}, the peak P_{out} and PAE are 0.43 W (26.3 dBm) and 40%, respectively. The PAE and P_{out} degrade at higher frequency (4.5 to 6 GHz) mainly due to the increment of switching and parasitic loss in the power units. In the region of 2.5 to 2.8 GHz, the lowered PAE is caused by the existence of the 3rd harmonic.

For the output power (e.g., at 3.8 GHz) under wideband data modulation, the simulated AM-AM characteristic and the back-off PAE versus P_{out} are plotted in Fig. 3 and 4, respectively. The output amplitude is linearly modulated by the digital input codes, and the PAE is still up to 20% after 6-dB output power back-off. Compared with [4], the wideband operation limits the output power and PAE due to the use of a high-order LC MN. However, the elevated V_{DD} decisively recovers a high PAE and output power. With digital predistortion, the simulated EVM is <6.8% under the 16-QAM modulated test signals. Table 1 benchmarks this work with the recent work.

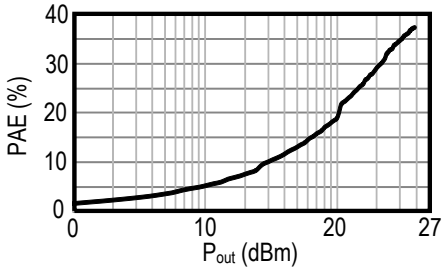

Fig. 4 PAE versus P_{out} at 3.8 GHz.

Table.1 Performance comparison with another SCPA [4].

	CMOS Process	Supply Voltages	Peak P_{out}	Output Bandwidth
[4] *	90 nm	1.5/3 V	25.2 dBm	1.9 to 2.9 GHz
This work #	65 nm	1.6/3.2 V	26.3 dBm	2.5 to 6 GHz

*Measurements #Simulations

IV. CONCLUSIONS

This paper has described the design and implementation of a P_{out}-improved wideband (2.5 to 6 GHz) class-D SCPA. It combines the SC modulation scheme with a 3rd-order LC MN and a supply-voltage-boosting technique to balance the key performance metrics, achieving a high P_{out} (26.3 dBm) and PAE (40%) in 65-nm CMOS.

ACKNOWLEDGEMENTS

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