An Analytical Linearization Method for CMOS MMIC Power Amplifier Using Multiple Gated Transistors

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Abstract: **In this paper, a novel analytical linearization method for CMOS MMIC power amplifier based on parallel connection of transistors (also named Multiple Gated Transistors) is proposed. By this method, the power amplifier's IMD_3 can be eliminated analytically by operating these transistors within the determined g_m'' linearized range. In order to demonstrate the proposed method usefulness, a 900 MHz Class AB power amplifier using 4 NMOS transistors with maximum aspect ratio (W/L)=1300/0.5 is designed based on 0.35 μm CMOS process. The simulated results demonstrate that –76dB IMD_3 can be obtained with 13dB as power gain.**

I. Introduction

The linearity of the MMIC power amplifier is of paramount importance for modern narrow band mobile communication system. Unlike the wide-band applications, unwanted harmonics may be easily filtered out. In the narrow-band application, harmonic non-linearity is of main concern. In particular, IMD_3 (3^{rd} Intermodulation Distortion) presents serious inference problem as this IMD_3 appears in the pass-band with other legitimate signal and this unwanted IMD_3 is not easily be filtered out [1]. In order to tackle this IMD_3, there are many techniques reported in the past few years [2-4]. Most of them rely on additional complex circuit to achieve MMIC power amplifier linearization. According to the topological similarities, there are three main techniques [5-7].

- Feedback
- Feedforward
- Predistortion

In order to reduce the circuitry complexity as addressed in the above approaches, a FET-level IMD_3 linearization method using multiple-gated transistors is proposed even there is little insight of the analytical design [8]. As such, an analytical linearization method for this multiple-gated transistors linearization is presented in this paper with the special emphasis on the IMD_3 and gain.

Besides this introduction, section *II* of this paper presents the analytical method for the power amplifier linearization technique using multiple-gated transistors whilst some simulation results based on 0.35μm CMOS process will be presented in section III in order to illustrate linearized power amplifier performance. Finally, the conclusion will be drawn in section IV.

II. Analytically Linearization Method

In this section, an analytical linearization technique is proposed based on the multiple- gated transistors approach [8]. By the Taylor series, the drain current i_{DS} of a MOSFET is related to the gate-source voltage and drain source voltage, it can be described as follows:

$$i_{DS}(v_{gs}) = I_{DC} + g_m v_{gs} + \frac{g_m'}{2} v_{gs}^2 + \frac{g_m''}{3!} v_{gs}^3 + \ldots \quad (1)$$

where g_m represents the transconductance of the MOSFET. From Eq. (*1*), it is obvious that IMD_3 will be directly related to v_{gs}^3. As such, its coefficient plays an important role to the power amplifier linearization. Two conventional MOSFETs' g_m'' subject to different bias conditions is plotted in Fig. 1. Both of them show one positive peak and one negative peak as depicted in Fig.1.

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It can be noticed that most of the MOSFET based amplifiers will be biased at saturation region as the situation of MOSFET1. Therefore, amplifier's IMD_3 will be mainly resulted from the negative peak of $g_m^{''}$. The reduction of this negative peak from maximum value to zero intuitively implies the IMD_3 elimination. In order to achieve this IMD_3 reduction, an auxiliary MOSFET2 is arranged in parallel with MOSFET1 and a Class AB power amplifier circuitry based on this parallel multiple-gated transistors is constructed and shown in Fig. 2(a) and Fig. 2(b) respectively. According to the proposed approach, the dash-block in Fig. 2(b) is replaced by the multiple-gated transistors configuration in Fig. 2(a). The negative peak of the MOSFET1's $g_{m1}^{''}$ can be cancelled by the MOSFET2's $g_{m2}^{''}$ positive peak value subject to different bias points as shown in Fig. 3. Moreover, a linearized range of the composite $g_m^{''}$ as depicted in Fig. 3 is resulted and so IMD_3 can be significant reduced if the amplifier is operated in this range.

The key analysis issue is then the analytical determination of the above linearized range. In fact, the bias voltage V_{GS2} of MOSFET2 should be chosen as follows:

$$V_{GS2} = V_{GS1} - \Delta V_{GS} \qquad (2)$$

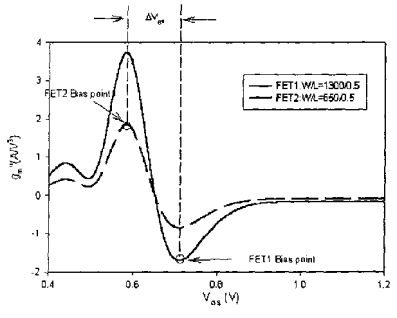

Fig. 1 DC characteristics of 2 MOSFETs

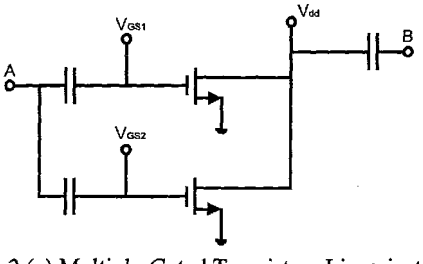

Fig. 2 (a) Multiple-Gated Transistors Linearization Configuration

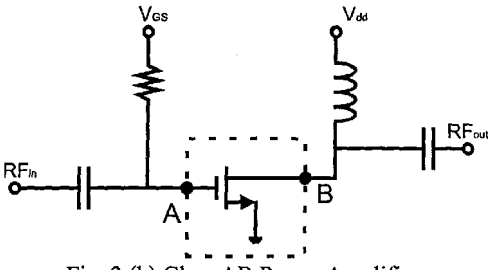

Fig. 2 (b) Class AB Power Amplifier

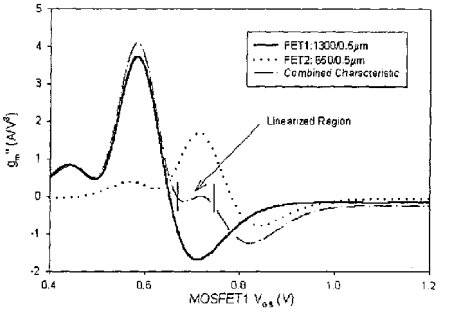

Fig. 3 $g_m^{''}$ Cancellation by 2 MOSFETs

In addition, the positive peak of MOSFET1 could be located at a value of $V_{GS1} = x_1$ such that

$$\left.\frac{\partial g_{m1}^{''}}{\partial v_{GS1}}\right|_{v_{GS1}=x_1} = 0 \text{ and } \left.\frac{\partial^2 g_{m1}^{''}}{\partial v_{GS1}^2}\right|_{v_{GS1}=x_1} < 0 \qquad (3)$$

As such, there are two values of V_{GS1} satisfying the above criteria, denoted as $g_{m1}^{''}(x_1)$, one in the cutoff region and one slightly greater than V_{th}. The one in the cutoff region is ignored because the MOSFET1 will not biased at this region in general.
Similarly, the negative peak determination is as follows:

$$\left.\frac{\partial g_{m1}^{''}}{\partial v_{GS1}}\right|_{v_{GS1}=x2} = 0 \text{ and } \left.\frac{\partial^2 g_{m1}^{''}}{\partial v_{GS1}^2}\right|_{v_{GS1}=x2} > 0 \qquad (4)$$

Also, there are two values of V_{GS1} satisfying the above criteria, denoted as $g_{m1}^{''}(x_2)$,one in subthreshold region and this is always ignored. Then, the suitable region is saturation ones.

Therefore, the required linear range is determined by

$$\Delta V_{GS} = |x_1 - x_2| \qquad (5)$$

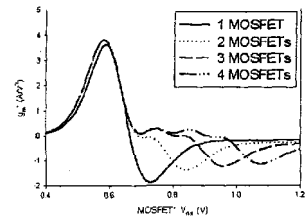

Fig. 4 g_m''' Cancellation by Multiple MOSFETs

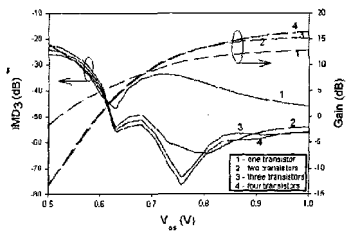

Fig.5 Simulation result of the power gain vs. the IMD_3

It is also true that multiple MOSFETs connected in parallel will increase this linear region as shown in Fig. 4.

III. Simulation Results

To verify the above, four power amplifiers using multiple-gated transistors linearization method are simulated based on conventional 0.35μm CMOS technology [9-10]. The MOSFET1 is biased at V_{GS1} and the other transistors are biased evenly from V_{GS1} respectively. This implies that MOSFET2 is biased at V_{GS1}-0.14V and so forth. The bias point of MOSFET1 is at the center of the linearized region. The gate lengths of different MOSFETs are all 0.5 μm, and the widths are 1300μm, 650μm, 500μm, and 420μm respectively. All of the bias differences and the sizes are determined according to the above analysis. The RF performance of the amplifier are tested by applying two-tone signals input of 900 and 905MHz with input power of −15 dBm and the supply voltage of 4V.

From Fig. 5, it is obvious that power amplifier with 4 MOSFETs can obtain superior IMD_3 (about −76dB) and power gain as high as 13dB subject to V_{GS1} = 0.75V. As such, this confirms the usefulness of the power amplifier using multiple-gated transistor linearization method.

IV. Conclusion

An analytical linearization method for MMIC power amplifier is presented in this paper. The required linearized range for the g_m''' is derived and illustrated by 4 power amplifiers. It is reported that power amplifier with 4 MOSFETs connected as multiple-gated structure offers IMD_3 as good as −76dB and power gain as high as 13dB.

Acknowledgments

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Reference

[1] Peter B. Kenington, *High-Linearity RF Amplifier Design*, Artech House, 2000.

[2] Cheon Soo Kim, Min Park, Chung-Hwan Kim, Yeong Cheol Hyeon, Hyun Kyu Yu, Kwyro Lee and Kee Soo Nam, "A Fully Integrated 1.9-GHz CMOS Low-Noise Amplifier," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 8, pp. 293–295, Aug. 1998.

[3] Robert H. Caverly, Scott Smith and Jiangang Hu, "RF CMOS Cells for Wireless Applications," *Analog Integrated Circuits and Signal Processing*, 25, pp. 5–15, Kluwer Academic Publishers, 2000.

[4] Ravi Gupta, David J. Allstot, "Fully Monolithic CMOS RF Power Amplifiers: Recent Advances," *IEEE Communications Magazine*, vol.37, no. 4, pp. 94–98, April 1999.

[5] Youngsik Kim, Youngoo Yang, Sanghoon Kang, Bumman Kim, "Linearization of 1.85GHz Amplifier Using Feedback Predistortion Loop," *Microwave Symposium Digest, 1998 IEEE MTT-S International*, vol. 3, pp. 1675–1678, 1998.

[6] Yusheng Chen, Boon Poh Ng, Kot, A.C., "Adaptive algorithms for feed-forward power amplifier linearizer,", *Microwave Symposium Digest. 2000 IEEE MTT-S International*, vol.1, pp. 485–488, 2000.

[7] Faulkner, M., "Amplifier linearization using RF feedback and feedforward techniques," *Vehicular Technology, IEEE Transactions on*, vol. 47, no. 1, pp. 209–215, Feb. 1998.

[8] Bonkee Kim, Jin-Su Ko, and Kwyro Lee, "A New Linearization Technique for MOSFET RF Amplifier Using Multiple Gated Transistors," *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 9, pp. 371–373, September 2000.

[9] Y. Cheng, M.C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P. K. Ko and C. Hu, "A Physical and Scalable I-V model in BSIM3v3 for Analog/Digital Circuit Simulation," *IEEE Trans. on Electron Devices*, vol. 44, no. 2, pp. 277–287, Feb 1997.

[10] *Cadence Spectre Reference*, Cadence Design Systems Inc., 1998.