Capacitive Floating Level Shifter: Modeling and Design

Wen-Ming Zheng[1,2], Chi-Seng Lam[1,2], Sai-Weng Sin[1,2], Yan Lu[1], Man-Chung Wong[1,2], Seng-Pan U[1,2], R.P. Martins[1,2,3]

1 - *State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China*

2 - *Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macao, China*

3 – *On leave from Instituto Superior Técnico, Universidade de Lisboa, Portugal*

E-mail: cslam@umac.mo or C.S.Lam@ieee.org

***Abstract*—This paper introduces the failure operation principle of the capacitive floating level shifter, as well as its simplified circuit model. Based on the model, the mathematical equations for analyzing the level shifter's characteristics and its respective performances are also derived. Design criteria for the capacitive floating level shifter are proposed derived from the model and corresponding MATLAB simulation results. Furthermore, transistor-level simulations using 65-nm CMOS technology verify the deduced simplified circuit model and the proposed design criteria, following which, overdesign can be avoided to guarantee the proper operation of the floating capacitive level shifter, thus saving chip area and reducing cost.**

***Keywords*—level shifter; floating level shifter; DC-DC converter; switched-capacitor; fully-integrated**

I. INTRODUCTION

Level shifters are used in applications where there is a need to interface between different voltage domains. There are two types of level shifters: full-swing and floating, which can be distinguished by whether the voltage domains share a common ground potential or not. Floating level shifters are used to shift the potential of control signals from circuits powered by low voltage power rails to the potential of circuits with floating power and ground rails [1]. Thus floating level shifters are often used in the gate drivers to drive power output stages in applications such as DC-DC converters, biomedical transducer drivers, Class-D audio amplifiers, MEMS, and LCD drivers[1]-[4]. Fig. 1(a) shows the basic floating level shifter circuit. As analyzed in [5], this type of level shifter cannot operate at high speed, and consumes high power and a large layout area. To cope with the speed problem, two capacitors can be added in parallel with the stacked transistor [6]-[8], as shown in Fig. 1(b) and (c), which further increases the layout area. The improved floating level shifters presented in [1], [5], [9] exhibit significant improvements in speed and layout area, but they are more complex and a control signal is required to set their initial state, which may not be suitable in some applications [10]. Furthermore, the improved floating level shifters presented in [1], [10]-[12] either consume static power or need additional pulse generation circuits, which also increases the level shifter circuit complexity.

A capacitive floating level shifter as shown in Fig. 2 was proposed by Tanzawa *et.al* in 2002 [13], in which the stacked transistors are eliminated when compared with Fig.1(c). This circuit is composed of three parts, a latch holding the level shifted voltage, two coupling capacitors connected with the latched nodes, and two inverters driving the coupling capacitors. This type of capacitive level shifter is simpler, and the chip area, current consumption and propagation delay are also small [4]. However, this capacitive level shifter may fail to operate if not designed properly. Among the existing circuit structures, only a rough and limited analysis of this type of level shifter can be found in [4] and [13]. In this paper, a complete analysis about the capacitive floating level shifter is presented, highlighting how to guarantee its normal operation and dynamic performances without overdesigning the size of its MOS transistors and capacitors. In section II, the failure operation principle of the capacitive floating level shifter is first introduced and its simplified circuit model is constructed. Based on this simplified circuit model, the mathematical equations for analyzing the level shifter's characteristics and performances are derived. To verify this circuit model, simulations are performed with MATLAB. Based on the model and the simulation results, the design criteria for the capacitive floating level shifter are proposed. In section III, transistor level simulations using 65-nm CMOS technology are provided to verify the deduced simplified circuit model and the proposed design criteria.

II. CAPACITIVE FLOATING LEVEL SHIFTER ANALYSIS

A. Failure Operating Principle

From Fig. 2, assume that the initial conditions for the circuit nodes *In*, n_1, *Out*, n_2 and *out_shift* are: *In* low, n_1 high, *Out* low, n_2 high, *out_shift* low. When *In* goes from low to high, n_1 is pulled down to GND and *Out* is pulled up to high. If C_b or the on-resistance of inverter *I*3 and *I*4 is sufficiently large, the changes of the voltage difference across the capacitor C_b will be small, then n_2 and *Out_Shift* will follow n_1 and *Out* to rise or fall approximately by the amplitude of V_{DDL}, respectively. If n_2 and *Out_Shift* rises or falls to the switching threshold [15] of the inverter *I*3 and *I*4, the state of the cross-coupled latch will change due to the positive feedback. In contrast, if C_b and the on-resistance are small, when n_2 and *Out_Shift* rises or falls following n_1 and *Out,* there will be large current discharging or charging C_b through the on-resistance, resulting in large changes of the voltage

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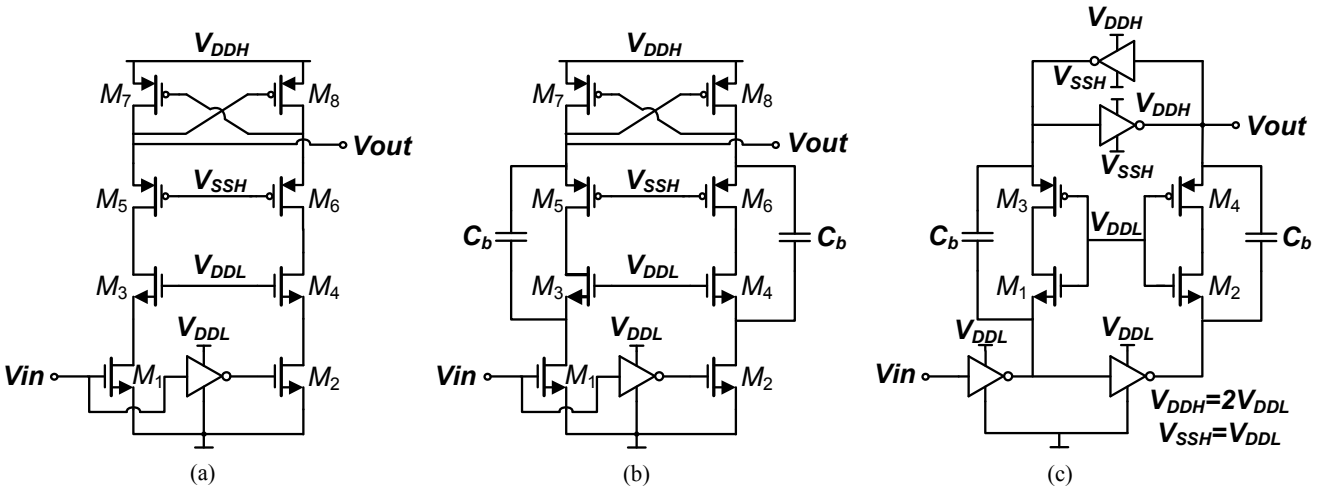


Fig. 1. (a) Basic floating level shifter [5], (b) basic floating level shifter with bootstrap capacitor [6], (c) 0-VDD to VDD-2VDD floating level shifter [7].

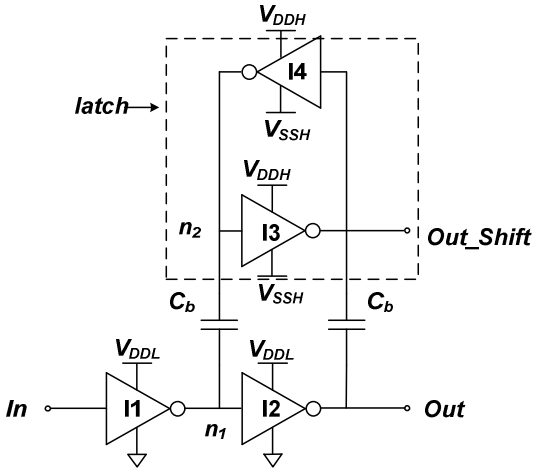


Fig. 2. Capacitive floating level shifter [13].

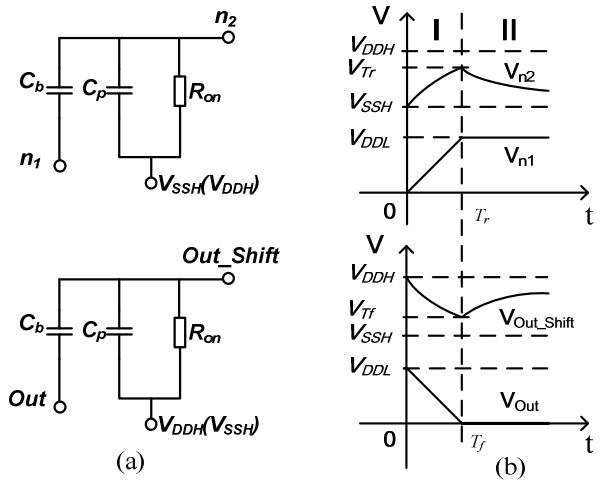


Fig. 3. (a) A simplified circuit model of the capacitive floating level shifter (b) its charging and discharging behavior.

difference across the capacitor C_b, then there is a chance that n_2 and *Out_Shift* will not reach the switching threshold to invert the latch via positive feedback, thus the level shifter fails to operate properly.

B. Simplified Circuit Model

To define the design criteria that will ensure the proper operation and performance of the capacitive floating level shifter, a simplified model is constructed, with the equivalent circuits at node n_2 and *Out_Shift* shown in Fig. 3(a), respectively, which are identical. The only difference is related with the fact that when the signal is low at one node it will be high at the other, and vice versa. In this model, C_p is the total parasitic capacitance at node n_2 or *Out_Shift*, and R_{on} represents the on-resistance of the transistors of both inverters *I*3 and *I*4. The equivalent circuit at node n_2 or *Out_Shift* is modeled by the parallel connection of C_p and R_{on}. The other terminal of C_p and R_{on} connects to V_{SSH} when V_{n2} is low, while to V_{DDH} when V_{n2} is high. This model only considers that the voltage rise or fall at node n_2 or *Out_Shift* is only caused by the voltage rise or fall at node n_1 or *Out*, and the inverter is only represented by its parasitic capacitance C_p and on-resistance R_{on}, not considering its dynamic characteristics. Then, V_{n2} will stop rising and begin to fall as V_{n1} reaches its steady state when the effects of V_{Out_Shift} and V_{Out} are not counted, V_{Out_Shift} will stop falling and begins to rise as V_{Out} reaches its steady state without the effects of V_{n2} and V_{n1}, and vice versa, as shown in Fig. 3(b). Actually, when both V_{n2} and V_{Out_Shift} reach the switching threshold of the inverter, they continue to rise or fall due to the positive effect of the cross-coupled inverter.

Assuming the voltage at node $n_1(V_{n1})$ and $Out(V_{Out})$ rises or falls linearly, V_{n2} can be obtained by KCL at node n_2 where current flows through C_b to node n_2 is equal to the current flowing from n_2 into C_p and R_{on}. In region I, as shown in Fig. 3(b), when V_{n1} rises linearly (i.e., $\frac{dV_{n1}(t)}{dt}$ is a positive constant), using KCL at node n_2 leads to,

$$C_b \frac{d\left[V_{n1}(t)-V_{n2}(t)\right]}{dt} = C_p \frac{dV_{n2}(t)}{dt} + \frac{V_{n2}(t)-V_{SSH}}{R_{on}} \quad (1)$$

Solving (1),

$$V_{n2}(t) = R_{on} * C_b \frac{dV_{n1}(t)}{dt} * \left(1 - e^{\frac{-t}{R_{on}(C_b+C_p)}} \right) + V_{SSH},\ (0 \le t \le T_r) \quad (2)$$

In region II as shown in Fig. 3(b), V_{n1} reaches its steady-state ($\frac{dV_{n1}(t)}{dt}$ =0), (1) thus becomes,

$$-C_b \frac{dV_{n2}(t))}{dt} = C_p \frac{dV_{n2}(t)}{dt} + \frac{V_{n2}(t)-V_{SSH}}{R_{on}} \quad (3)$$

T_r is the rise time of V_{n1}, and if the voltage at time T_r is V_{Tr}, solving (3) implies,

$$V_{n2}(t) = (V_{T_r} - V_{SSH}) * e^{\frac{-(t-T_r)}{R_{on}(C_b+C_p)}} + V_{SSH},\ (t \ge T_r) \quad (4)$$

In this model, it is only considered that the voltage at node n_2 is pulled up by the rise of V_{n1} (charge pump effect), and V_{n2} will begin to fall in region II, as Fig. 3(b) and (4) illustrate.

When V_{n1} rises, V_{Out} will fall due to the effect of the inverter $I2$. Similarly, assuming V_{Out} falls linearly, using KCL at node *Out_Shift* and solving the resulting differential equations, V_{Out_Shift} can be obtained as follows,

$$V_{Out\_Shift}(t) = R_{on} * C_b \frac{dV_{Out}(t)}{dt} * \left(1 - e^{\frac{-t}{R_{on}(C_b+C_p)}} \right) + V_{DDH},\ (0 \le t \le T_f) \quad (5)$$

$$V_{Out\_Shift}(t) = (V_{T_f} - V_{DDH}) * e^{\frac{-(t-T_f)}{R_{on}(C_b+C_p)}} + V_{DDH},(t \ge T_f) \quad (6)$$

where T_f is the fall time of V_{Out}, V_{Tf} is the voltage at time T_f. On the other hand $\frac{dV_{Out}(t)}{dt}$ is a negative constant in (5), because V_{Out} falls linearly.

The case where V_{n1} falls and V_{Out} rises linearly is similar as the above.

C. Simulation and Analysis with MATLAB

The above equations based on the simplified level shifter model can be simulated with MATLAB, assuming that V_{n1} rises linearly and V_{Out} falls linearly. The case where V_{n1} falls and V_{Out} rises both linearly are similar. Furthermore, the propagation delay of inverter $I2$ also plays an important role in the proper operation of the level shifter, as it will be illustrated and discussed later.

Table I shows a set of capacitive floating level shifter parameters for MATLAB simulation. It is assumed that the capacitances of two C_b, R_{on} of $I3$ and $I4$ in Fig.2 are the same. T_d represents the propagation delay of inverter $I2$. Fig. 4(a) shows the corresponding MATLAB simulations. From Fig. 4(a), it is clearly seen that when the voltage V_{n1} rises, V_{n2} rises until V_{n1} stops rising, then V_{n2} begins to fall. V_{Out} falls and V_{Out_Shift} falls until V_{Out} stops falling, then V_{Out_Shift} begins to rise. Supposing that the switching thresholds of the inverters $I3$ and $I4$ are at the middle of the voltage level (1.8V in this case) to shift to, which is optimal for inverting the latch, and V_{n2} and V_{Out_Shift} is pulled down or pulled up only via C_b, then the region to reliably invert the latch is the area enclosed by the black lines (V_{n2} and V_{Out_Shift}) as shown in Fig. 4(a). Within this area, the pull up voltage is greater than the required switching threshold (1.8V) while the pull down voltage is less than the switching threshold, simultaneously, which will definitely change the state of the latch via positive feedback. Therefore, if this condition is satisfied, the level shifter can operate properly. In Fig. 4(b), when C_b decreases to 60fF, V_{n2} and V_{Out_Shift} never reach the switching threshold, there is no area enclosed by V_{n2} and V_{Out_Shift}, thus the level shifter can fail to operate.

It should be noted that in Fig. 4(a), V_{n2} stops rising and begins to fall, V_{Out_Shift} stops falling and begins to rise due to the simplified model which only considers the charge pump effect without taking into account the dynamics and positive feedback of the inverters $I3$ and $I4$. In reality, V_{n2} will rise to 2.4V and V_{Out_Shift} will fall to 1.2V in the case of Fig. 4(a). The cases exhibited in Fig. 5 are similar.

To determine the effects of other parameters (T_d, R_{on}, T_r, C_p) on the level shifter proper operation and performances, Fig. 5(a) shows the simulation results when the propagation delay of the inverter $I2$ is changed to T_d=20ps while keeping other parameters unchanged. When compared with Fig. 4(a), it clearly shows that the region to reliably invert the latch becomes smaller and the time required for V_{n2} and V_{Out_Shift} to reach the switching threshold, simultaneously, becomes longer as T_d increases. If T_d is further increased, there will be no enclosed area, and then the level shifter can fail to operate. Fig. 5(b) shows the case when only R_{on} is increased to 500Ω, the enclosed area becomes wider and the time becomes shorter, Fig. 5(c) and (d) show the situation when V_{n1} rise time Tr is increased to 70ps and C_p is increased to 50fF respectively, both enclosed areas become smaller and the time longer, when compared with Fig. 4(a).

TABLE I. CAPACITIVE FLOATING LEVEL SHIFTER PARAMETERS (*MATLAB* SIMULATION)

T_r(ps)	R_{on}(Ω)	C_b(fF)	C_p(fF)	T_d(ps)	V_{SSH}(V)	V_{DDH}(V)
50	300	200	20	0	1.2	2.4

D. Design Procedures

Based on the previous analysis and simulation results, the following design considerations for capacitive floating level shifter are summarized for sizing MOS transistors of the inverters $I1$, $I2$, $I3$ and $I4$ and C_b.

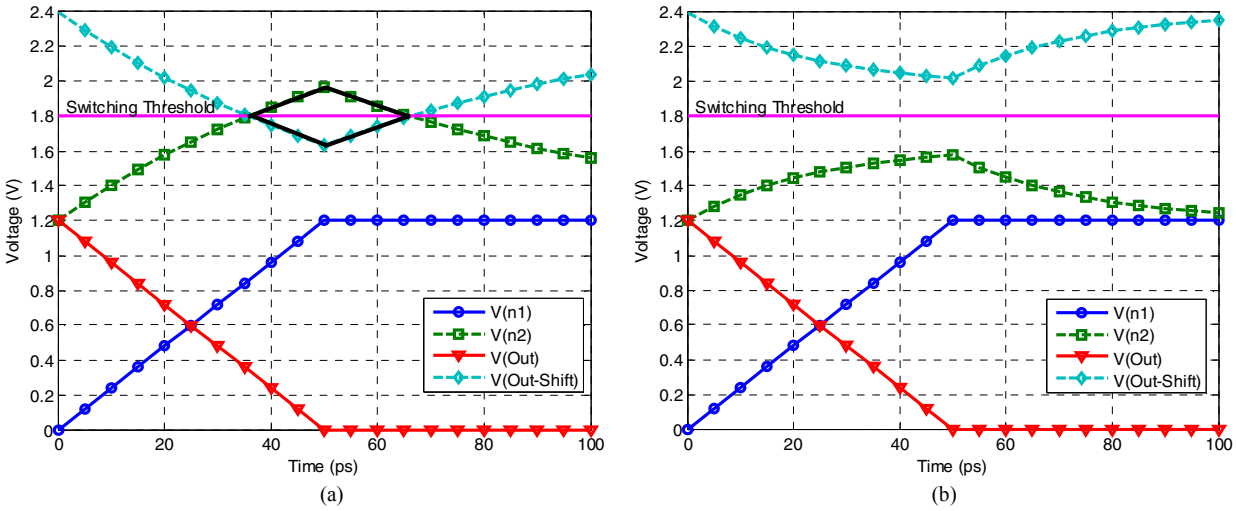


Fig. 4. MATLAB simulation results of V_{n2} and V_{Out_Shift} when (a) C_b=200fF and (b) C_b=60fF.

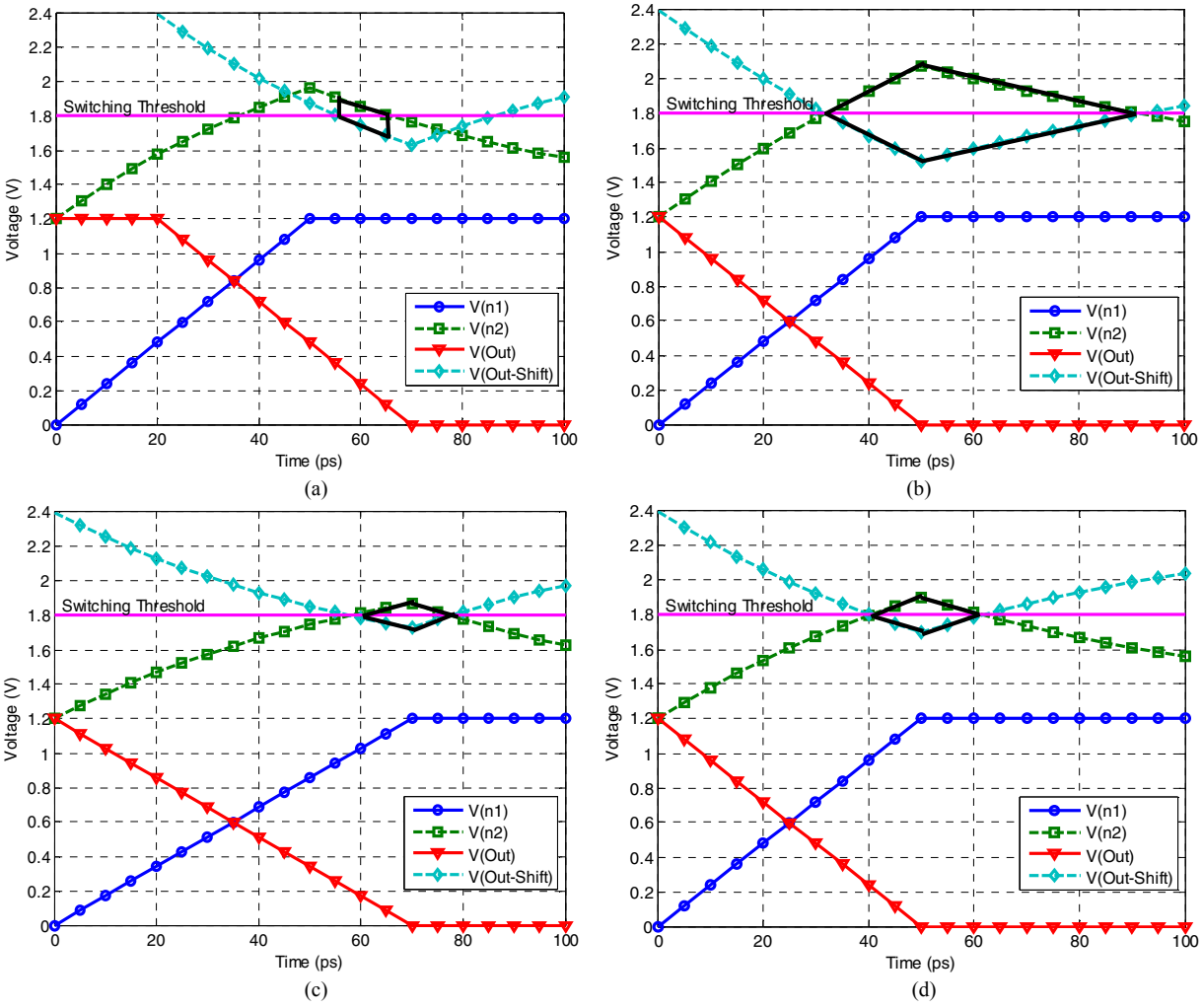


Fig. 5. MATLAB simulation results of V_{n2} and V_{Out_Shift} when (a) T_d=20ps, (b) R_{on}=500Ω, (c) T_r=70ps and (d) C_p=50fF, while other parameters are the same as Fig. 4(a).

1). Determining the size of I1 and I2: When R_{on} is sufficiently large, V_{n2} and V_{Out_Shift} will follow V_{n1} and V_{Out} to keep the voltage difference across C_b almost constant. However, large R_{on} turns the inverter more sensitive to noises and disturbances. Typical values of R_{on} for a well-designed inverter are in the kΩ range [15]. Then, the size of the MOS transistor for inverters *I*3 and *I*4 can be determined according to R_{on}(in kΩ range) and the switching threshold. The switching threshold should be at the middle of the floating voltage level (V_{DDH} and V_{SSH}), which is optimum to invert the latch.

2). Determining the size of I3 and I4: When R_{on} or C_b is sufficiently large, V_{n2} and V_{Out_Shift} will follow V_{n1} and V_{Out}. The rise time and fall time of *I*1 and *I*2 can be determined to be equal to the desired level shifter output rise and fall times. Then, the size of *I*1 can be determined according to the fall time and rise time and the total parasitic capacitance at node n_1 and n_2, and the size of *I*2 can be obtained according to the fall and rise times and the total parasitic capacitance at node *Out* and *Out_Shift* (the load capacitor should be included). Considering the propagation delay of *I*2, the design margin of the size of *I*1 and *I*2 should be considered.

3). Determining the capacitance of C_b: C_b can be obtained with the help of (2) and (5) in such a way that V_{n2}(t) and V_{Out_Shift} can reach the switching threshold voltage. Also, the design margin should be counted.

4). Fine tune the level shifter: If the rise and fall times of the level shifter output are not satisfied the required specifications, of *I*1 and *I*2, *I*3 and *I*4 can be simultaneously scaled up in order to meet the desired performance, while keeping C_b unchanged. To meet the delay requirements, it is necessary either to scale up *I*1 and *I*2 or C_b.

III. Simulation Results

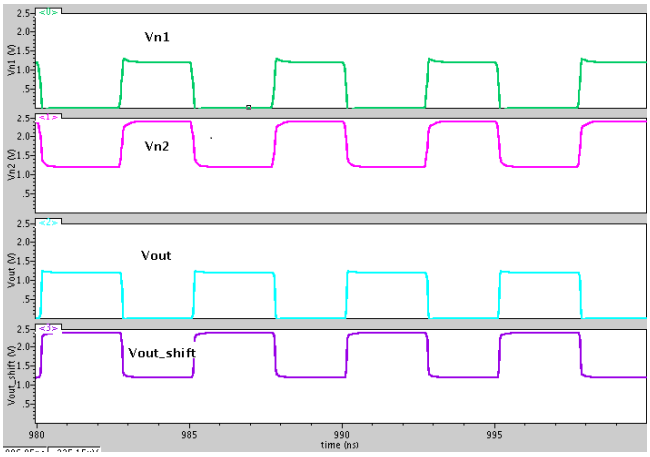
To verify the deduced model and previous failure operation analysis, the transistor level of the capacitive floating level shifter circuit are built using a STM 65nm CMOS process, shifting the input signal ranging from 0-1.2V to 1.2-2.4V.

A set of designed parameters for simulating the level shifter performances are summarized in Table II, in which those designed parameters' values are also used to obtain the conditions of Fig. 4(a). The load capacitance of the level shifter C_L=10fF, which represents the input capacitance of the output buffer of the level shifter.

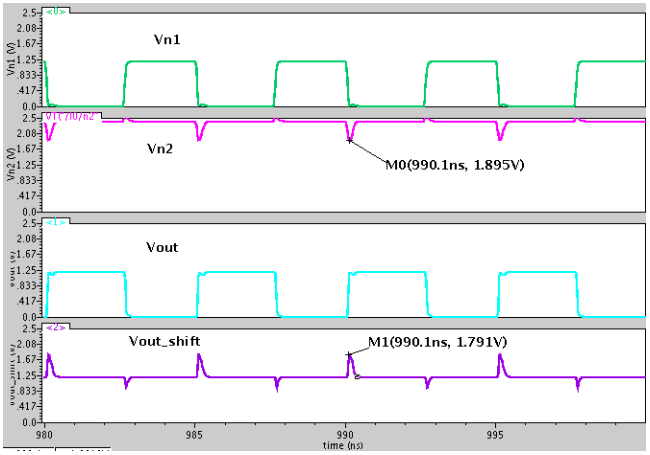
TABLE II. Designed Level Shifter Parameters for Simulation

Component	Type of MOS		*W(μm)(L=0.06μm)*	
*I*1	P	N	3	1.2
*I*2	P	N	3	1.2
*I*3	P	N	2	0. 8
*I*4	P	N	2	0. 8
C_b	200fF			
C_p	20fF			

Fig.6 shows the simulated waveforms of the level shifter based on the parameters from Table II. The simulated rise time T_r and fall time T_f of V_{n1} and V_{Out} are close to 50ps, and the propagation delay T_d of *I*2 is approximately 20ps. The level shifter operates properly as Fig.6 shows. Fig.7 shows the simulation results when C_b decreases to 60fF. It is obvious that when V_{n1} falls, V_{n2} only falls up to 1.89V, and V_{Out_Shift} only rises to 1.79V, thus they do not have enclosed area as indicated in Fig. 4(b), therefore, the level shifter fails to operate properly in this situation.



(a)



(b)

Fig. 6. Simulated waveforms of the level shifter with (a) C_b=200fF, (b) C_b=60fF (From top to bottom: V_{n1}, V_{n2}, V_{Out}, V_{Out_Shift}).

The level shifter can be redesigned according to the proposed design procedures of section II in order to shift the input signal from 0-1.2V to 1.2-2.4V.

- First, with R_{on} in the kΩ range, then the NMOS width of *I*3 and *I*4 can be chosen approximately as the minimum value according to the CMOS process, and the PMOS width of *I*3 and *I*4 is chosen according to the NMOS width and the switching threshold (1.8V).
- Supposing the rise and fall times of the level shifter output are required to be less than 50ps, and the load capacitance of the level shifter C_L=2fF, after calculation, the minimum size is sufficient for *I*1 and *I*2 to meet the requirements.
- After determination of the size of the four inverters, C_b can be determined using Eq.(2) or Eq.(5) such that V_{n2}(t) and

V_{Out_Shift} can reach the switching threshold voltage (1.8V). The calculated C_b is close to 12fF, and C_b=20fF is chosen, considering the design margin and the propagation delay of $I2$.

The designed parameters according to the proposed design procedures are summarized in Table III. The corresponding simulation results are shown in Fig. 7. The rise and fall time of V_{n1}, V_{Out} and V_{Out_Shift} are 64ps, 37ps and 48ps respectively, which meets the design target. It should be noted that following the proposed designed procedures, the approximate minimum sizes of the inverters already meet the requirements, which can avoid overdesign, thus saving chip area and reducing cost.

TABLE III. PARAMETERS OF THE LEVEL SHIFTER DESIGNED ACCORDING TO THE PROPOSED DESIGN PROCEDURES

Component	Type of MOS		*W(μm)(L=0.06μm)*	
$I1$	P	N	0.34	0.135
$I2$	P	N	0.34	0.135
$I3$	P	N	0.34	0.135
$I4$	P	N	0.34	0.135
C_b	20fF			
C_p	≈2fF			

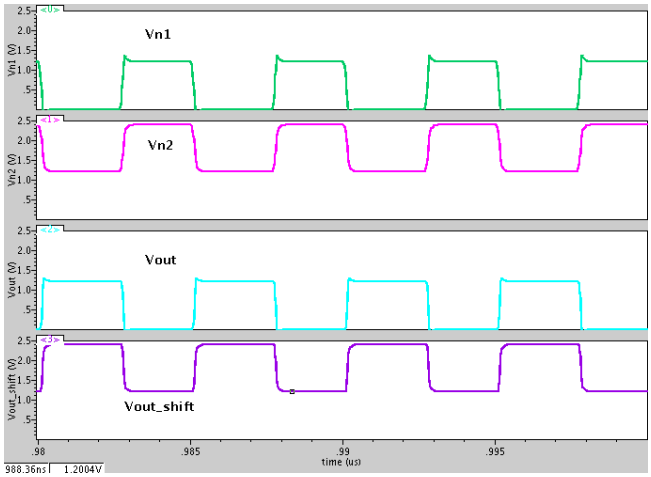


Fig. 7. Waveforms of the level shifter designed following the proposed design procedures. (From top to bottom: V_{n1}, V_{n2}, V_{Out}, V_{Out_Shift}).

IV. CONCLUSIONS

In this paper, the failure operation principle of the capacitive floating level shifter has been introduced and its simplified circuit model constructed. Based on it, the mathematical equations for analyzing the level shifter's characteristics and performances were derived. To verify this circuit model, simulations were performed with MATLAB. With the model and simulation results the design criteria for the capacitive floating level shifter has been proposed. Finally, transistor-level simulations using an ST 65-nm CMOS technology verified the deduced simplified circuit model and the proposed design criteria, following which, overdesign can be avoided to guarantee the proper operation of the floating capacitive level shifter, thus saving chip area and decreasing cost.

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