An Overview of Digital Low Drop-out Regulator Design

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***Abstract*— Digital Low Drop-out Regulator (D-LDO) has recently drawn significant attention due to its process scalability and application to low supply voltage operation. However, the response of a conventional D-LDO is determined by the sampling clock, and thus proportional to the power consumption. Hence recent trends for D-LDO design is to break this power-speed tie. In this paper, three D-LDO design strategies are overviewed and comprehensively discussed, including unequal transistor sizing, multi-loop control and asynchronous control. Then, the design guideline for a fast response D-LDO is drawn.**

Keywords- Low drop-out regulator; digital; fast response; power consumption; PI control; asynchronous control

I. INTRODUCTION

Modern energy-efficient digital integrated circuits (ICs), e.g. Centre Processor Unit (CPU), apply multiple strategies for power saving, including the fine-grained supply voltage management. As in Fig. 1, the whole chip may be divided into multiple function units (FUs), each can be optimized independently, such as by the dynamic voltage scaling (DVS) technique. To fulfill this goal, each FU should be powered by a regulator with a compact size, low quiescent current and fast response.

The analog low drop-out regulator (A-LDO) [1], which have been studied for decades, seems to meet these requirements. It should be noted that the reduced supply voltage (V_{DD}) in the modern digital ICs can supply the power transistor if it works in the saturation region. However, this V_{DD} may fail to support a high gain error amplifier that is pivotal for the regulation accuracy, as shown in Fig. 2(a). Meanwhile, the application of A-LDO undermines the process scaling merit of the digital circuits.

As the counterpart of the A-LDO, the digital LDO (D-LDO) [2-12] is made from digital building blocks as in Fig. 2(b). A digital sensor, which can be either comparator or analog-to-digital converter (ADC), is employed to compare the output voltage (V_{OUT}) and the reference voltage (V_{REF}). The EA with high V_{DD} in A-LDO is typically replaced by a digital controller (integrator), which ensures a reduced steady error and precise regulation as well. Then the controller turns on and off the power switch array according to the required loading current. Consequently, the all-digital implemented D-LDO works well under low supply voltage condition and enjoys the process scalability.

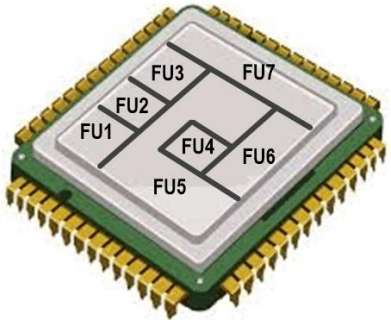

Fig. 1 A digital modern digital IC is typically divided into multiple FU for power optimization.

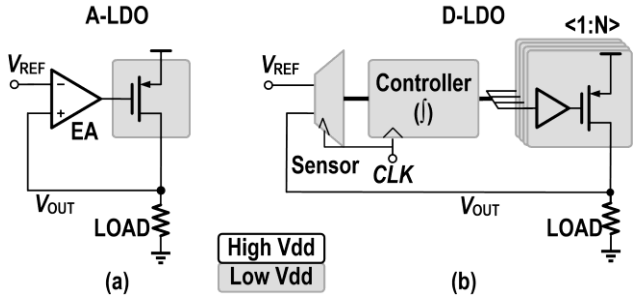

Fig. 2 The architectures of (a) A-LDO, and (b) D-LDO.

For the response speed of the conventional D-LDO, it is related to the frequency of the sampling clock. Nonetheless, the power consumption of the digital circuits will increase proportionally with the sampling frequency. Hence, the speed of the D-LDO is limited by the power consumption.

To break the power-speed trade-off, several fast response techniques with reduced power consumption have been proposed in previous literatures, which is reviewed here. This work is organized as follows. The strategy of unequal power transistor sizing is given in Section II. The proportional-integration (PI) control scheme is presented in Section III. The asynchronous control is discussed in Section IV. Finally, the design guideline and the conclusion are drawn in Section V.

II. UNEQUAL POWER TRANSISTOR SIZING

The slow response of the conventional D-LDO is mainly because its power transistors are equally sized, while the control word (the output current) can only be changed 1 unit bit/sampling cycle. This not only causes a large over/undershoot during load transient instant, but also a long

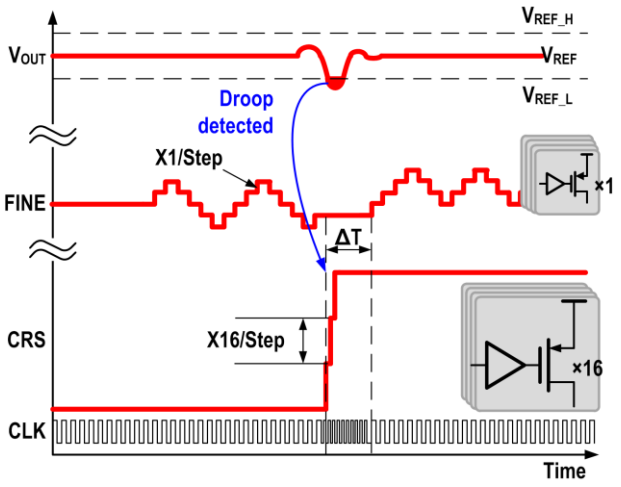

Fig. 3 The transient waveforms of the D-LDO with a 16× weighted linear search when V_{OUT} exceeds the preset boundary.

tracking time for V_{OUT} to stabilize to V_{REF}. Therefore, the unequal power transistor schemes [2, 3], [5, 6] have been proposed to address this issue.

A. *Weigthed Linear Search*

The weighted linear search schemes have been proposed in [2, 3], aiming at fast transient response and low quiescent current in static state. The fundamental working principle can be explained as in Fig. 3. The power transistor array is divided into multiple sections, e.g. coarse section and fine section in [2], where the unit transistor in coarse section is sized 16 times of that in fine section. And the control words for these two sections are FINE and CRS, respectively. CRS can be increased/decreased by carry in/out from FINE. This configuration helps to widen the D-LDO loading range with reduced control logics.

When in a static state, CRS is kept unchanged, while FINE varies as a limit cycle oscillation (LCO) [4], with 1 unit step/cycle. When a load transient occurs, the fine section is disabled and coarse section is activated, where the CRS will change 16 unit step/cycle (16× weighted linear searching). This is triggered by detecting V_{OUT} exceeding a preset boundary (between V_{REF_H} and V_{REF_L}). Meanwhile, the sampling frequency is also boosted, which will quickly drive V_{OUT} back within the boundary. These operations may be unstable and power hungry, and thus will be terminated within a ΔT duration (known as a burst-mode) and D-LDO will return to the 1× weighted learn searching.

However, this scheme may still need a very high sampling frequency for the droop detection and triggering the N× weighted learn searching. Additionally, this scheme is more suitable to the application where the load transient takes place only occasionally. For the application with load changing all the time, D-LDO will always be in the 16× weighted linear searching, causing large ripple and power consumption.

B. *Binary Search*

To further speed up the response and tracking period, [5] proposed a D-LDO with a binary sizing power transistor

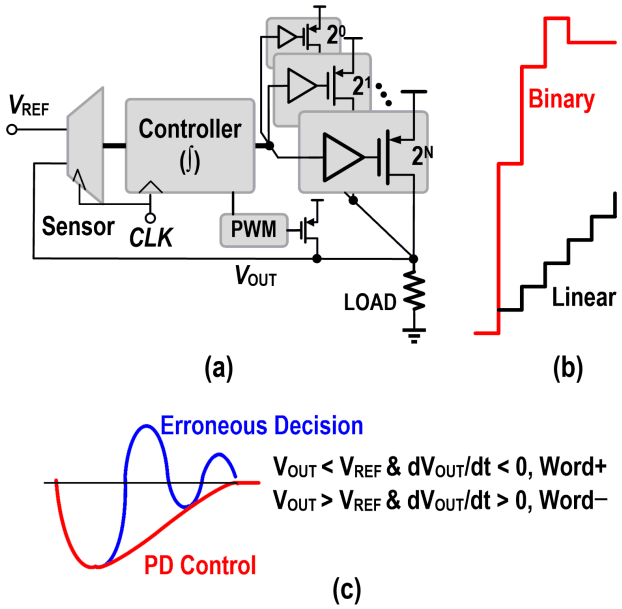

Fig. 4 (a) The schematic of D-LDO with binary-weighted power transistors, (b) the control word changing comparison between binary and linear search, and (c) the PD control law for a stable V_{OUT}.

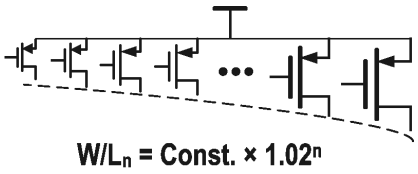

Fig. 5 The schematic of exponential-weighted power transistors.

array, as shown in Fig. 4(a). And a binary search and a successive approximation recursive (SAR) algorithm is performed, so that the D-LDO only needs N cycles to reach the final control word, which is much faster than the linear search as in Fig. 4 (b). Moreover, this scheme extends the output current range from N to 2^N with much less circuit complexity, using only N-bit power transistors. For a higher output accuracy, a least significant bit (LSB) power transistor, controlled by a pulse width modulation (PWM), is added in parallel to the binary sizing array.

Considering the quantization error, an erroneous successive decision may be made during switching, causing an unstable response as in Fig. 4(c). As a solution, a proportional-derivative (PD) control is executed, where the control word switching is not only triggered by comparing V_{OUT} and V_{REF}, but also the changing trend of V_{OUT}. With this PD control, the stability is improved, also as in Fig. 4(c).

For the drawback of the binary search scheme, there still needs a fast sensor to trigger the search. Hence transient response may be degraded.

C. *Exponential Search*

To mitigate the erroneous successive decision and instability made in binary search scheme, [6] proposed an exponential search method. As shown in Fig. 5, now the power transistors are sized in an exponential way, i.e. the

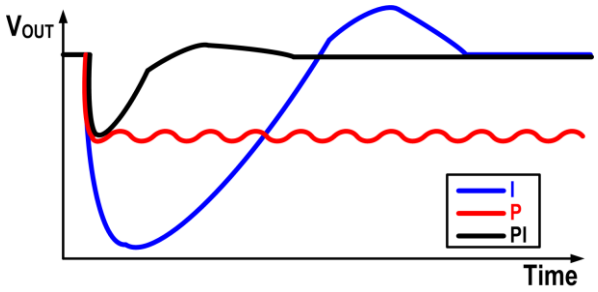

Fig. 6 The transient responses of the I, P, and PI controls.

W/L ratio of *n*th transistor is chosen to be proportional to 1.02^n. The ratio 1.02 is determined as all the transistors in the array can be certain integer times of the unit one, which is highly favorable for layout matching.

The exponential power transistor sizing might be a good trade-off between loop stability and circuit complexity. [6] achieves a 4000× maximum-to-minimum output current ratio with a 255-bit control word, together with a short tracking time.

III. Multi-loop Control

A. Digital PI Control

For a fast response A-LDO, multi-loop design [1] is frequently employed, where the fast loop deals with the transient response while the slow loop provides a precise regulation. Similarly, this strategy can be applied to D-LDO.

The proportional-integration (PI) control was firstly proposed in [7] to fulfill this idea. As shown in Fig. 6, the proportional (P) path manages to response quickly to the load transient, but fails to provide a required output voltage (V_{OUT}). And it is vice versa for the integration (I) path. When combing these two paths together, the D-LDO deals well with tracking time and regulation accuracy, with a moderate sampling frequency (200 MHz). However, a continuous-time 3-bit analog-to-digital converter (ADC) is utilized for a fast sensing, which may increase both the quiescent current and design difficulty. This results from that the response speed of the PI control, especially for the over/undershoot, is still limited by the sensor, which is discussed as follows.

Let us take the undershoot case as an example. The sensor output $Sensor_{OUT}$ will not change instantly when a load current I_{LOAD} step-up occurs (at t_1), but at the next rising edge of the sampling clock of the sensor (at t_2). V_{OUT} will then drop from t_1 on, since the current gap between I_{LOAD} and the output current I_{LDO} can be provided only from the output capacitor discharging. Then to prevent metastability and ensure a secured sampling, $Sensor_{OUT}$ will typically be sampled and the digital control word *n* begins to change at t_3. After that, the D-LDO outputs more current, and finally reaches the required I_{LOAD} at t_4, where the V_{OUT} droop stops.

Therefore, the overall undershoot ΔV_{MAX} can be divided into two parts: ΔV_{DLY} from t_1 to t_3 caused by the delay of the sensing, and ΔV_{REACT} from t_3 to t_4 coming from the response of the digital control. Although t_3-t_4 could be significantly minimized by the aforementioned techniques, e.g. unequal

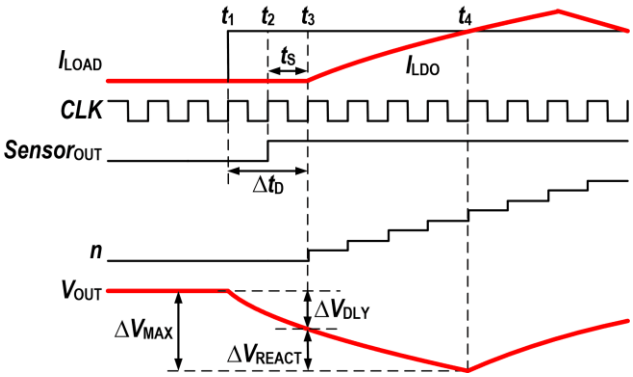

Fig. 7 The transient waveforms of clocked-sensor-based D-LDO when an undershoot takes place.

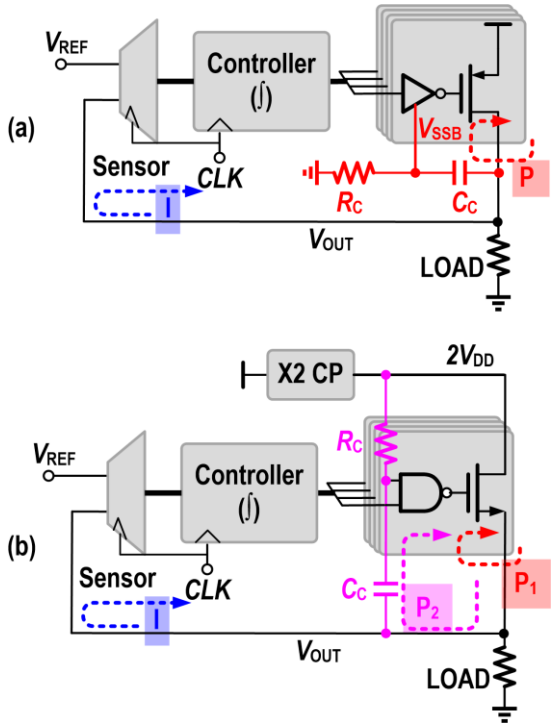

Fig. 8 The conceptual schematics of AA D-LDO in (a), and (b), where both P controls are implemented in an analog way.

transistor sizing and digital PI control, and t_1-t_3 can be shorten by using the both rising and falling edge sampling, t_1-t_2 can rarely be reduced. This is determined by the delay of the sensing. As a numerical calculation in [8], a maximum 2V ΔV_{DLY} can happen with a 10 mA/10ns load step, 1 nF output capacitor, 10 MHz sampling frequency.

B. Analog-P, Digital-I Control

To mitigate the delay of the sensing and thus the under/overshoot, analog-assisted (AA) D-LDOs were proposed, e.g. in [9] and [10]. These schemes can be regarded as an analog-P, digital-I control as shown in Fig. 8, where both the I controls are still implemented by digital integrator, while the P controls are fulfilled in an analog way with minimized static quiescent current. Both analog-P

TABLE I. COMPARISON AMONG RECENT D-LDO TECHNIQUES

	Under/overshoot	Tracking time	Power consumption
Unequal transistor sizing	Medium	Short	Medium
Digital PI control	Medium	Short	Medium
Analog-P digital-I control	Small	Medium	Medium
Asynchronous	Medium	Medium	Low

controls are designed to be easily scaled down with the digital circuits.

The P control in [9] is implemented by coupling V_{OUT} to the ground nodes of the driving inverter with a high pass network (R_C and C_C). Then the V_{OUT} spike will generate a larger/smaller output current in the under/overshoot scenarios. This P path is fast, but it is only effective when the power transistor driven is turned on, which limits the minimum loading current.

[10] designs two analog-P paths for an even faster response, where P_1 is intrinsically formed by the N-type power transistor, and P_2 is achieved by coupling V_{OUT} to the gate voltage. Nevertheless, a ×2 charge pump (CP) is required to provide a higher supply voltage for the NMOS.

IV. ASYNCHRONOUS CONTROL

Another strategy to achieve a fast response and low quiescent current is increasing the sampling frequency of the sensor circuit, while minimizing the controller sampling frequency, e.g. by an asynchronous control [11], [12]. Both the signal and clock of the next stage controller are generated by the previous stage, using delay cells. This prevents a high frequency global flipping of the digital circuits and thus a high static power consumption.

Nevertheless, the asynchronous logics are sensitive to process, voltage, and temperature (PVT) variations. This may degrade the circuit robustness especially when the supply voltage is low. Meanwhile, a sensor working at high frequency is still needed.

V. DESIGN GUIDELINE AND CONCLUSION

The D-LDO becomes a hotspot recently, due to its low power supply and its compatibility to process scaling with digital circuits. And previous literatures proposed techniques to break the trade-off between response speed and power consumption in the conventional D-LDO designs. This paper reviews and analytically discusses the recent D-LDO techniques that aims at simultaneous fast response and low quiescent current.

The aforementioned techniques are compared in Table I. For the unequal transistor sizing and digital PI control techniques, they achieve very short tracking time with a moderate sampling frequency. However, the under/overshoot may hardly be fully optimized. Similar circumstance can be found in asynchronous control, while it achieves the lowest power consumption. But when the amount of digital logic is further reduced as in the binary search, the quiescent current saved by the asynchronous design may be minor comparing to the synchronous counterpart. The analog-P digital-I control scheme will be optimal for under/overshoot reduction, as long as the analog-assisted circuits consumes little static power.

Moreover, it should be noted that these techniques are compatible to each other. Consequently, it might be optimal for a D-LDO uses unequal transistor sizing, performs the searching algorithm in an asynchronously, and implements an analog P-control.

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REFERENCES

[1] Y. Lu *et al*., "A Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power Supply Rejection," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 707–716, Mar. 2015.

[2] S. B. Nasir *et al*., "All-Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Digital Load Circuits," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8293–8302, Dec. 2016.

[3] M. Huang *et al.*, "A Fully Integrated Digital LDO with Coarse-Fine-Tuning and Burst-Mode Operation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 7, pp. 683–687, Jul. 2016.

[4] M. Huang *et al.*, "Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 9, pp. 903–907, Sep. 2016.

[5] L. G. Salem, J. Warchall, and P. P. Mercier, "A Successive Approximation Recursive Digital Low-Dropout Voltage Regulator with PD Compensation and Sub-LSB Duty Control," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 35–49, Jan. 2018.

[6] Y. Zhang *et al.*, "A Capacitor-less Ripple-less Hybrid LDO with Exponential Ratio Array and 4000x Load Current Range," *IEEE Transactions on Circuits and Systems II: Express Briefs*, accept for publication.

[7] D. Kim and M. Seok, "Fully Integrated Low-drop-out Regulator Based on Event-driven PI Control," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 148–149.

[8] M. Huang *et al*., "An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 20–34, Jan. 2018.

[9] M. Huang *et al*., "An Output-capacitor-free Analog-assisted Digital Low-dropout Regulator with Tri-loop Control," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 342–343.

[10] X. Ma *et al*., "A 0.4V 430nA Quiescent Current NMOS Digital LDO with NAND-based Analog-assisted Loop in 28nm CMOS," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 306–308.

[11] Y.-H. Lee *et al.*, "A Low Quiescent Current Asynchronous Digital-LDO with PLL-Modulated Fast-DVS Power Management in 40 nm SoC for MIPS Performance Improvement," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 1018–1030, Apr. 2013.

[12] F. Yang and P. K. T. Mok, "A Nanosecond-Transient Fine-Grained Digital LDO with Multi-Step Switching Scheme and Asynchronous Adaptive Pipeline Control," *IEEE Journal of Solid-State Circuits*, vol. PP, no. 99, pp. 1–12, 2017.