# A Power-Efficient 1.056 GS/s Resolution-Switchable 5-bit/6-bit Flash ADC for UWB Applications

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***Abstract*— A 1.056 GS/s, 5-bit/6-bit switchable flash analog-to-digital converter (ADC) is designed in 0.18-μm CMOS, which is suitable to be used in an OFDM-UWB transceiver. A resolution switchable structure is proposed to optimize power consumption according to the dynamic requirement of the application. Two-stage interpolation and averaging techniques are employed to average the offset of the preamplifiers. Monte Carlo simulation results show that the proposed ADC achieves 4.2b/5.0b ENOB in 5-bit/6-bit working modes with a 413-MHz input signal. The mean value of DNL and INL is 0.32 and 0.56 LSB for 5-bit mode, while 0.47 and 0.62 LSB for 6-bit mode. The analog part consumes 36 mW and 98 mW from a 1.8-V supply in 5-bit and 6-bit operation mode, respectively.**

## I. INTRODUCTION

There is growing interest in commercial Ultra-WideBand (UWB) communication systems since FCC opened up 7,500 MHz of spectrum (from 3.1 GHz to 10.6 GHz) for use by UWB devices. At present, both direct-sequence impulse communications and multiband OFDM UWB systems [1] are under consideration for the standard. This paper deals with the ADC design for the multiband OFDM system. The ADC resolution is determined by the tolerable quantization noise, the AGC resolution, and the level of WLAN interferences that are only partially attenuated by the baseband channel-select filter. In [2], it has been proved that the use of a 5-bit front-end ADC with 4-bit Effective-Number-Of-Bit (ENOB) for 110/200 Mbps, and a 6-bit ADC with 5-bit ENOB for 480 Mbps is sufficient for MB-OFDM UWB system.

The ADC is always a power-hungry component for the whole analog front-end of the UWB transceiver. Since the UWB systems are always used in portable devices, low-power designs are therefore of critical importance to extend the battery life. Where maximum sampling rate and low to moderate resolution is required, flash ADCs are still a good candidate of choice [3, 4]. However, the major advantages of flash architecture also present its main problem: the number of comparators increases exponentially with the resolution specifications, leading typically to a large die area and high power consumption. When a converter with 5-bit is enough for data rates of 110/200 Mbps, the use of an extra bit resolution will increase the power consumption and will be uneconomical. To overcome this problem, we present a resolution switchable flash ADC which can adapt its resolution according to the system's dynamic operation mode and to optimize the power utilization. With 1.056 GS/s sampling frequency and an ENOB of 4.2 bits and 5.0 bits, respectively, at an input signal frequency of 413 MHz, the ADC fulfils the different data rates requirements of the MB-OFDM system. Due to its large ERBW different receiver topologies can be supported. However, the proposed ADC will not be limited to only these applications.

This paper is organized as follows: section II illustrates the flash ADC architecture and the key ideas to improve the linearity and reduce the power consumption. Section III describes and explains the circuit implementation of the main building blocks. Finally, in section IV simulation results are provided to verify the effectiveness of the design and to demonstrate the performance of the ADC.

## II. ADC ARCHITECTURE

The block diagram of a 5-bit/6-bit switchable flash ADC with resistive averaging and interpolating is presented in Fig. 1. The resistive ladder sub-divides the converter reference voltage into a set of $2^4$ reference voltages, which are compared in parallel with the analog input signal by the subsequent differential preamplifiers. Resistive averaging and interpolating have been adopted to reduce the mismatch effect and the number of preamplifiers. Two switching arrays are used before and after the second preamplifier stage to realize the switching between 5-bit and 6-bit resolution working modes. The second gain stage will be shut down and skipped at 5-bit resolution mode to save power. The comparator array can also be split into two groups, one of which will be turned off when the converter working with 5-bit resolution. To relieve the comparator offset requirements, pre-amplification, interpolation and averaging techniques have been applied. A logic decoder converts the thermometer code generated by all the comparators into a binary code that approximates the input signal every clock cycle.

Generally, there are three main techniques explored in this design to realize the ADC.

- Resolution scalable according to the transceiver's working condition, including the working data rate, AGC resolution and the performance of the baseband channel-select filter.
- Use of interpolation to reduce preamplifier number and employ averaging to alleviate the mismatch impact on

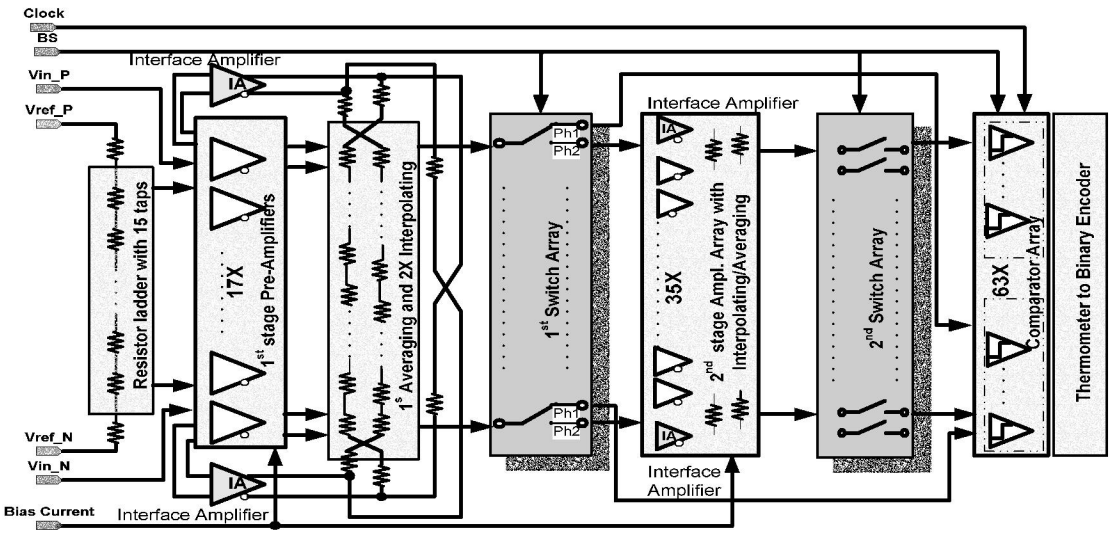


Fig. 1: Resolution-switchable flash ADC with resistive averaging and interpolation

preamplifier offset, thus allowing additional downscaling to save power and silicon area.

- Triple-cross connection adopted in the first and second averaging resistor string (shown in Fig.1) with only two interface amplifiers used instead of using many over range references and dummy amplifiers to solve the resistive averaging boundary problem and improve the averaging efficiency [5].

## III. BUILDING BLOCKS AND DESIGN ISSUES

The resolution switchable flash ADC consists of several important building blocks that are addressed next.

### *A. Combined Averaging and Interpolation*

Interpolation between reference levels reduces the number of preamplifiers thus resulting in low power consumption. It also has a positive effect on the differential non-linearity (DNL) of the ADC [6]. Beyond these advantages, two-stage interpolation is used in this design to exploit its flexibility of switching between 5-bit and 6-bit resolution working mode. Fig. 2 presents the resistive interpolation and the preamplifier circuit. Interpolation by a factor of 2 can be achieved by splitting up the averaging resistors in two equal parts. A combination of averaging and interpolation is employed in our design. To avoid loading effect an output buffer is added to the input amplifier, as shown in Fig. 2.

The offset averaging technique proposed in [7] is an effective method to alleviate the mismatch impact in preamplifier or comparator arrays and, simultaneously, signal-to-noise ratio is improved without using additional power. On the other hand, averaging is achieved by inserting ladder resistors between the outputs of adjacent amplifiers. Although the averaging technique allows the use of small size transistors throughout the design, it also causes problems at the boundaries of the averaging resistor network. At the edge, the zero-crossings shift inward due to the lack of amplifiers outside the boundary, which causes systematic nonlinearity errors. Besides, the number of random components contributing to the averaging is diminished at the boundary and then counteracts the DNL/INL improvement due to averaging.

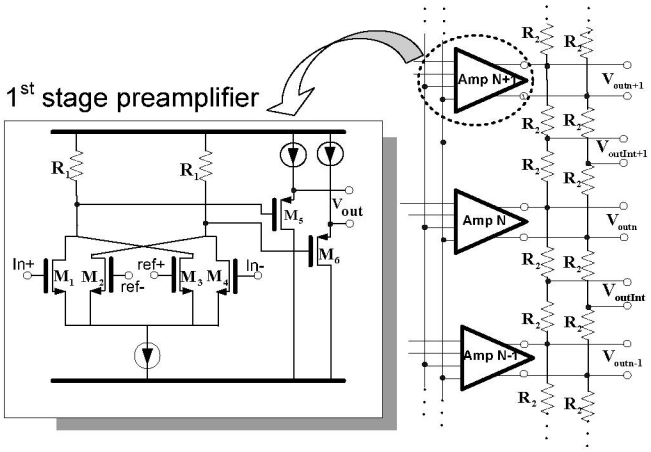


Fig. 2: Resistive interpolation and preamplifier

The traditional way to solve the termination problem is either to use dummy amplifiers [4] or to resort to extra boundary termination circuits [8]. The dummy method needs many dummy preamplifiers to become more effective. Since only a part of the amplifier array and reference range are usable, this method is not power efficient. Although the extra boundary termination circuit consumes less power and area, it only restores the systematic errors when the averaging window is narrow and the boundary issue is less severe. In this paper, a triple-cross connection method [5] is chosen to solve the boundary problem with only two interface amplifiers used, as what is shown in Fig. 1. The two crossings at the boundaries minimize the zero-crossing shifts and the third crossing is for proper termination of the resistor network.

### *B. Resolution Switching Circuits between 5-bit and 6-bit*

When a 5-bit ADC is used, the second preamplifier stage and half of the comparators will be shut down to save power. An enable signal BS (Bit Select) is given to the ADC as a resolution-select signal, Where BS=0 means that 5-bit is used and BS=1 means 6-bit ADC is needed. The biasing circuit for the second amplifiers array is shown in Fig. 3. When BS=0, the gate of the tail current source for the second stage preamplifier is disconnected from the biasing

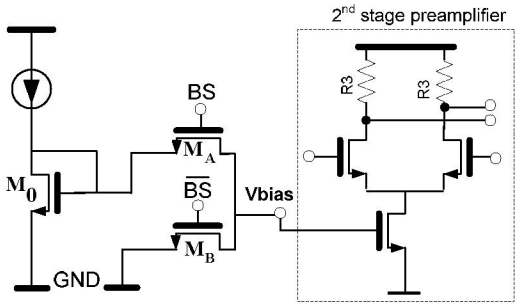


Fig. 3: Switchable biasing circuit for 2nd gain stage

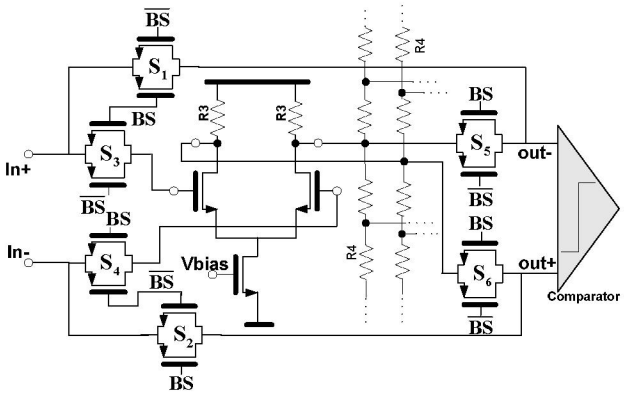


Fig. 4: Switching circuit between two resolution modes
BS =0, 5-bit; BS =1, 6-bit

current $M_0$ and pulled-down to GND by $M_B$, so that the second gain stage will be cut-off and then not consuming additional power.

The switching circuit before and after the second gain stage is illustrated in Fig. 4. Here single differential amplifier with resistive load is used as the second gain stage for its simplicity and wide bandwidth. When the ADC works with 5-bit resolution, BS=0, $S_1$, $S_2$ are on while switches $S_3$, $S_4$, $S_5$ and $S_6$ are off, thus the second stage amplifier and the following interpolating resistors string are skipped. From previous analysis we know that the amplifier is powered-down at this moment with its biasing voltage $V_{bias}$=0. The simulation results show that, switching off the second gain stage will save the system over half of the static power consumption when the converter works in 5-bit mode. The reason is that the 2nd stage contains totally 35 preamplifiers while the 1st stage has only 17 preamplifiers. Since only half of the comparators are switched off in 5-bit mode, adding switching circuit *S5* & *S6* will introduce on resistance in only half of the signal paths in 6-bit mode. This imbalance of signal paths time-constant will introduce frequency dependent nonlinearity errors. To alleviate this problem, dummy switches are added before the comparators which do not require switching to balance the on resistance.

### C. *High Speed Comparator*

When the ADC is working in 5-bit resolution mode, only 33 comparators including two overflow indicators are used. Another half of the comparators are turned off for minimum power dissipation. The circuit for the high speed low power comparator [9] is shown in Fig. 5. This comparator has two operating states, evaluation phase and reset phase. During evaluation phase, $V_{latch}$ is logically high and the current source $M_0$ turns on, the input devices $M_{1,2}$ sense the differential input, the imbalance potential on $V_{out}^+$

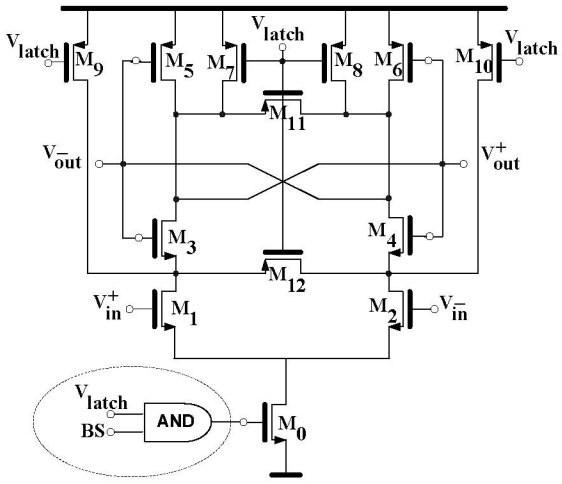


Fig. 5: High speed comparator and its switching circuit

and $V_{out}^-$ is then regenerated to full swing. In reset phase, $M_0$ turns off and all reset transistors $M_7$~$M_{12}$ turn on. The reset devices $M_7$~$M_{12}$ eliminate all imbalance charge, so the previous data is cleared. The input referred offset of the comparator due to device mismatch can be made relatively small by the two preceding gain stages and the averaging technique; therefore we can use small size transistors to ensure high-speed operation.

In Fig. 5, the power-down control circuit inside the dashed circle is added only to 32 out of the total 65 comparators. When the bit-select signal BS=0, current source $M_0$ turns off and the current path of the comparator has been cut off. To avoid delay mismatch, dummy control circuits have been added in the remaining 33 comparators which are operating in both 5-bit and 6-bit modes.

## IV. Simulation Results

The proposed resolution-switchable flash ADC has been implemented using a 0.18-μm CMOS process and simulated at circuit-level. The effectiveness of the proposed ADC with averaging and interpolating techniques has been verified comprehensively by Spectre simulator with the components' mismatch effect considered. Fig. 6 shows the simulated DNL and INL from one case of Monte-Carlo simulations, and Fig. 7 illustrates the histogram of DNL and INL of 100-run, with mean DNL /INL of 0.47/0.62 LSB, respectively, for 6-bit mode.

In addition to static parameters, the dynamic performance of the flash ADC is obtained through a Monte-Carlo simulation using an

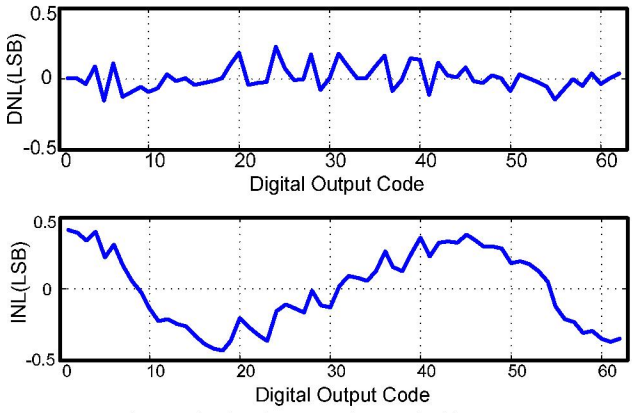


Fig. 6: Simulated DNL and INL of 6-bit ADC

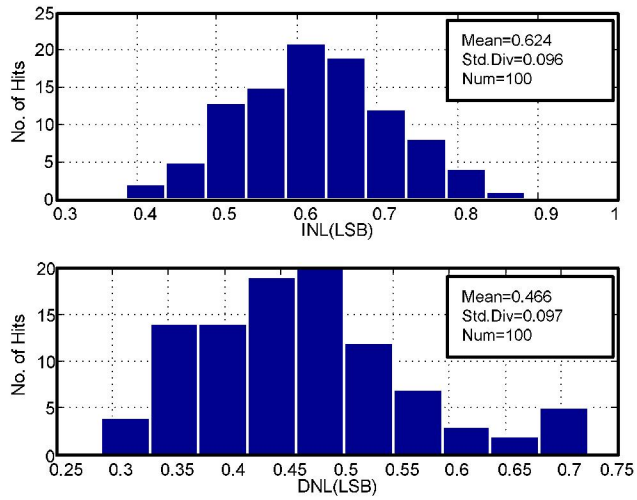


Fig. 7: Histogram of INL and DNL of 6-bit ADC

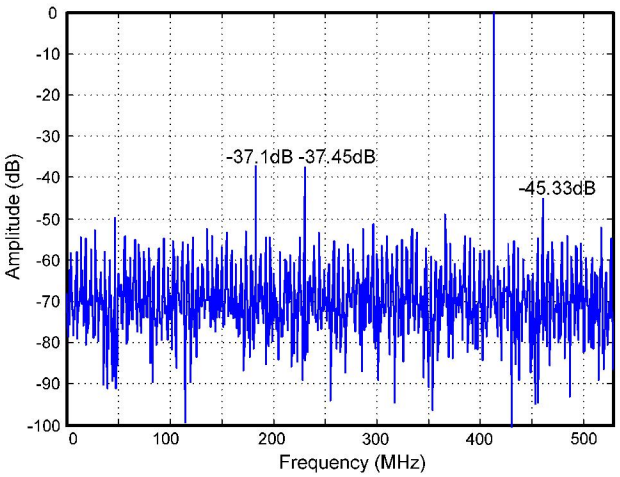


Fig. 8: FFT of a 413 MHz input signal sampled at 1.056 GS/s

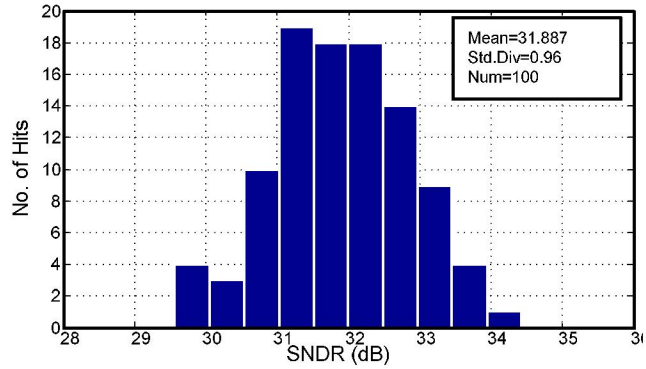


Fig. 9: Histogram of SNDR of 6-bit ADC @$f_{in}$=413 MHz

input signal of 413 MHz and sampling frequency of 1.056 GS/s, with the spectrum for one case presented in Fig. 8. Fig. 9 also shows the corresponding histogram where the ADC achieves a mean SNDR of 31.887 dB (corresponding to an ENOB of 5.0 bits).

The performance of the whole ADC is summarized in Table I. The analog part power consumption of the 5-bit resolution mode is 36 mW, while for 6-bit resolution, it is 98 mW, so it is evident that the proposed ADC is powered economically by dynamically changing the resolution according to the transceiver's working condition.

TABLE I : PEFORMANCE SUMMARY OF THE PROPOSED ADC

| Parameter | | Resolution | |
|---|---|---|---|
| | | *5-bit* | *6-bit* |
| Supply voltage | | 1.8 V | |
| Input range | | $1V_{PP}$(±500mV) | |
| Sampling Frequency | | 1.056 GS/s | |
| DNL/INL | | 0.32/ 0.56 LSB | 0.47/ 0.62 LSB |
| ENOB | @ $f_{in}$=43MHz | 4.8 | 5.5 |
| | @ $f_{in}$=413MHz | 4.2 | 5.0 |
| Power Consumption (analog part) | | 36 mW | 98 mW |

## V. CONCLUSIONS

In this paper a 1.056 GS/s resolution-switchable flash ADC with averaging and interpolating has been presented. The ADC is designed to be able to switch between 5-bit and 6-bit resolution according to the receiver's working condition. Instead of using a 6-bit resolution ADC for the system, the proposed ADC can achieve better performance on power optimization. The analog part consumes 36 mW for 5-bit and 98 mW for 6-bit resolution modes and the mean DNL/INL value is 0.32/0.56 LSB for 5-bit mode and 0.47/0.62 LSB for 6-bit mode, respectively. The simulation results show that the proposed ADC fulfills the requirements of the MB-OFDM UWB receiver.

## ACKNOWLEDGMENT

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