16.2 A 4× Interleaved 10GS/s 8b Time-Domain ADC with 16× Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input

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The ever-increasing data traffic in wireline communication systems has led to the demand for high-speed ADCs with a large input BW. Time-interleaved SAR ADCs with a large interleaving factor suffer from a large input capacitance [1] and often have a limited BW, or otherwise they necessitate a power-hungry broadband input buffer [2]. Flash ADCs [3] not only face the same challenge from the large input parasitics but also limited resolutions resulting from offset. Recently, time-domain ADCs [4-5] have shown promising speeds resulting from a small input capacitance due to their inherent voltage-to-time converter (VTC) as a sub-channel wideband buffer, but also show limited resolution (6b) due to the mismatches between the time steps. When targeting a higher resolution [6], calibration is necessary to unify the time quantization steps and often requires a known input condition with a large lookup table, thus introducing complexity. In this work, a 10GS/s ADC is achieved by just aggregating four 8b two-stage time-domain ADCs running at 2.5GS/s. The gain between the stages is inherently defined by a 16× time interpolator in the second stage, which not only saves power but also allows the time quantization steps to be free from calibration. The presented time-domain ADC achieves >37.5dB SNDR at an 18GHz input due to its small input capacitance and buffer-like VTC, and also obtains a metastability error rate $<10^{-8}$ through a timing-extended residue transfer scheme. Moreover, the time quantization in the two-stage ADC also shows PVT robustness benefits from the interpolation-based gain.

The time-domain ADC scales with VTC and TDC for conversion. Its conversion speed f_s for N-bit resolution is defined by the time step T_{LSB}, that is $f_s<1/(2^{N+1}\times T_{LSB})$ when assuming half of the period is for sampling, thus reducing T_{LSB} increases the ADC conversion speed. Both the Vernier [7] and pulse shrinking [5] TDCs achieve a sub-gate time resolution; however, a calibration for their highly nonlinear quantization steps is needed. Such time step variation over PVT also imposes a gain calibration as if they are applied in two-stage architectures. Ring-oscillator-based TDCs [4] demonstrate a fine time step as well, but with high power consumption from the oscillator, while still requiring time step calibration for T_{LSB}<2ps [6]. In this design, the 16× interpolation-based two-stage TDC resolves the above power and complex calibration shortcomings, achieving a 1.375ps T_{LSB}.

Figure 16.2.1 shows the block diagram of the 4× interleaved ADC. The sub ADC is an 8b time-domain ADC, which consists of a S/H, a VTC, and a two-stage TDC. The S/H adopts bootstrapped switches with cross-coupled compensation for high-linearity sampling on an input capacitance of only 45fF (single-ended). The dynamic VTC converts the sampled voltage into a time difference (S_{P1}<0>, S_{N1}<0>) through a pair of current sources and crossing detectors. The pseudo-differential and discharging features guarantee the high linearity of the VTC. Monte Carlo simulation with PVT variation shows that the VTC together with S/H has <–52dB THD. It is worth noting that the VTC also acts as an isolator between the S/H and the quantizer, thus ensuring that the time-domain quantization has a negligible impact on the S/H. Such a superior feature over the voltage-domain counterparts enables a large input BW (>18GHz) in this design. The 8b TDC comprises a 4b pseudo-differential flash TDC (with 1b sign) as the coarse stage and a 5b single-ended interpolation TDC (with 1b redundancy) as the fine stage. A folding-based time residue transfer connects them and generates the single-ended time residue (R_{F1}, R_{S1}). The 16× interpolator in the fine stage achieves a PVT-robust gain between the two stages. All the time comparators in both stages share the same topology but with different sizes to eliminate calibration. The 10GS/s ADC is clocked by a 5GHz differential source, and the 4 low-jitter sampling clocks with 25% duty cycle are generated through a low-jitter selection on the differential input clocks (P1_1, P1_2) directly.

Figure 16.2.2 presents the fine-stage 5b interpolation TDC. The 22ps delay cells in the flash and interpolation TDCs have the same topology and thereby PVT response. The 22ps time delay is allocated into 16 time intervals with the 16× time interpolator to achieve an inherent and accurate inter-stage gain of 16 (LSB_{Coarse}/LSB_{Fine}=16). Dummy delay cells and interpolators are added both before and after the quantization cells to shield the terminal effect. The 16× time interpolator is a 4-stage cascade of 2× phase interpolators with balanced input and output loading for better matching. Behavioral simulations on the SNDR of an 8b TDC (4+5-1) with either a 5b Vernier TDC or a 16× interpolation TDC as the fine stage versus unit delay variation (σ) are shown in Fig. 16.2.2. From the results, the presented interpolation TDC relaxes the requirement of the fine-stage delay units significantly compared with the Vernier TDC. With a 50% fine-stage variation (to 1.375ps) and a 1% coarse-stage variation (to 22ps), the presented ADC achieves ~43dB SNDR. Consequently, the time interpolation saves this design from complex time step and inter-stage gain calibrations. Extra delay is inserted to the R_S signal path for dummy matching and time range shifting whereas its accuracy is quite relaxed due to the 1b redundancy.

High-speed voltage-domain ADCs often suffer from metastability errors originated by the voltage comparators. The metastability of the time comparator can be suppressed through a different rising time on the comparing edges, but not enough for targeting an error rate $<10^{-8}$. A time residue transfer with metastability-reduced timing is shown in Fig. 16.2.3, where the time residue of the flash TDC (t_{res}) is generated with a time folding and subtraction operation. The inherent linear time folding is achieved by an edge selector, while the subtraction is from a dynamic differential AND. The time-folding selection is shifted by one flash TDC time step and extra delay units are embedded in the time subtraction, which gives rise to the >100ps available decision range for the flash TDC comparators, thereby lowering the metastability error rate. To assist this, the global reset of the folding and subtraction is re-timed from ϕ_S to ϕ_T. Afterwards, the differential time residue is converted to single-ended with another timing-extended re-trigger (ϕ_{T_D}) to reduce the metastability error in the fine stage. The offset that occurred in the above operation is well within the designed redundancy range, and is eventually removed together with the multi-channel offsets in the digital domain.

The ADC is fabricated in a 65nm CMOS technology with an active area of 0.095mm^2 in Fig. 16.2.7. Calibration on the VTC offsets is done one-time in the foreground for better dynamic range. The multi-channel gain, offset, and time skew are removed in the background together with the residue transfer offset. No calibration related to time step and inter-stage gain is applied. In Fig. 16.2.4, the 10GS/s ADC shows 40.1dB SNDR and 52.8dB SFDR with a Nyquist input, and achieves 37.6dB SNDR and 46.7dB SFDR with a ~18GHz input. The spur at $2f_{in}$-$f_s/2$ is caused by a relatively higher HD_2 in one of the channels. In Fig. 16.2.5, two chips both show <0.5dB and <0.6dB SNDR variation across –55°C to 125°C and ±5% supply variations, respectively when set to a common output swing. Both chips achieve a >18GHz BW, resulting from the presented architecture with a small input capacitance. The measured metastability error rate is $<10^{-8}$. The 1V-supplied ADC consumes 50.8mW at 10GS/s, with a maximum conversion rate of 12GS/s. The achieved Walden FoM is 61.5fJ/conv.-step, and the Schreier FoM is 150.0dB. Compared with state-of-the-art ADCs in Fig. 16.2.6, this work shows a superior SNDR/SFDR at both Nyquist and over Nyquist input, while also avoiding time step calibration in the time-domain conversion.

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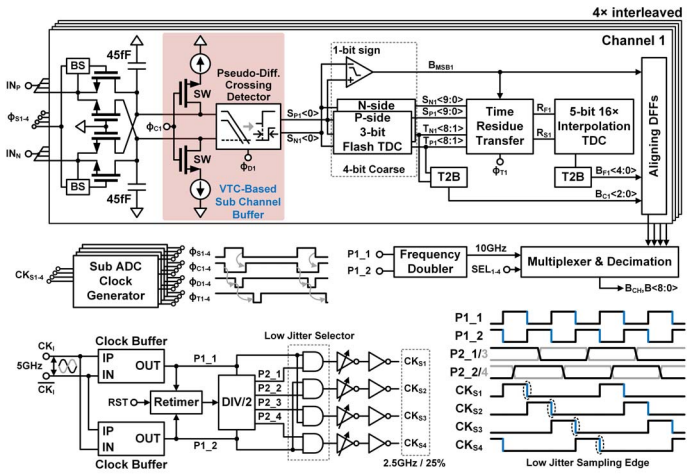

Figure 16.2.1: Block diagram of the 4× interleaved time-domain 8b two-stage ADC and low-jitter clock timing.

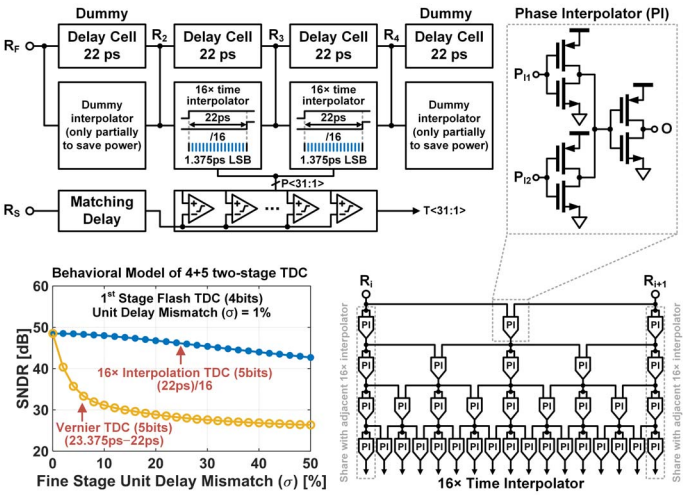

Figure 16.2.2: 5b fine-stage TDC based on 16× time interpolation and behavioral comparison between Vernier and interpolation TDCs.

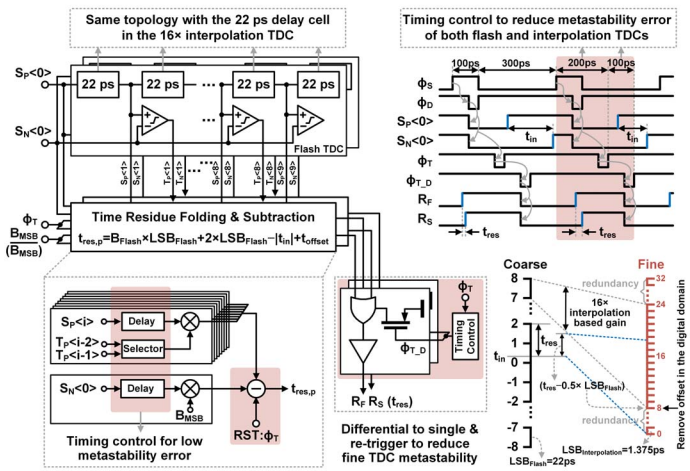

Figure 16.2.3: Time residue transfer implementation details with timing for low metastability error (an example with an input time difference (t_{in})=7.33ps is shown).

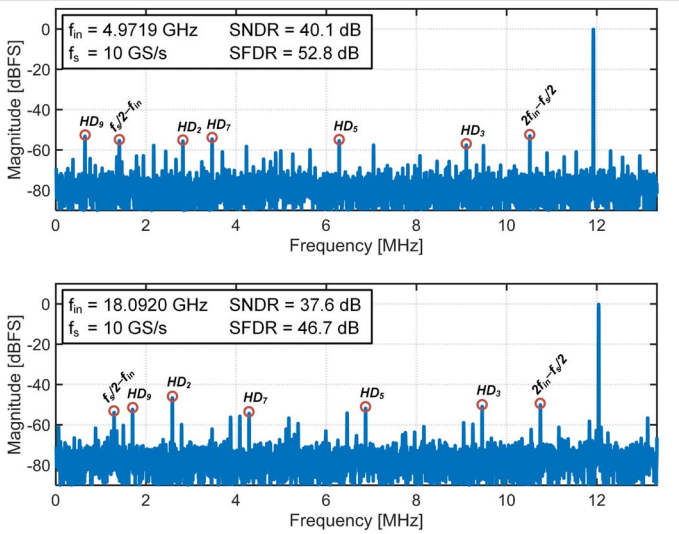

Figure 16.2.4: Measured 8192-point output spectra at 10GS/s with Nyquist (5GHz) and over Nyquist (18GHz) input frequencies (decimated by 375).

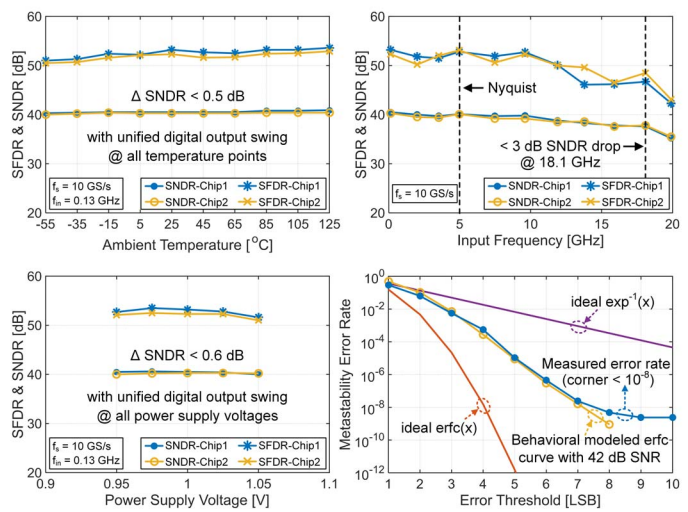

Figure 16.2.5: Measured SFDR and SNDR versus ambient temperature, power supply variation, and input frequency at 10GS/s with two chips; and the ADC metastability error rate.

	This Work	[4] JSSC 16	[5] CICC 19	[2] ISSCC 14	L. Kull VLSI 13	Y. Frans VLSI 16
Architecture	TI Time Domain ADC			TI SAR ADC		
Technology	**65nm CMOS**	65nm CMOS	65nm CMOS	28nm SOI	32nm SOI	16nm FinFET
Resolution [bits]	**8**	6	6	6	8	8
Sampling Speed [GS/s]	**10**	10	10	10	8.8	28
Number of Channels	**4×**	4×	2×	8×	8×	32×
Supply Voltage [V]	**1.0**	1.3	1.0	1.0	1.0	0.9
Power [mW]	**50.8**	98.0	29.7	32.0	35.0	280.0
SNDR @ Nyq. [dB]	40.1	27.2	32.5	33.8	37.0	31.5
SFDR @ Nyq. [dB]	52.8	42.1	40.7	41.1	48.8	39.1
SNDR @ >Nyq. [dB]	37.6 @18.1GHz	24.6* @7.0GHz	26.0* @8.0GHz	29.7 @19.8GHz	N/A	N/A
SFDR @ >Nyq. [dB]	46.7 @18.1GHz	32.3* @7.0GHz	28.5* @8.0GHz	46.1 @19.8GHz	N/A	N/A
FOM_{Walden} [fJ/conv.-step]	61.5	523.7	86.2	80.4	68.9	325.7
$FOM_{Schreier}$ [dB]	150.0	134.3	144.8	145.7	148.0	138.5

* Estimated from the input frequency sweep results.

Figure 16.2.6: Performance summary and state-of-the-art comparison.

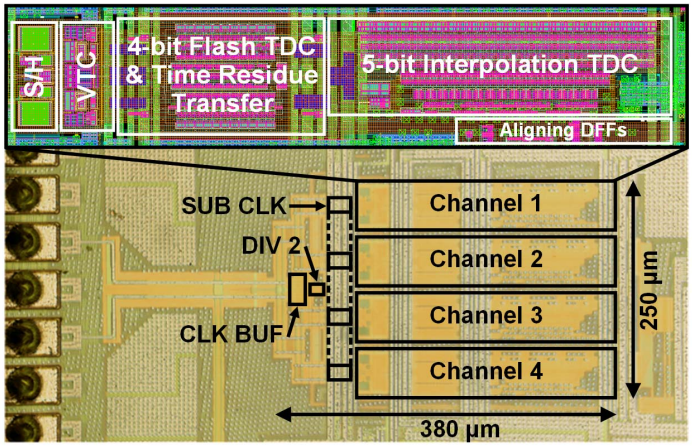

Figure 16.2.7: Chip micrograph with one-channel ADC layout view.

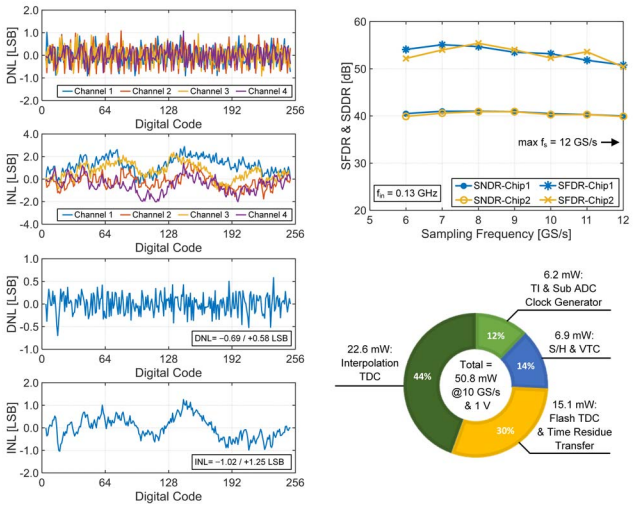

Figure 16.2.S1: Measured DNL and INL of the individual and aggregate channel, SFDR and SNDR versus sampling frequency, and power consumption breakdown.

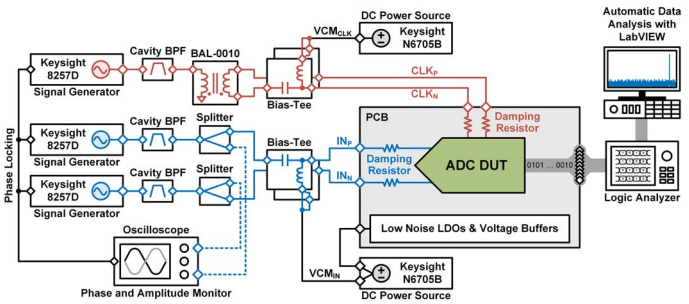

Figure 16.2.S2: ADC measurement setup.

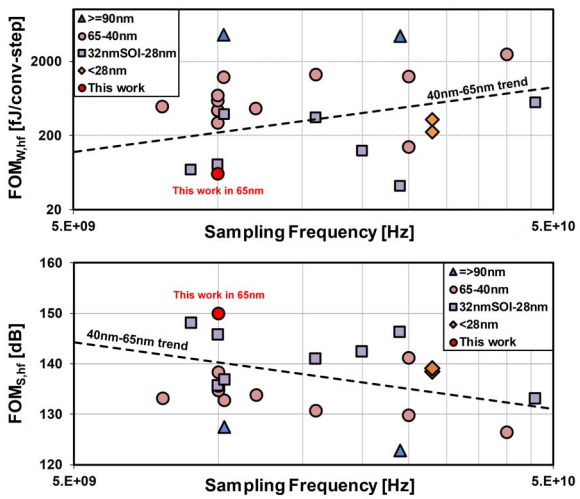

Figure 16.2.S3: Walden and Schreier FoM comparisons with ISSCC/VLSI 1997-2019. (filter: sampling frequency>5GS/s, and bit number<9). (B. Murmann, "ADC Performance Survey 1997-2019").

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