A Process-insensitive Current-Controlled Delay Generator with Threshold Voltage Compensation

He-Gong Wei, U-Fat Chio, Sai-Weng Sin, Seng-Pan U and R.P. Martins[1]
Analog and Mixed Signal VLSI Laboratory (http://www.fst.umac.mo/en/lab/ans_vlsi)
Faculty of Science and Technology, University of Macau, Macao, China
Tel:+853-83978796, Fax: +853-28840542, Email:weihegong@ieee.org
1 – On leave from Instituto Superior Técnico/TU of Lisbon, Portugal

***Abstract*—A process-insensitive current-controlled delay generator is presented with a large tunable range of the time delay. By adopting process variation compensation techniques in the generation of time delay, the delay generator is able to provide process-insensitive clock pulses. The circuit has been fabricated in 90nm CMOS technology, consumes 310µW from a 1.1V supply. Using, in a typical case, 20µA of reference current, it can generate a delay of 2.36 ns. The delay variation observed in 14 measured chips has shown a standard deviation of 1.24%.**

I. Introduction

Sampled-data systems incorporating data conversion and switched-capacitor filters are indispensable in state-of-art IC design, being crucial in telecommunication, consumer electronics and medical imaging applications [1], [2]. In such discrete-time systems, the clock generator is one of the extreme importances and the accuracy of the clock signal is determinant in the overall design, since the overall resolution is often related with it. However, the variation of the clock pulse width exists inevitably and is normally associated with process or temperature variations in the delay paths. Usually, large design margins should be adopted in the transistor implementation to overcome such process variations but this would imply extra power consumption with the subsequent degradation of system performance.

Therefore, process-insensitive delay generators are highly demanded and effective solutions have been proposed either off-chip [3] or on-chip [4]. This paper presents an advanced current-controlled delay generator using process-insensitive components like current mirror and MOS-capacitors [5], avoiding the complexity of a delay-locked loop (DLL). By applying the threshold voltage compensation method, the proposed delay generator reduces the deviation induced by the internal inverter buffer, thus becoming more robust to process variations than existing designs [5], [6].

II. Delay Generator Implementation

Traditionally, the delay generator is implemented by the inverter-chain, also designated as g_m/C circuit [7] that accumulates the time delay of the inverters and provides the time delay for the system. Although its architecture is quite simple, it suffers from a significant process variation sensitivity that can imply a significant ±15% variation in time delay.

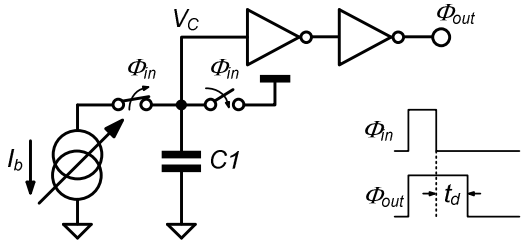

Figure 1: Traditional current-controlled delay generator.

An alternative solution, the current-controlled delay generator [5] [6] was previously proposed to achieve higher process-insensitivity with the utilization of less process-sensitive circuit elements. Figure 1 shows the simplified schematic of the delay cell which contains basically a current source, a capacitor, switches, output buffers and I/O clock phases. The top-plate of the capacitor is firstly charged to the supply and Φ_{out} will be high. Then, it is linearly discharged by a constant current I_b which is controlled by the current source, and the generated delay t_d can be calculated as $C_1\Delta V_C/I_b$ where ΔV_C equals the supply voltage. The current is provided by the current source and its accuracy is mainly related with the precision of the current mirror and the reference current. This is usually accurate and the current mirror is relatively easy to design with good matching. Therefore, the current will not be significantly affected by process variations. Besides, a MOS-capacitor usually ensures also smaller sensitivity to process variations, when compared with other type of implementations of the capacitors [5]. Normally, the MOS-capacitance varies around ±5% with process. Since both the current and capacitor are insensitive to process-variation, the generated t_d will be also process-insensitive.

However, the result of the circuit from Figure 1 still shows that it varies with process, mainly because of threshold voltage variation of the inverter connected to the capacitor. When V_C decreases, the inverter will be triggered to generate t_d once the V_C crosses its threshold voltage that depends on the robustness of the N/PMOS transistors and is highly process-sensitive. A possible solution of the problem will be introduced next.

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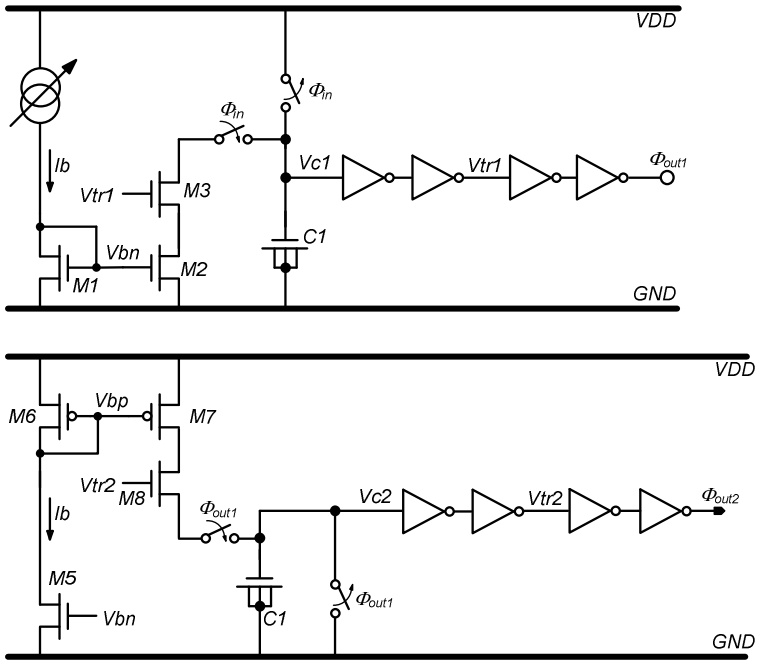


Figure 2: The circuit implementation of the proposed advanced current-controlled delay generator

III. Current-Controlled Delay Generator with Threshold Voltage Compensation

The proposed process-insensitive current-controlled delay generator is exhibited in Figure 2 and it includes an upper and lower part. The upper part is similar to [5] and was previously described. It receives the input clock Φ_{in} and then provides the output clock Φ_{out1} to the lower part of the delay generator with a delay of t_{d1} at the falling edge of the clock. Comparing to the upper part, the lower part also has two operation phases but the load capacitor C_2 (value equal to C_1) is now reset to ground (instead of the supply in the upper circuit) and will be charged with a constant current I_b. When Φ_{out1} is high, C_2 will be discharged by a NMOS switch M9 and reset to ground; when Φ_{out1} is low, the switch S_2 will be on and C_2 is charged by a constant current from a p-type current mirror and the delay of t_{d2} is generated. Observing the entire delay generator from Figure 2, the input clock Φ_{in} obtains two delays t_{d1} and t_{d2} in the upper and lower parts, respectively. Due to the opposite property of the two half delay generators, t_{d1} and t_{d2} are able to compensate the process variation between each other and then the total time delay could be more stable, in other words, process-insensitive.

The process variation compensation theory can be illustrated by the different graphics of Figure 3 that contains the typical waveforms from the upper (Figure 3(a)) and lower (Figure 3(b)) parts. The waveforms in 'fs' and 'sf' process corners, which produce the most significant drifts in inverter's threshold, are shown to be comparable with the typical corner ('tt' corner), from the analysis of the process variation effect. As shown also in Figure 3, the C_1/C_2's top-plate voltage V_{C1}/V_{C2} starts decreasing/increasing linearly once the input clock falls/rises, until it reaches the threshold voltage V_T of the following inverter. Meanwhile, the V_{tr1}/V_{tr2} will be triggered. Since the V_T of the inverter varies in different process corners, the V_{tr1}/V_{tr2} would trigger at different time and therefore the produced output clock would have a different time delay. Before analyzing the variation in the time-domain, it would be important to determine the slope of V_{c1} and V_{c2} when C_1/C_2 is discharging/charging. Then, since

$$i = C\frac{dV_C}{dt} \tag{1}$$

it implies that,

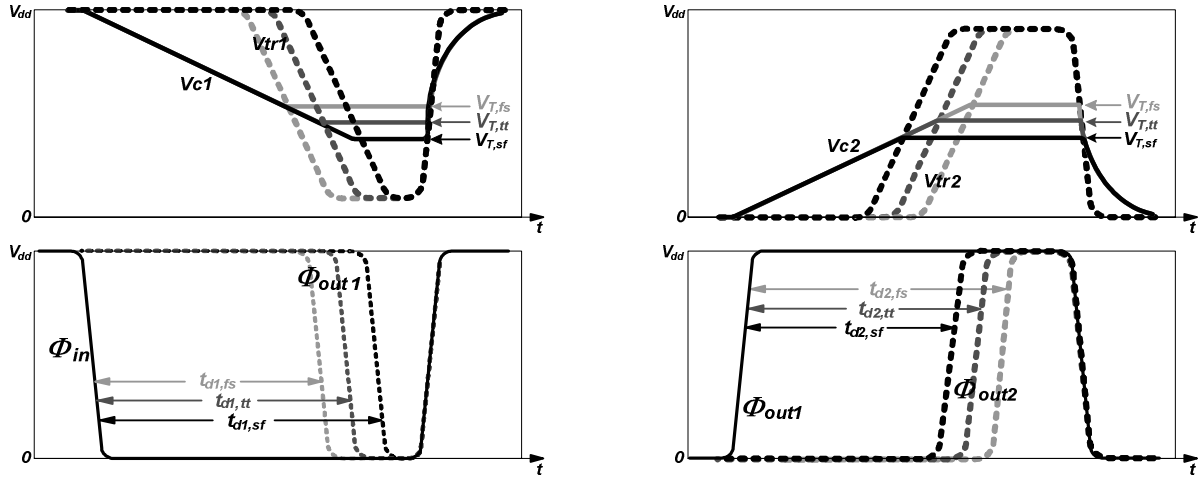
$$\begin{aligned} slope &= \frac{dV_C}{dt} = \frac{i}{C} \\ \Rightarrow slope\big|_{Vc1} &= \frac{dV_{C_1}}{dt} = -\frac{I_b}{C_1}, \\ slope\big|_{Vc2} &= \frac{dV_{C_2}}{dt} = \frac{I_b}{C_2} \end{aligned} \tag{2}$$

As C_1=C_2 it will lead to,

$$slope = -slope\big|_{Vc1} = slope\big|_{Vc2} \tag{3}$$

Thus, in the tt corner, the total delay will be given by

$$\begin{aligned} t_{d,tt} &= t_{d1,tt} + t_{d2,tt} \\ &= \frac{V_{T,tt} - V_{DD}}{slope\big|_{Vc1}} + \frac{V_{T,tt} - 0}{slope\big|_{Vc2}} \\ &= \frac{V_{T,tt} - V_{DD}}{-slope} + \frac{V_{T,tt} - 0}{slope} \\ &= \frac{V_{DD}}{slope} \\ &= const. \end{aligned} \tag{4}$$



(a) (b)

Figure 3: Characteristic waveforms in the (a) upper and (b) lower parts of the proposed advanced delay generator with process-variation

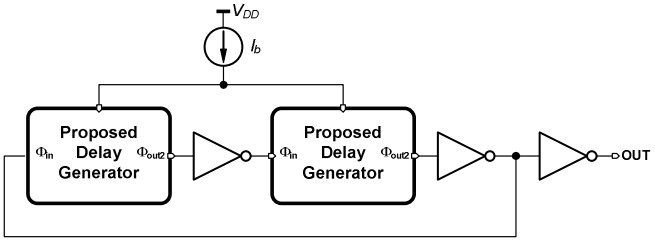


Figure 4: Tested oscillator containing two series-connected proposed delay generators

In addition, the threshold voltage V_T of the inverter is also related to the supply and it can be expressed as a function of V_{DD}. However, (4) is still valid since V_T can be cancelled from the calculation.

The results of time delays in the 'fs' and 'sf' corners are similar to the typical shown above and the total delay in each corner will be the same. Therefore, the problem existing in [5] [6], process variation induced by the inverter connected to V_C, is alleviated by the proposed compensation method.

IV. Measurement Results

The proposed delay generator provides a very narrow delay in the time domain that is quite difficult to be measured. Therefore, the delay generator must be connected with few inverters in order to build an oscillator where the delay's deviation in the time domain can be converted to the variation of the oscillation frequency. In other words, the oscillator will provide a clock output whose frequency will be changed by applying different bias currents I_b into the delay generator. From equation (2) to (4), the frequency of the oscillator f_{osc} can be expressed as

$$f_{osc} \propto t_d^{-1} = \frac{Slope}{V_{DD}} = \frac{I_b}{V_{DD}C_1} \qquad (5)$$

It is obvious that f_{osc} is proportional to the bias current I_b since both V_{DD} and C_1 are constants.

Moreover, in order to avoid measuring an extreme high frequency on the printed circuit board (PCB), two delay generators are connected in series in the oscillator as shown in Figure 4. The proposed current-controlled delay generator is implemented in 90nm CMOS technology and the micrograph of the tested chip is shown in Figure 5, with an active area of 7650μm^2.

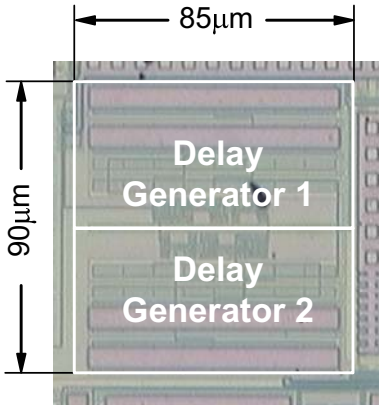


Figure 5: Micrograph of proposed current-controlled delay generator.

Figure 6 shows the measured characteristic curves of the 14 fabricated samples of the proposed current-controlled delay generator and Figure 7 illustrates the measured curve of the 12th sample whose result is close to the average of all 14 samples'. As shown in Figure 6 and 7, the oscillator's output frequency is almost directly proportional to the input bias current. When the bias current is large enough, the oscillator's frequency begins to be saturated since the overall time delay will be dominated by the delay in the intrinsic logic gates. On the other hand, if the bias current is quite small, the measurement becomes complicated because the accurate small current is hard to provide which also degrades the measurement accuracy of the input current. Therefore, the proposed current-controlled delay generator would be able to provide a precise clock from 40MHz to 400MHz (the double of the frequency because two delay generators are connected in series in the tested oscillator). Figure 8 shows the histogram of the oscillator's frequency at the maximum control bias current with a standard deviation of only 1.24%.

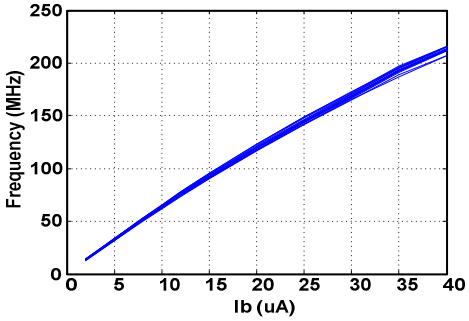


Figure 6: Measured characteristic curves of 14 fabricated samples.

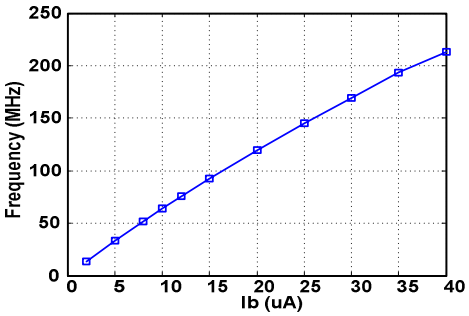


Figure 7: Measured characteristic curve of No. 12 sample.

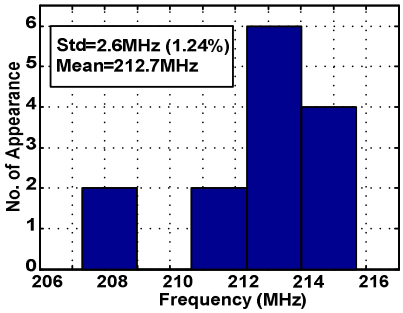


Figure 8: Statistics of measured oscillator frequency of 14 samples at I_b=40μA.

The performance comparison of the proposed delay generator with several prior designs is shown in Table I, where other results were obtained from transistor-level simulations with the BSIM4 model. The delay cells were tested by building the oscillator as shown in Figure 4. Therefore, the variation of the oscillator's frequency will represent the process variation of the tested delay generator. With an average frequency of 212MHz, which corresponds to a delay of 2.36ns in each proposed delay generator, the process variation of different delay cell designs are found and summarized in Table I. The variation of the proposed delay generator is the minimum among the 4 designs and the process corner simulation results are also shown in the Table I. Finally, the performance summary of the proposed delay generator is presented in Table II.

V. Conclusions

In this paper, a current-controlled delay generator which can be widely used in sampled-data systems has been introduced. It has been implemented in 90-nm CMOS operating at 1.1V. With the proposed threshold voltage compensation method, the presented delay generator becomes robust to process variations. Total 14 chip samples were measured and the standard deviation is 1.24% when the control bias current is 20μA.

TABLE I: BENCHMARK OF THE VARIATION WITH OTHER DESIGNS (THE AVERAGE f_{osc} = 212MHz)

	σ *	Process Corner Simulation **
This work	1.24%	-5.9%/+5.0%
gm/C circuit	3.18%	-13.4%/+14.9%
[6]	2.12%	-7.0%/+6.9%
[7]	2.26%	-10.7%/+9.0%

*: The standard deviation of this work is obtained from measured results while the others are from MC simulations with BSIM4 model.
**: The process corner simulation results are at transistor-level with BSIM4 model.

TABLE II: PERFORMANCE SUMMARY OF THE PROPOSED CURRENT-CONTROLLED DELAY GENERATOR

Technology	90nm CMOS
Power supply	1.1 V
I_b (Oscillator)	40 μA
I_b (Delay Gen.)	20 μA
Std. of variation	1.24%
Power of Oscillator	679μW
Power of Delay Generator	310μW
Active Area	85μm × 90μm

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