A 34fJ 10b 500 MS/s Partial-Interleaving Pipelined SAR ADC

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Abstract

A 10b 500MS/s ADC is presented that shares a full-speed SAR at front-end and interleaves the pipelined residue amplification with shared opamp and 2nd-stage SAR ADCs, which achieves high speed, low power and compact area. The prototype ADC in 65nm CMOS achieves a mean SNDR of 55.4dB with 8.2mW power dissipation at 1.2V. The active die area including the offset calibrations is 0.046mm^2.

Introduction

Low power consumption and high speed ADCs are highly demanded for battery-powered mobile applications. For high-resolution (≥10b), pipeline [1]-[3] and time-interleaved (TI) pipelined-SAR [4] ADCs are the most potential architectures to achieve high speed (>200MS/s), while their FoM are >90fJ/conv.-step. This paper proposes a partial interleaved pipelined-SAR architecture that implements a high speed single channel SAR for front-end sampling and conversion, which is then pipelined by time interleaved 2nd-stage low speed SAR ADCs. The design eliminates the sampling mismatches from TI-scheme and achieves high resolution, high speed and low power dissipation.

ADC Architecture and Implementation

Fig. 1 shows the ADC architecture and its timing diagram. The 1st-stage implements a high-speed 6b 2b/cycle SAR ADC. By using interpolation, two pairs of differential capacitive DACs (DAC$_A$ and DAC$_B$) instead of 3 are employed for the front-end sampling and conversion. Only the residue voltage at DAC$_A$ is processed and amplified by a low inter-stage gain of 4 and pipelined to 2nd-stage SAR ADCs in a 2×TI with opamp-shared scheme. The TI residue amplification capacitor arrays (RAC$_{A1}$ and RAC$_{A2}$) also serve as a reference division [5] for the 1st-stage ADC. The 2nd-stage consists of two TI-1b/cycle SAR ADCs that determine 5b output. Each SAR is built with a 6b split-DAC where extra 1 bit is for the offset cancellation [5]. Two stages have 1b overlapping for digital error correction that relaxes the conversion accuracy of 1st-stage to 7b, including the settling and matching of DAC$_A$ and DAC$_B$.

During the sampling phase (Φs=1&Φ_1=1), the differential input signal $\pm V_{in}$ are sampled onto the DAC$_A$, DAC$_B$, RAC$_{A1}$ and RAC$_B$, simultaneously. In the conversion phase (Φc=1&Φ_1=1) the 1st-stage solves the coarse 6b in 3 cycles (1.2ns), and the residue is generated within the DAC$_A$ and RAC$_{A1}$. When the conversion is completed (Φ_2=1), the RAC$_{A1}$ disconnects to DAC$_A$, and connects to the opamp's input. The residue at the top-plate of RAC$_{A1}$ is amplified to 2nd-stage SAR.

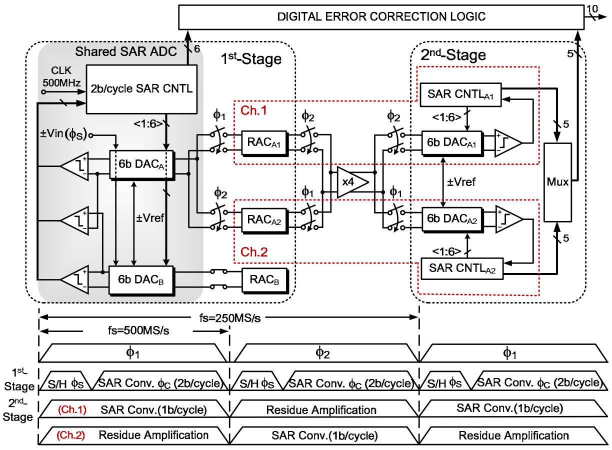

Fig. 1 Overall ADC architecture and its timing diagram.

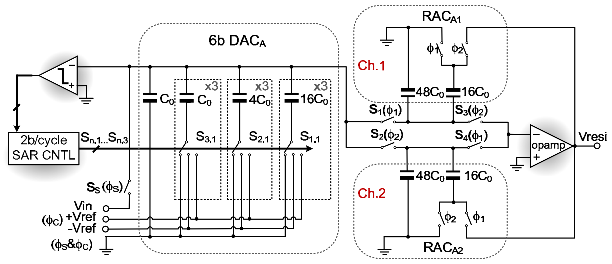

Fig. 2 1st-stage 6b SAR ADC w/ Opamp-shared TI-Residue Amplification.

Meanwhile the DAC$_A$ switched to RAC$_{A2}$ starts a new conversion. In the subsequent pipelined phase (Φ_1=1) when the rest 5b is determined by the 2nd-stage SAR, it is passed to digital error correction logic for the final 10b output. The front-end SAR ADC operates at 500MS/s, while each interleaved channel works at 250MS/s with an equivalent duration of 2ns to perform the amplification and conversion.

Fig. 2 shows the implementation of 1st-stage DAC$_A$ and the TI residue amplification. The input signal is pre-charged at top-plate of entire array via switch S$_S$, which is bootstrapped and controlled by Φs. Since the TI switches (S$_1$ and S$_2$) are kept on until its corresponding conversion is completed, no timing mismatches happen between two channels. During bit cycling, the RAC$_{A1}$ is involved in SA conversion and grounded to scale down the reference voltage [5], while another one RAC$_{A2}$ serves as a flip-around MDAC that feeds back a 16C$_0$ to opamp's output for the x4 residue amplification. The 6b DAC$_A$ is assigned as segment thermometer-code array instead of binary-weighted one to avoid the extra decode logic in SAR controller that reduces the loop delay. The DAC$_A$ and each RAC contain the same total units of 64C$_0$ that is determined by the thermal noise. A custom designed unit capacitance of 5.5fF is formed with fringe structure (2μm× 2.4μm) using the metal layer 1-5. The total input capacitance is

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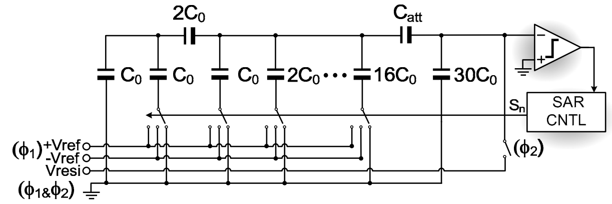

Fig. 3 2^{nd-}stage 6b SAR ADC implementation

1.4pF single-ended, half of which is from DAC_B and RAC_B. The switches S_1 and S_2 implemented between the DAC_A and RAC_A increase RC time constant required for each bit settling, which is relaxed to $\pm 1/2^8 V_{FS}$ due to 1b digital error correction. The small residue swing at the end of the 1st-stage conversion ($<18.75mV_{p-p}$) allows the switch to be designed with gate capacitance <10fF (3% of the RAC_A of 350fF), so that the error of charge injection and clock feedthrough is controlled within 10-bit accuracy. The channel gain mismatch mainly due to the mismatches between RAC_{A1} and RAC_{A2} are tolerated within the design constraint. The opamp implemented as a telescopic structure with gain-boosting [5] achieves 1.7GHz GBW and an open-loop gain of 69dB that is sufficient to suppress the opamp's finite gain error and memory effect. The comparators used in 1st-and 2nd-stage SAR are dynamic latch [5] for low power dissipation.

With ×4 inter-stage gain, the 2nd-stage SAR quantizing the residue from the 1st-stage is $1/16V_{in\text{-}FS}$. Besides, by 1b overlapping, $\pm V_{ref\text{-}2nd}$ is required to be equal to $\pm 1/16V_{ref\text{-}1st}$. Thus a 6b DAC with an attenuator C_{att} is used to scale down the reference by 16 as shown in Fig.3. The capacitance of C_0 and C_{att} is 5.5fF and 12fF, respectively. The low total equivalent capacitance of 176fF improves the bandwidth of the opamp.

The top-plate sampling avoids the extra charges transfer of input signal at the bottom to the top-plate of the DAC. Also, the distributed bottom-plate sampling switches is replaced by one top-plate switch S_S that simplifies the layout routing. However, the top-plate sampling together with the mismatch of C_{att} result in an overall inter-stage gain error, which is measured by using the code histogram statistics and calibrated in digital domain by multiplying a gain factor to 5b 2nd-stage digital output. The gain error calibration is implemented off-chip together with the digital error correction logic. In practice, the inter-stage gain error can be calibrated on-chip with low cost, which has already been implemented in our 2nd design. The offsets including the comparators in 1st- and 2nd-stage as well as the opamp are all on-chip calibrated by similar solutions done in [5]. The supplies are used directly as reference voltages for 1st- and 2nd-stage SA conversions.

Measurement Results

The ADC occupies 0.046mm^2 (330μm×140μm) core area and is fabricated in 1P7M 65nm CMOS with low-V_T option. Its die photo is shown in Fig. 4. Fig. 5 presents the measured SNDR of 20 chips. The chip with mean SNDR is selected to report the rest measurement results. Fig.6 shows both the measured FFT @ DC and near Nyquist input. Fig.7 shows the measured dynamic performances with and without gain calibration. The resulting ERBW is 280MHz. The DNL/INL before and after offset and gain calibrations are 22.7/19.5LSB and 0.49/1.1LSB, respectively. The total power consumption is 8.2mW at a 1.2V supply, including 4.5mW analog power (S/H, DAC, comparators and opamp) and 3.7mW digital power (clock generator, SAR logic and offset calibration). The performance summary and comparison with State-of-the-art ADCs are shown in Table I.

Acknowledgment

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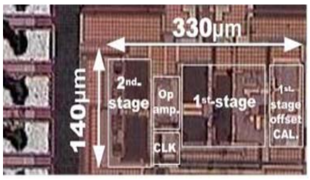

Fig.4 Die chip photograph.

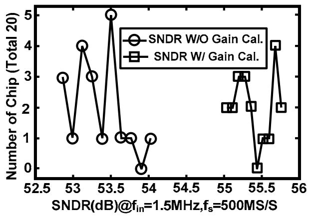

Fig.5 Measured SNDR Histogram.

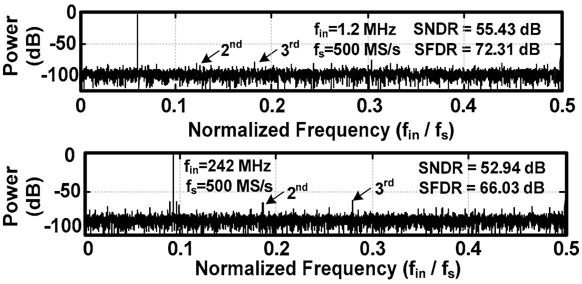

Fig. 6 16384 point FFT for 1.2&242MHz inputs (decimated by 25).

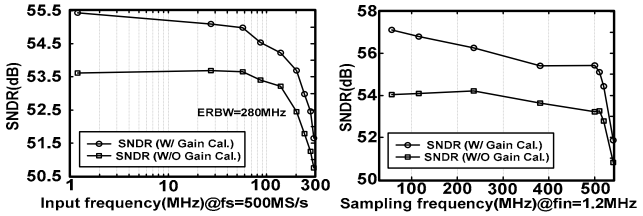

Fig. 7 Dynamic performance of the ADC (w/&w/o gain calibration).

TABLE I : Performance Summary and Comparison

	[1] VLSI' 11	[2] ISSCC' 11	[3] JSSC' 09	[4] CICC' 10	**This Work (w/&w/o gain cal)**	
Architecture	Pipeline	Pipeline	Pipeline	Pipeline-SAR	Pipeline-SAR	
Technology (nm)	40	40	90	65	65	
Resolution (bit)	11	12	10	10	10	
Sampling Rate (MS/s)	300	800	500	204	500	
Supply Voltage (V)	1.8	1/2.5	1.2	1	1.2	
Power (mW)	40	105	55	9.5	8.2	
Area (mm^2)	0.42	0.88	0.5	0.22	0.046	
DNL/INL (LSB)	0.3/1.5	0.4/2.1	0.4/1	0.74/0.9	0.48/1.1	0.58/1.6
SNDR (dB)	56.6	59	52.8	55.2	55.4	53.6
FoM =Power/($2^{ENOB@DC}$fs) (fJ/conv.-step)	240	180	310	95.4	34	42