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A Coin-Battery-Powered LDO-Free 2.4-GHz Bluetooth Low-Energy Transmitter with 34.7% Peak System Efficiency

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***Abstract*— This Brief reports a 2.4-GHz Bluetooth Low-Energy (BLE) transmitter (TX) that can operate against a coin-battery voltage discharging from 1.5 to 1 V, corresponding to a 99.2% battery capacity usage (BCU). Specifically, a class-B/C push-pull power amplifier (PA) with dual feedback control loops is proposed to dynamically adjust two gate biases, ensuring stable output power and low output HD_2. The TX fabricated in 65-nm CMOS occupies a die area of 0.5 mm^2, and achieves three stable power levels: $P_{out,H}$ (2.7 ± 0.4 dBm), $P_{out,M}$ (−0.1 ± 0.6 dBm) and $P_{out,L}$ (−2.5 ± 0.8 dBm). At $P_{out,H}$, the system efficiency reaches 34.7%. The 1-Mbps GFSK output (m = 0.5) and $HD_{2,3}$ comply with the BLE specifications, and the FSK error is 8.2%. A tiny demo board with an antenna, a crystal and a coin battery (Nanfu LR44) verifies the feasibility of the TX over-the-air, achieving 27.5 hours of continuous operation for a 1-dB reduction of the received power.**

Index Terms— Battery capacity usage (BCU), Bluetooth Low-Energy (BLE), CMOS, direct-coin-battery-powered (DCBP), output power, power amplifier (PA), system efficiency.

I. Introduction

LOW-COST wireless smart sensors (e.g. beacon tags) are the key enabler of a wide variety of Internet-of-Things (IoT) applications. To miniaturize the sensor's footprint while prolonging the battery lifetime, ultra-low-power (ULP) radios powered by coin batteries is a promising solution. Yet, the coin battery discharges from its nominal 1.5 V to its cut-off voltage ~1 V. Existing ULP radios [1-3] typically assume a constant supply voltage (V_{DD}) given by a low-dropout regulator (LDO), but the LDO induces power loss and limits the battery capacity usage (BCU).

To enhance the power efficiency and BCU, a coin-battery-powering (CBP) LDO-free TX compliant with the Bluetooth Low-Energy (BLE) standard is developed. The key idea is to stabilize the output power (P_{out}), and other key performance metrics, against an unregulated V_{DD} falling from 1.5 to 1 V. For instance, for a low-cost 1.5-V Nanfu LR44 coin battery delivering a 5-mA constant current, the BCU is 70% at 1.2 V, and 99.2% at 1 V, with a 24-hour total battery lifetime (Fig. 1). For a typical LDO having a 0.2-V dropout voltage, the BCU of [1-3] is only 70%. Also, for a constant current consumption, the power loss in the LDO also penalizes the TX power efficiency

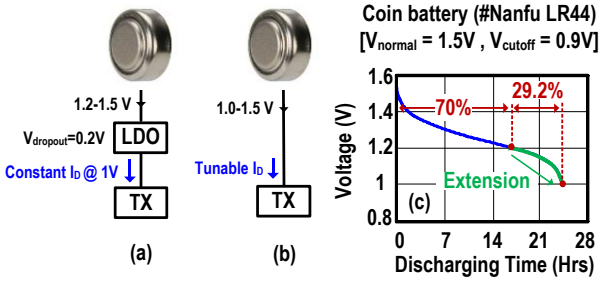

Fig. 1. (a) Conventional CBP TX with LDO. (b) Proposed CBP TX without LDO. (c) BCU of CBP TX with and without the LDO.

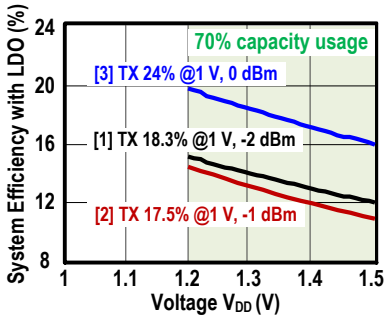

Fig. 2. Calculated TX efficiencies of the recently reported BLE TXs [1-3] assuming they are powered by a 1.5-V coin battery with a LDO.

(E_{TX}) of [1-3] (Fig. 2). In fact, the dropout voltage of the LDO is even higher if V_{DD} is excessive, resulting in a lower E_{TX}.

The proposed CBP TX features both P_{out} regulation and E_{TX} optimization to secure its performances over a wide range of V_{DD} from 1.5 to 1 V, extending the BCU to 99.2% (Fig. 1). Moreover, the current consumption can be downscaled at a high V_{DD} to freeze E_{TX}. The key building blocks are a push-pull class-C voltage-controlled oscillator (VCO) and a class-B/C push-pull power amplifier (PA). The latter is aided by dual feedback control loops to dynamically adjust the key biases, such that both P_{out} and 2nd-harmonic emission (HD_2) are well-controlled.

Section II introduces the proposed CBP TX and its design details. Section III summarizes the experimental results, and the conclusions are drawn in Section IV.

II. Proposed CBP TX and Design Details

The proposed CBP TX is based on an analog phase-locked loop (PLL), a VCO and a PA followed by a LC bandstop filter

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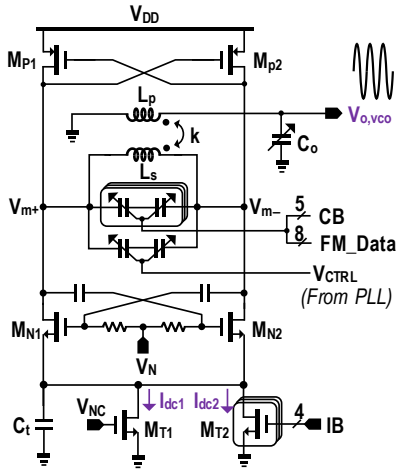

Fig. 3. Proposed push-pull class-C VCO with a transformer tank for D2S.

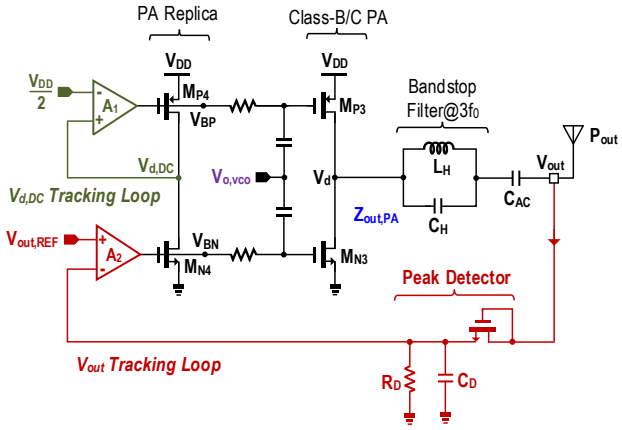

Fig. 4. Proposed class-B/C push-pull PA structure with dual feedback control loops to track the peak of V_{out} and $V_{d,DC}$.

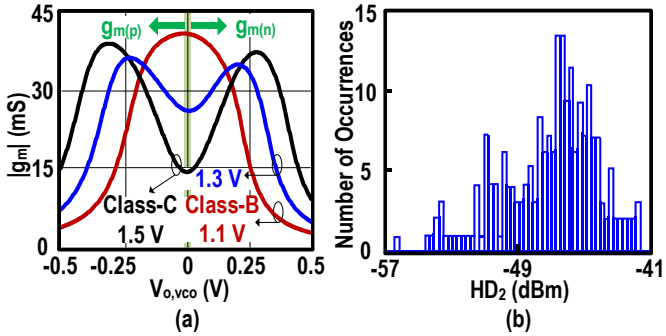

Fig. 5. (a) Simulated g_m of the class-B/C push-pull PA versus $V_{vco,o}$ at different V_{DD} and (b) Monto-Carlo simulation results of the HD_2 at V_{DD} = 1.2V (including both the process variation and device mismatch with 210 samples).

to suppress the HD_3. The open-loop GFSK modulation is realized by an 8-bit capacitor array applied in the VCO. Their design details are presented next.

A. Push-Pull Class-C VCO with an Output Transformer

The push-pull Class-C VCO [4] has demonstrated a higher power efficiency than the typical PMOS-/NMOS-only Class-C VCO. As shown in Fig. 3, the differential outputs of the VCO are extracted and combined to a single-ended one through a transformer. The differential-to-single-ended (D2S) conversion serves to boost the swing of the PA input by 3 dB and suppress the 2nd-harmnoic from 32 dBc (at $V_{m+/-}$) to 56 dBc (at $V_{o,vco}$), while does not induce extra power consumption when compared with the active D2S conversion circuit used in [5]. $M_{T1,T2}$ define the bias current (I_{dc1} + I_{dc2}) of the VCO. As V_{DD} is expected to vary specifically from 1.5 to 1 V, a roughly constant swing of $V_{o,vco}$ can be achieved by digitally tuning M_{T2} (4 bits) against V_{DD}.

To reduce the power consumption of the VCO, we choose large values of L_p (2.6-nH) and L_s (2.3 nH) to achieve a large tank impedance $|Z_{tank}|$ when looked from the secondary coil L_s of the transformer. According to the EM-simulation, Q_p = 19, Q_s = 18 and the coupling factor k is 0.8. Z_{tank} has two peaks located at 2.4 GHz and 7.4 GHz with magnitudes of ~560 and ~220 Ω. The overall g_m provided by $M_{N1,N2}$ and $M_{P1,P2}$ is ~3.72 mS, which only satisfies the gain condition at 2.4 GHz avoiding the bimodal oscillation.

A 5-bit binary-weighted switch-capacitor-array (SCA) and an A-MOS varactor are employed for coarse and continuous frequency tuning to cover the BLE band from 2.4 to 2.48 GHz with margin. An 8-bit thermometer-weighted SCA is utilized for the frequency modulation (FM) with a resolution of 7.8 kHz.

B. Class-B/C Push-Pull PA with Dual Feedback Loops for HD_2 Suppression and P_{out} Stabilization

It is critical to maximize the PA efficiency since it is the most power-hungry block in the BLE transmitter. The class-E [6]-[7] or class-F [8]-[9] PAs can have a high drain efficiency by reducing the overlap between the voltage and current waveforms of the switching transistors. Their differential input stages also help suppressing the HD_2 emission. However, if operating under a high V_{DD} (1 to 1.5 V), a large equivalent resistance seen by the PA switching transistors is needed to maintain a small P_{out} (0 to 3 dBm). The need of a bulky output matching network (MN) to realize a large impedance scaling-up ratio would in turn degrade the PA efficiency and increase chip area.

Compared with the class-E/-F counterparts, the single-ended (SE) class-D PA can generate lower P_{out} at the same V_{DD} that may avoid the use of lossy and bulky MN. However, it suffers from poor 2nd- and 3rd- harmonic emission and thus needs either extra on-chip filters [5], or a calibration loop that matches the conduction angles between the NMOS and PMOS transistors by detecting the common-mode voltage at the PA replica output [10] for 2nd-harmonic suppression. Both methods would inevitably degrade the overall TX system efficiency.

In this work, a class-B/C push-pull PA is employed to avoid the MN when delivering a low P_{out} similar to the SE class-D PA. A dynamic biasing loop is proposed to suppress the HD_2 emission without affecting the PA efficiency. M_{N3} and M_{P3} in the PA (Fig. 4) are sized as 100/0.06 μm and 200/0.06 μm to ensure that $\mu_n(W/L)_{N3} = \mu_p(W/L)_{P3}$, where μ_n (μ_p) is the mobility of M_{N3} (M_{P3}). Thus, the matching between the conduction angles of M_{N3} and M_{P3} can be guaranteed by dynamic biasing M_{P3} to ensure the DC voltage of the PA output V_d is always equal to mid-V_{DD}. A 25×-downsized PA replica (M_{N4} and M_{P4}) with a maximum current of ~18 μA is employed to generate a replica DC voltage $V_{d,DC}$ of the PA output V_d and an error

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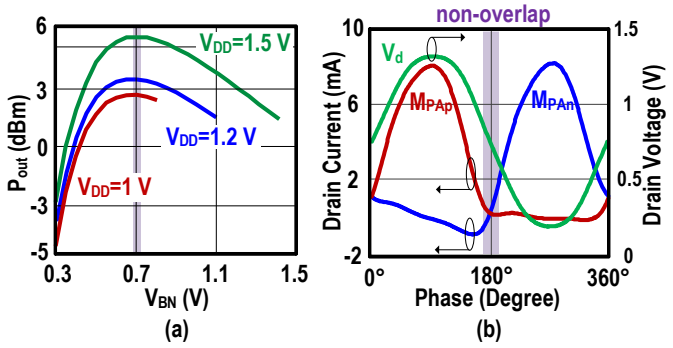

Fig. 6. Simulated (a) relationship between P_{out} and V_{BN} and (b) drain currents and voltage of M_{N3} and M_{P3} when delivering $P_{out,H}$ at V_{DD}=1.5 V.

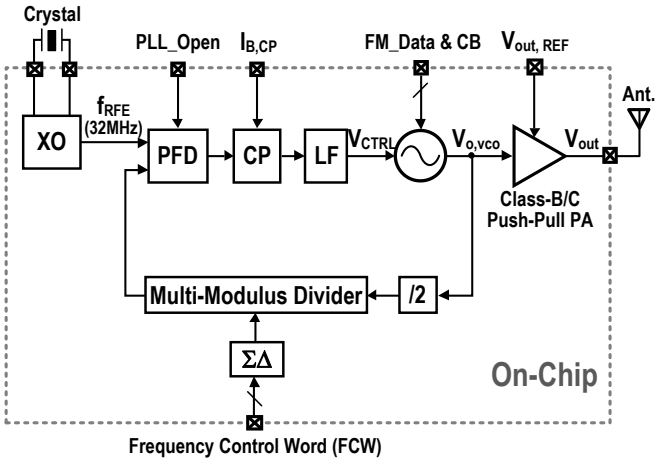

Fig. 7. Block diagram of the entire CBP TX.

amplifier A_1 locks $V_{d,DC}$ to mid-V_{DD} by adjusting the gate bias V_{BP} of M_{P3}. As shown in Fig. 5(a), the simulated $g_{m(N3)}$ and $g_{m(P3)}$ are symmetrical at different V_{DD}. The simulated HD_2 in SF and FS corners is the same (−45 dBm) as that in the TT corner. Without the $V_{d,DC}$ tracking loop, the simulated HD_2 drops to −28 dBm in the SF corner. The monte-Carlo simulation shows the mean and standard deviation of HD_2 are −47.6 dBm and 2.7 dB, respectively. All the HD_2 performances are below −42 dBm [Fig. 5(b)]. To suppress the 3rd-harmonic emission, a band-stop filter (L_H, C_H) is inserted between the PA output and the antenna.

Here, the impedance $Z_{out,PA}$ at the PA output is 50 Ω to avoid the use of MN. For the push-pull PA (Fig. 4) to deliver a 3-dBm P_{out} at the antenna, the drain amplitude V_d is 0.45 V. Practically, V_{DD} >1.1 V is essential to surmount the loss of the bondwire. When V_{DD} is high, the amplitude of V_{out} needs to be kept unchanged to ensure a constant $P_{out} = V_{out,amp}^2/2R_{ant}$. Here a V_{out} tracking loop is employed to stabilize P_{out} under PVT variation, by adjusting the gate bias voltage V_{BN} of $M_{N3,N4}$. The bandwidth of the two loops are both ~4 MHz determined by the error amplifiers A_1 and A_2. The simulated phase margin of the V_{out} tracking loop is ~80° when the $V_{d,DC}$ tracking loop is kept closed. For a certain P_{out}, the PA is possible to be biased at Class A/B region with a larger V_{BN} [Fig. 6(a)]. To keep the PA always in the Class B/C to maximize its power efficiency, we need to keep a monotonic relationship between P_{out} and V_{BN}. This can be achieved by using a low supply voltage for the error amplifier A_2 to limit the maximum V_{BN} to ~0.7 V [Fig. 6(a)].

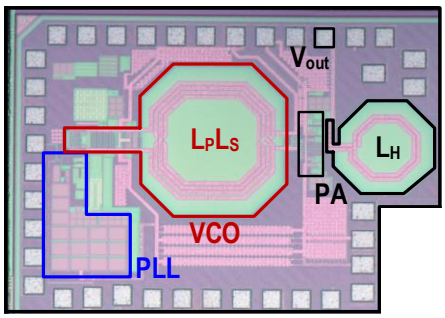

Fig. 8. Chip micrograph of the CBP TX.

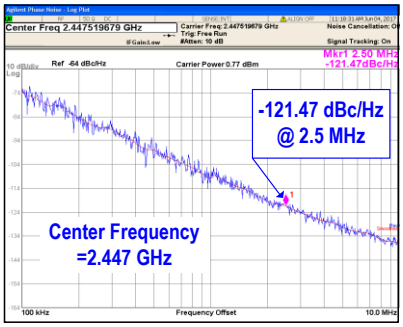

Fig. 9. Measured VCO phase noise at 2.447 GHz at V_{DD} = 1.2 V.

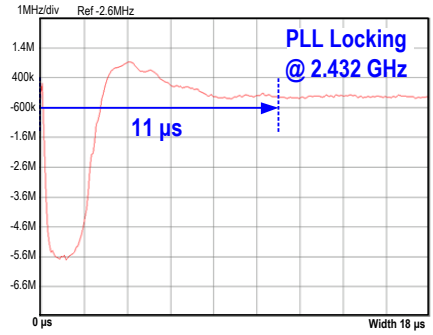

Fig. 10. Measured settling time of analog PLL down to ±50 kHz frequency error.

From simulation, the PA reaches its maximum efficiency of 47% at V_{DD} = 1.1 V (class-B mode) when delivering a P_{out} of 3 dBm. When V_{DD} is high, the PA efficiency drops since the output swing is kept constant. Fortunately, the PA enters into the class-C mode when V_{DD} is high [Fig. 5(a)]. The reduced conduction angle of the current aids improving the drain efficiency that reduces the degradation of the PA efficiency [Fig. 6(b)]. From simulations, the PA efficiency slightly degrades to 44% at V_{DD} = 1.5 V.

To offer three power levels at P_{out}, M_{N3} and M_{P3} are sub-divided into two parts (P_{ST1} : P_{ST2}) with a scale of (3 : 2). The expected power levels are: +3 dBm ($P_{out,H}$) when $P_{ST1,2}$ are ON, 0 dBm ($P_{out,M}$) when only P_{ST1} is ON, and finally −3 dBm ($P_{out,L}$) when only P_{ST2} is ON.

C. CBP TX Operation

Fig. 7 shows the entire CBP TX architecture. A fractional-N analog PLL is employed to lock the VCO frequency to the desired channel before data transmission. The 4th-order passive loop filter helps suppress the noise from the ΣΔ modulator and

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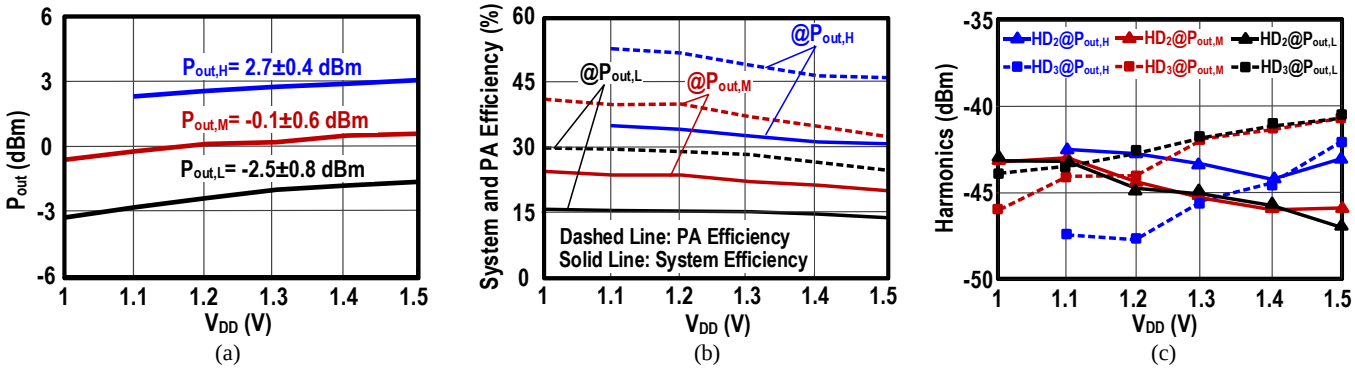

Fig. 11. Measured (a) P_{out}, (b) PA and system efficiencies, and (c) HD_2 and HD_3 of the CBP TX versus V_{DD}.

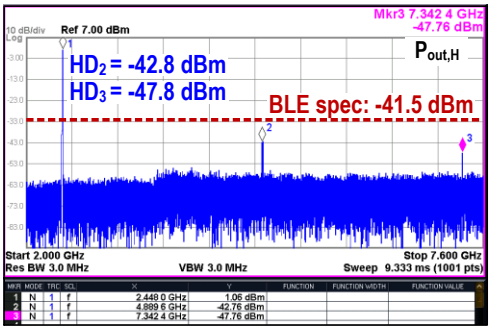

Fig. 12. Measured one-tone output spectrum @ $P_{out,H}$ (V_{DD}=1.2 V).

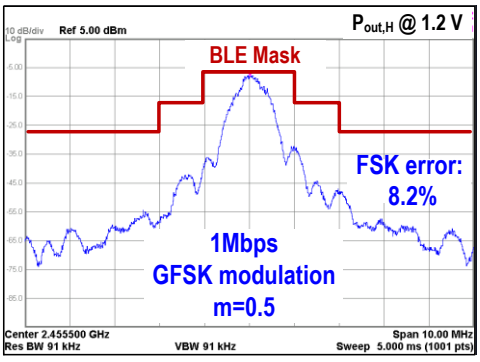

Fig. 13. Measured GFSK modulated output spectrum.

reference spur. Once the channel is selected, the PLL loop is opened by disabling the phase-frequency detector (PFD) and the FM data transmission is realized by directly modulating the capacitor bank of the VCO as proposed in [2]. The PLL can also be reused to provide a stable LO signal for the receiver.

III. Experimental Results

A. TX Performance

The CBP TX prototyped in 65-nm CMOS occupies a die area of 0.5 mm^2 (Fig. 8). The measured VCO frequency tuning range is from 2.3 to 2.6 GHz. At 2.447 GHz, the measured phase noise of VCO at 2.5 MHz offset is −121.47 dBc/Hz (spec: −102 dBc/Hz) at V_{DD} = 1.2 V (Fig. 9) and it degrades to –118 dBc/Hz at V_{DD} = 1 V.

The analog PLL consumes 0.5 mA at a fixed supply voltage of 1 V, dominated by the charge pump current of 0.3 mA. Using a reference frequency of 32 MHz, the PLL measures a settling time of ~11 µs when settled to 2.432 GHz within a frequency

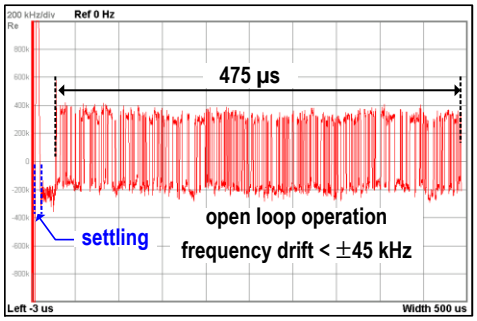

Fig. 14. Measured demodulated TX frequency for 475 μs BLE packet in the open-loop operation.

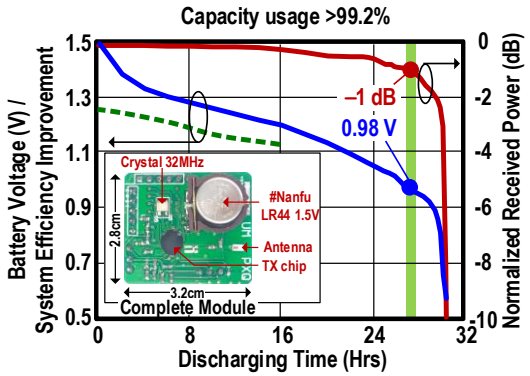

Fig. 15. Measured battery voltage (Solid-line), system efficiency improvement ratio (Dash-line) and normalized received power (Solid-line) versus time when the proposed TX directly powered by a coin battery (*Nanfu LR44* 1.5 V). Inset is the complete CBP TX module.

error of ±50 kHz (Fig. 10). At 2.436 GHz, the reference and worst fractional spurs measure −60.4 and −40 dBc, respectively.

The TX supports three output power levels: $P_{out,H}$, $P_{out,M}$ and $P_{out,L}$ as plotted in Fig. 11(a), where the cable and PCB loss (~1.5 dB) is de-embedded. When delivering $P_{out,M}$ and $P_{out,L}$, the output power is within the range of −0.1 ± 0.6 and −2.5 ± 0.8 dBm, respectively, when V_{DD} changes from 1.5 to 1 V (BCU =99.2%). When delivering $P_{out,H}$, a minimum V_{DD} of 1.1 V is used to prevent further degradation of $HD_{2,3}$.

Fig. 11(b) plots the measured system (PA + VCO) and PA efficiencies at three different P_{out} levels, i.e. $P_{out,H}$, $P_{out,M}$, and $P_{out,L}$. When delivering $P_{out,H}$ at 1.1 V, the push-pull PA has a maximum efficiency of 52.4%, and the corresponding system efficiency is 34.7%. When powered by a 1.5 V battery using an LDO, the system efficiency will drop to 25.4% while the

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TABLE I.
SUMMARY AND PERFORMANCE COMPARISON WITH PRIOR ART.

	This work	ISSCC'15 [1]	TMTT'12 [2]	ISSCC'11 [3]	JSSC'16 [7]	TMTT'13 [11]
Applications	**BLE**	BLE	BAN	Healthcare	BLE	BLE
Require LDO? *	**NO**	Yes	Yes	Yes	Yes	Yes
V_{DD}	**1 to 1.5**	1	1	1	0.5 / 1 %	1
Coin-Battery BCU (%)	**99.2 (1.5→1 V)**	70 (1.5→1.2 V)	70 (1.5→1.2 V)	70 (1.5→1.2 V)	70 (1.5→1.2 V)	70 (1.5→1.2 V)
E_{TX} (%) @ P_{out} (dBm)	**19→22 @ −0.1±0.6 14→15.1 @ −2.5±0.8**	18.3 @ −2	17.5 @ −1	24 @ 0	36 @ 3 28 @ 0	25 @ 1.6
E_{LDO+TX} (%) @ P_{out} (dBm)	**19→22 @ −0.1±0.6 14→15.1 @ −2.5±0.8**	12→15 @ −2	11.6→14.6 @ −1	16→20 @ 0	12→15 @ 3 9.3→11.6 @ 0	17→20 @ 1.6
TX Active Area (mm^2)	**0.5**	0.8 #	1.54	1.1 #	0.65	0.6 #
$HD_{2,3}$ (dBm) @ all P_{out}	**< −41.5**	< −49	N/A	N/A	< −47	< −32
VCO Phase Noise @ 2.5 MHz (dBc/Hz)	**−121.5**	N/A	−118.5	N/A	−116 (@1 MHz)	−108.3 (@1 MHz)
CMOS Technology	**65 nm**	40 nm	130 nm	90nm	28 nm	130 nm

* Assume LDO dropout voltage= 0.2 V # Estimated from the chip micrograph % 0.5 V for DCO and PA and 1 V for the ADPLL

measured system efficiency of our CBP TX is 30.5% at V_{DD}=1.5 V.

Fig. 11(c) shows the measured HD_2 and HD_3 at different P_{out} levels with an off-chip capacitor of 0.5 pF, which are all below −41.5 dBm. Fig. 12 shows the single-tone output spectrum when delivering $P_{out,H}$ at V_{DD} = 1.2 V.

Fig. 13 shows the GFSK modulation spectrum using 1-Mbps data rate and modulation index m=0.5. The measured FSK error is 8.2% while the open-loop frequency drift during one BLE package (475 μs) is within ±45 kHz (Fig. 14).

B. System Demo and Comparison

To demo the data transmission over-the-air, the TX chip is wire-bonded to a tiny evaluation board (2.8×3.2 cm^2) with a coin battery (Nanfu LR44), a 32-MHz crystal, and an RF ceramic chip antenna is developed. The Agilent PXA N9030A with an antenna is used to mimic a receiver placed 10 cm away from the TX. After the TX continuously works for 27.5 hours, the battery voltage drops from 1.5 to 0.98 V (BCU=99.2%) and the received power drops only 1 dB (Fig. 15). Compared with the case that operates under a constant current and an LDO, the system efficiency of the CBP TX can be improved by 1.24× /1.16× at a battery voltage of 1.5 V/1.2 V (Fig. 15).

Table I compares the proposed CBP TX with the state-of-the-art BLE TXs. By eliminating the LDO, our design can extend the BCU by 29.2%. Although [7] can achieve a higher system efficiency of 36% at P_{out} = 3 dBm, an extra LDO is required if it is directly powered by a 1.5-V coin battery which degrades the overall system efficiency to 15%. Our design demonstrates the highest ETX when directly powered by the 1.5-V coin battery by avoiding the use of the LDO.

IV. CONCLUSIONS

This paper proposed a CBP LDO-free TX for the BLE standard. It is based on a class-B/C push-pull PA with dual feedback control loops to realize dynamic biasing against an inconstant coin-battery voltage (1.5 to 1 V). By eliminating the LDO, both the system efficiency and BCU are improved. The TX fabricated in 65-nm CMOS offers three stable power levels: $P_{out,H}$ (2.7 ± 0.4 dBm), $P_{out,M}$ (−0.1 ± 0.6 dBm) and $P_{out,L}$ (−2.5 ± 0.8 dBm). The peak system efficiency is 34.7% at $P_{out,H}$. A demo board verified the feasibility the TX via over-the-air transmission. The TX can operate continuously for 27.5 hours with only 1 dB output power drop, corresponding to a BCU of 99.2%.

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