Generalized Type III Controller Design Interface for DC-DC Converters

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***Abstract*—In this paper, a generalized Type III controller design interface for DC-DC converters is built and presented in order to calculate the compensator parameter values in a more convenient and fast way. When the specifications of the DC-DC converter (buck, boost, buck-boost, etc.) are input to the MATLAB design interface, the corresponding parameters values (resistors and capacitors) of the Type III compensator and the bode plot of the DC-DC converter open loop gain can be obtained. By designing the Type III controller though this interface, the DC-DC converter can obtain stable and fast transient response performances with small steady state error. Finally, simulation results using 65-nm CMOS technology are presented to verify the developed generalized Type III controller design interface for different DC-DC converters.**

I. INTRODUCTION

In the world, almost every electronic product uses several components that are designed to be operated under a constant voltage source. There are many applications of DC-DC converter such as bioelectric products, PV cells, battery applications and so on [1] - [3]. Both of them have different requirements in terms of supply voltage levels, operation frequency and current consumption levels. Fig. 1 shows some examples of today electronic products' requirements. As the source voltages from batteries may not match with the component supply voltage rating, or may vary considerably around the normal specifications, DC-DC converters are usually required.

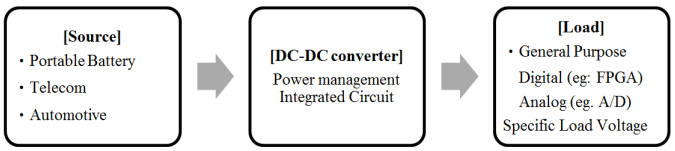

Fig .1. An example of nowadays electronic products requirements [4]

Generally speaking, a DC-DC converter can be classified into three general types such as: (i) Buck converter, or step-down converter in which the output voltage is smaller than the input voltage, (ii) Boost converter, or step-up converter in which the output voltage is larger than the input voltage, and (iii) Buck-boost converter, a converter that combine the characteristics of buck and boost topologies, in which the output voltage can be larger or smaller than the input voltage.

In order to obtain stable and fast transient response performance with small steady state error for DC-DC converters, Type II compensators are widely used in the closed control loops. Although the required components of Type II compensator used are less than Type III compensator, it can boost the phase up to +90 degrees only. Therefore, for some DC-DC converter topologies such as boost converter, it is insufficient for the compensation by using the Type II compensator because it requires the compensator to have a phase angle larger than 90 degrees. Thus in those cases, the Type II compensator cannot provide enough phase boost to keep the closed-loop stable, and this is where a Type III compensator is required. A Type III compensator can theoretically boost the phase up to +180 degrees at some frequencies, and for that reason it can provide the required phase boost to maintain a reasonable phase margin.

In this paper, in order to obtain i) stable, ii) fast transient response and iii) small steady-state error performances for different DC-DC converters, the design of the closed-loop Type III controller will be presented and discussed in Section II. In Section III, a generalized Type III controller parameters design interface for different types DC-DC converters (buck, boost, buck-boost, cuk, etc.) is also constructed in order to calculate the compensator parameters values in a more convenient and fast way under the design specifications. Finally, based on the developed interface, simulation results using 65-nm CMOS technology are also done for buck and boost DC-DC converters in order to verify the convenience and effectiveness of the generalized Type III controller design interface.

II. DESIGN OF CLOSED-LOOP TYPE III CONTROLLER FOR DC-DC CONVERTERS

A. Principle of The Closed-Loop Controller

In DC-DC switching converter systems, the whole architecture can be expressed as a negative feedback structure, and the closed-loop control block diagram of DC-DC switching power converter is shown in Fig. 2. In Fig. 2, $T_c(s)$ represents the transfer function for the error amplifier and compensation network; $T_m(s)$ represents the transfer function of a pulse-width modulator; $T_p(s)$ represents the transfer function for a type of DC-DC power converter (can be any DC-DC converter topology); and β represents the feedback network. Hence, the closed-loop control block diagram of the DC-DC converter system can be modeled by a typical control system indicated in Fig. 3.

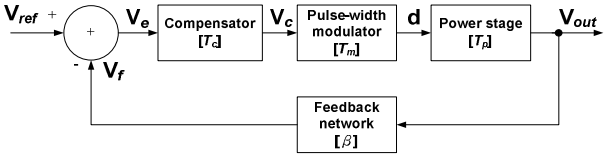

Fig. 2. Closed-loop control block diagram of DC-DC switching power converter system

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From Fig. 3, G(s) represents the sum of transfer functions of $T_c(s)$, $T_m(s)$ and $T_p(s)$, while β is the feedback network function. Here the feedback signal V_f will be subtracted from the reference signal V_{ref} and generate a new error signal V_e into the function G(s). As a result, the closed-loop transfer function can be got as (1):

$$T_{cl}(s) = \frac{G(s)}{1+\beta G(s)} \quad (1)$$

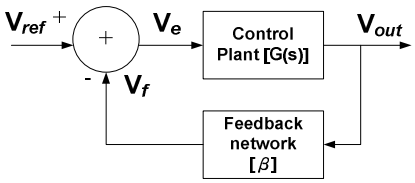

Fig. 3. Block diagram of typical closed-loop control system

B. Pulse-Width Modulator

As Fig 4 indicates, a typical pulse-width modulation (PWM) generation circuit consists of a comparator. The compensation output error signal V_c, is fed into the inverting terminal on the comparator and a ramp signal V_{ramp} operating at the switching frequency f_{sw}, is fed into the non-inverting terminal respectively. Therefore, the comparator will be triggered to high level (make the switch to turn on) if the error signal V_c is larger than the ramp signal V_{ramp}; On the other hand, the comparator will be triggered to low level (make the switch to turn off) if the error signal V_c is smaller than the value of the ramp signal V_{ramp}. Consequently, a specified duty cycle of an output waveform can be generated by the varying error signal and is used to control the output voltage of the converter system. A clear operation process and waveforms for PWM generation circuit is shown in Fig. 5.

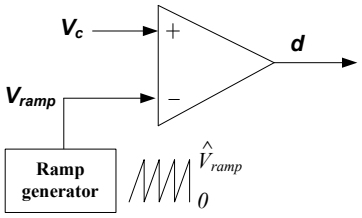

Fig. 4. PWM generation circuit

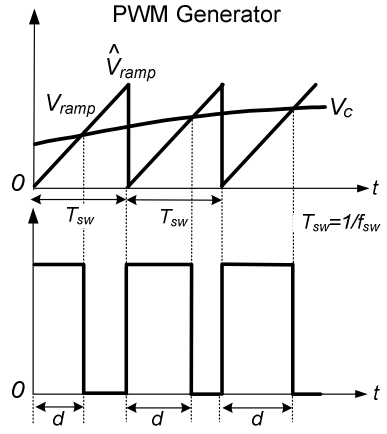

Fig. 5. PWM generation circuit waveform

In order to design a closed-loop DC-DC converter system, the transfer function of pulse-width modulator (T_m) is necessary to be deduced. By the circuit waveform as shown in Fig. 5, it can be observed that the ratio of the error signal to the ramp voltage will be equal to the duty cycle. Therefore, the transfer function of pulse-width modulator (T_m) can be easily deduced as (2) ,where $\hat{V}_{\text{ramp}}$ represents the peak value of ramp signal:

$$T_m(s) = \frac{d}{V_c} = \frac{1}{\hat{V}_{\text{ramp}}} \quad (2)$$

C. Feedback Network

From the feedback network, it operates as a voltage divider in the DC-DC power converter system. Fig. 6 shows several circuits diagrams of feedback network; Fig. 6(a) is voltage divider circuit so that it is independent of the frequency; Fig. 6(b) is a lead feedback network and Fig. 6(c) is a lag feedback network respectively. In this paper, Fig. 6(a) is applied because it does not need to involve the frequency so that it can be designed easily. Moreover, Table I summarizes their transfer functions.

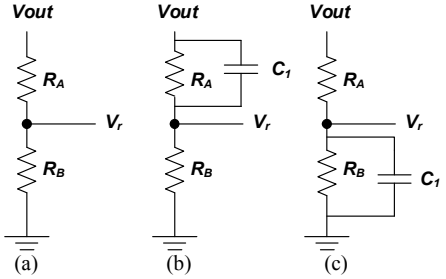

Fig. 6. Circuit diagrams of thee feedback network

TABLE I TRANSFER FUNCTIONS OF THREE FEEDBACK NETWORK

Type	Fig. 6(a)	Fig. 6(b)	Fig. 6(c)
Transfer Function β	$\frac{R_B}{R_A+R_B}$	$\frac{R_B}{R_A+R_B}\frac{1+sC_1R_A}{\left(1+\frac{sC_1R_AR_B}{R_A+R_B}\right)}$	$\frac{R_B}{R_A+R_B}\frac{1}{\left(1+\frac{sC_1R_AR_B}{R_A+R_B}\right)}$

D. Type III Compensator

Fig. 7 shows the circuit diagram of a Type III compensator, which composes of an error amplifier, three resistors (R_1, R_2 and R_3) and three capacitors (C_1, C_2 and C_3) respectively. By finding the input and output impedance as shown in (4) and (5), the voltage transfer function of Type III controller can be obtained as (3):

$$T_c(s) = T_{\text{type III}}(s) \equiv -A_v(s) = \frac{Z_f}{Z_i}$$

$$= \frac{R_1+R_3}{C_2R_1R_3} \times \frac{\left(s+\frac{1}{R_2C_1}\right)\left[\left(s+\frac{1}{C_3(R_1+R_3)}\right)\right]}{s\left(s+\frac{C_1+C_2}{R_2C_1C_2}\right)\left(s+\frac{1}{C_3R_1}\right)} \quad (3)$$

Where

$$Z_f = \frac{s+\frac{1}{R_2C_1}}{sC_2\left(s+\frac{C_1+C_2}{R_2C_1C_2}\right)} \quad (4)$$

$$Z_i = \left(\frac{R_1R_3}{R_1+R_3}\right)\frac{s+\frac{1}{C_3R_1}}{s+\frac{1}{C_3(R_1+R_3)}} \quad (5)$$

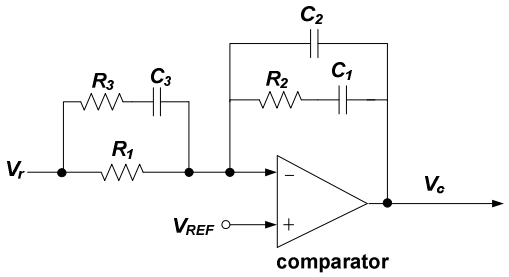

Fig. 7. Circuit diagram of a Type III compensator

From 3, the three poles (one at the origin) and two zeros are expressed in Table II:

TABLE II POLES AND ZEROS FOR THE TYPE III COMPENSATOR

Poles		Zero	
f_{p1}	0 (at origin)	f_{z1}	$\frac{1}{2\pi * R_2C_1}$
f_{p2}	$\frac{C_1 + C_2}{2\pi * (R_2C_1C_2)}$	f_{z2}	$\frac{1}{2\pi * C_3(R_1 + R_3)}$
f_{p3}	$\frac{1}{2\pi * C_3R_1}$		

After comprehending the characteristics of the Type III compensator network, its components values can be calculated. The corresponding value of crossover frequency f_c should be considered first, that it is usually defined as a frequency that the magnitude of the loop gain is equal to unity. Generally speaking, the crossover frequency can be set as a range of 1/5 to 1/10 of switching frequency. Apart of them, there are two other recommendations for deliberating the crossover frequency. First, the crossover frequency is confined with bounded with the upper range of the lowest right hand plane zero (RHPZ) location, because the selection should be lower than the worst case of the RHPZ position, in order to limit the duty ratio's slew rate. An adequate result can be given by choosing it below 30% of the lowest RHPZ position[5] (f_c<0.3f_{zp}). Another consideration concerns is the resonant frequency, since the DC-DC converter system would be unstable if there were insufficient gain to damp LC network of the output impendence. Therefore, the crossover frequency must be placed at least three times of the resonant frequency [5] (f_c>3f_o).

Since the compensation network can accurately go to the required gain and phase once the gain and phase at specified crossover frequency is known, a new mathematical tool called K-factor [6] will be used to calculate the Type III controller components' values. Hence, the K-factor equation for Type III compensator is:

$$K = \left\{\tan\left[\left(\frac{\varphi_m}{4}\right) + 45°\right]\right\}^2 \tag{6}$$

Where the $\varphi_m$is the required phase boost for the Type III compensator.

From Fig. 8, it is shown that the K factor of Type III compensator can theoretically boost up from 0^o to 180^0 but in fact approximately 160^o only because if 180^o is used to boost up, the K-factor will become undefined and this is one of the important points while designing the closed-loop Type III compensator by using this method.

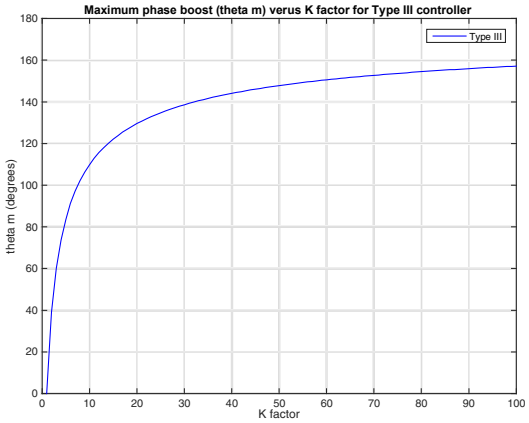

Fig. 8. Maximum phase boost φ_m vs. K factor for Type III compensator

By choosing the conventional DC-DC boost converter as a design example, the next step is to calculate the compensator gain ($T_c(j\omega_c)$) and the required phase boost (φ_m) needed at the crossover frequency for the boost converter. The compensator gain will be calculated first by plug in s=jω_c into the magnitude of the transfer function of boost converter power stage [7] as shown in (7):

$$\left|T_p(j\omega_c)\right| = T_{p0}\frac{\left(1+j\frac{\omega_c}{\omega_{zn}}\right)\left(1-j\frac{\omega_c}{\omega_{zp}}\right)}{1+j\frac{\omega_c}{Q\omega_0}-\left(\frac{\omega_c}{\omega_0}\right)^2} \tag{7}$$

By multiplying (7) to the transfer function of feedback network (β) and pulse-width modulator (T_m), the magnitude of the compensator can be found as:

$$|T_c(j\omega_c)| = \frac{1}{|T_p(j\omega_c)|*\beta*T_m} \tag{8}$$

Then the required phase boost (φ_m) should be calculated. Similar with the calculated gain above, by plug in s=jω_c into the phase of the transfer function of boost converter [7], the phase with the power stage at the crossover frequency $\varphi_{Tp}(\omega_c)$ is calculated as (9):

$$\varphi_{Tp}(\omega_c) = -180° + \tan^{-1}\left(\frac{\omega_c}{\omega_{zn}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{zp}}\right) - \tan^{-1}\left[\frac{\left(\frac{\omega_c}{Q\omega_0}\right)}{1-\left(\frac{\omega_c}{\omega_0}\right)^2}\right] \tag{9}$$

The required phase boost (φ_m) can be calculated by using the phase margin (PM) specification and the phase of the power stage at crossover frequency $\varphi_{Tp}(\omega_c)$ as shown in (10):

$$\varphi_m = PM - \varphi_{Tp}(\omega_c) - 90° \tag{10}$$

After the required gain $|T_c(j\omega_c)|$ and required phase boost φ_m for the compensator are calculated, the value of the K factor can be calculated. Therefore, the value of the Type III compensator components can be calculated by setting R_1 by

the designer itself. Then the other components can be calculated by the following equations:

$$C_2 = \frac{1}{\omega_c * |T_c| * R_1} \quad (11)$$

$$R_3 = \frac{R_1}{K-1} \quad (12)$$

$$C_1 = C_2 * (K-1) \quad (13)$$

$$C_3 = \frac{1}{\omega_c * \sqrt{K} * R_3} \quad (14)$$

$$R_2 = \frac{\sqrt{K}}{\omega_c * C_1} \quad (15)$$

III. A Generalized Type III Controller Parameters Design Interface for DC-DC Converters

Hence, a generalized Type III controller parameters design interface is developed in this paper, so that it can provide a more convenient and fast way to calculate the corresponding Type III controller parameters for different types of DC-DC converter in order to obtain stable and fast transient response with small steady-state error system performances. Moreover, the design step for finding the parameters of the Type III controller is summarized as below:

- Transfer function of power stage (e.g. Buck/Boost converter) (T_p)
- Transfer function of pulse-width modulator (T_m)
- Transfer function of feedback network (β)
- Transfer function of the compensator (T_c)

1. Design the crossover frequency (f_c) and the desired phase margin (PM);
2. Determine the gain value and the phase equation of the DC-DC converter at crossover frequency;
3. Design the gain of the Type III compensator and the required boost phase at f_c;
4. Calculate the separation factor (K);
5. Calculate the component parameters of the Type III compensator and its poles and zeros;
6. Combine all the transfer function in above steps to determine whether the specified phase margin is located at f_c.

Fig. 9 shows a generalized Type III controller parameter design interface constructed by using the Matlab GUI tools. As shown in Fig. 9, the right up corner illustrates several types of DC-DC converter topology for selection. Then the left hand side is the interface for the users to input the DC-DC converter specification. Those specifications that need the users to input are input voltage (V_{in}), output voltage (V_{out}), load resistance (R), capacitor (C) and inductor (L), ESR of C and L, switching frequency (f_{sw}) and so on. After input those specification data, press the "open-loop" button and then the corner frequency (f_o), duty cycle (D) can be calculated and also the bode plot of open loop gain of DC-DC converter will be plotted. After started the open-loop simulation, input other remaining parameters such as the peak of ramp voltage ($\hat{V}_{ramp}$), voltage divider resistance (R_B), crossover frequency (f_c) and also the desired phase margin (PM). Press the "parameters calculate", then the result of the designed parameters (R_2, R_3, C_1, C_2, C_3) of the Type III controller as shown in Fig. 7 will be displayed at the bottom part of the interface. Moreover, the bode plot of the open loop gain obtained through this interface can let the users to verify the design as well.

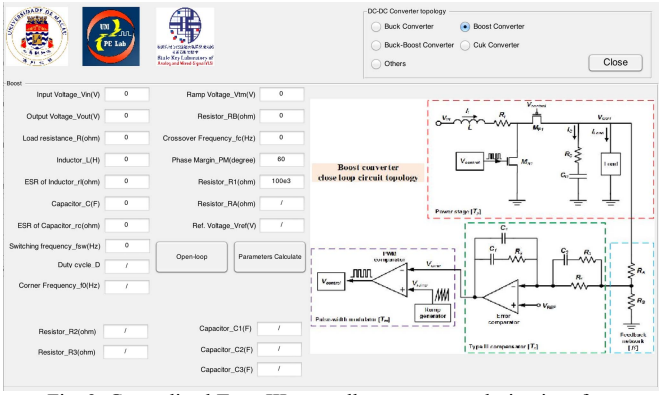

Fig. 9. Generalized Type III controller parameters design interface

IV. Simulation Results

In order to verify the proposed generalized Type III controller parameters design interface for DC-DC converters, conventional DC-DC buck and boost converter circuits are built using 65nm CMOS process in an integrated circuit design tool Cadence respectively. A set of designed parameters for buck and boost converter are summarized in Table III and IV respectively.

TABLE III. Designed Parameters for Buck And Boost Converter

Parameters	Buck Converter	Boost Converter
	Value	Value
Input voltage V_{in}	1.2V	1V
Output voltage V_{out}	0.6V	1.5V
Load resistance R_{load}	10 ohm	
Switching frequency f_{sw}	200MHz	
Switching Period T_s	5ns	
Inductor L / ESR of inductor r_l	15nH / 10mΩ	5nH / 10mΩ
Capacitor C / ESR of capacitor r_c	20nF / 20mΩ	
Peak value of ramp voltage $\hat{V}_{ramp}$	1V	1.2V
Reference voltage V_{ref}	0.5V	0.6V
Testing phase margin (PM)	30°, 45°, 60°, 68°	

From Table III, the component parameters of Type III compensator can be calculated in the following step. By setting the crossover frequency (i.e. fifth of switching frequency), the gain and phase value of the DC-DC converter can be calculated by (7) and (9).Then the required phase boost (φ_m) can be calculated by (10) with the desired PM. After the required gain and the required phase boost $\varphi_m$are calculated, the value of the K factor can be obtained by (6).

In order to verify the effect of load transient response under different phase margin value and the effectiveness of the developed design interface in this paper, Tables V summarizes the designed Type III controller parameters under different PM= 30°, 45°, 60°and 68° respectively.

TABLE V SUMMARIZES THE K-FACTOR AND THE DESIGNED TYPE III CONTROLLER PARAMETERS UNDER TESTING PM FOR BUCK CONVERTER

	Desired Phase Margin(PM)			
	30°	45°	60°	68°
K-Factor	10.89	18.45	36.84	60.01
R1 (kΩ)	100			
R2 (kΩ)	598	440	305	235
R3 (kΩ)	10	5.8	2.8	1.7
C1 (fF)	21	38	80	132
C2 (fF)	2.3	2.3	2.3	2.3
C3 (fF)	120	162	234	662

TABLE IV SUMMARIZES THE K-FACTOR AND THE DESIGNED TYPE III CONTROLLER PARAMETERS UNDER TESTING PM FOR BOOST CONVERTER

	Desired Phase Margin(PM)			
	30°	45°	60°	68°
K-Factor	17.67	34.73	94.28	217.39
R1 (kΩ)	100			
R2 (kΩ)	328	227	135	107
R3 (kΩ)	6.0	3.0	1.1	0.5
C1 (fF)	58	117	323	625
C2 (fF)	3.5	3.5	3.5	2.9
C3 (fF)	178	258	433	662

Figs. 10 – 13 show the DC-DC converter output voltage V_{out} waveforms during load transient I_{Load} (60mA to 120mA) for the conventional DC-DC buck converter. Fig. 10 shows an output voltage waveform with large overshoot, slight oscillation phenomenon and long settling time because of insufficient phase margin (PM=30°); Fig. 11 shows the output voltage at a phase margin of PM=45°during load transient, it has a smaller overshoot and smoother transient response with shorter settling time than PM=30°case. Fig. 13 shows the output voltage at a phase margin of PM=68° during load transient, it has a similar overshoot and settling time as PM=45°case. Fig. 12 shows the output voltage at a phase margin of PM=60° during load transient, it can be clearly shown that it has the smoothest transient response, shortest settling time and similar overshoot among the four cases.

On the other hand, from Table III again, the component parameters of Type III compensator can be calculated. First, the crossover frequency will be set as quarter of the RHPZ in order to fulfill the considerations mentioned before. After setting the crossover frequency, the gain and phase value of the DC-DC converter can be calculated by (7) and (9). With the desired PM, then the required phase boost (φ_m) can be calculated by (10). After the required gain and the required phase boost $\varphi_m$are calculated, the value of the K factor can be obtained by (6).

For verifying the effect of load transient response under different phase margin value and the effectiveness of the developed design interface in this paper, Tables IV summarizes the designed Type III controller parameters under different PM= 30°, 45°, 60°and 68° respectively.

Figs. 14 – 17 show the DC-DC converter output voltage V_{out} waveforms during load transient I_{Load} (150mA to 300mA) for the conventional DC-DC boost converter. Fig. 14 shows an output voltage waveform with large overshoot, slight oscillation phenomenon and long settling time because of insufficient phase margin (PM=30°); Fig. 15 shows the output voltage at a phase margin of PM=45°during load transient, it has a smaller overshoot and smoother transient response with shorter settling time than PM=30°case. Fig. 17 shows the output voltage at a phase margin of PM=68° during load transient, it has a similar overshoot and settling time as PM=45°case. Fig. 16 shows the output voltage at a phase margin of PM=60° during load transient, it can be clearly shown that it has the smallest overshoot, smoothest transient response and shortest settling time among the four cases.

Therefore, Figs. 10 – 17 verified the effectiveness and convenience of the proposed generalized Type III controller parameters design interface for different DC-DC converters in this paper.

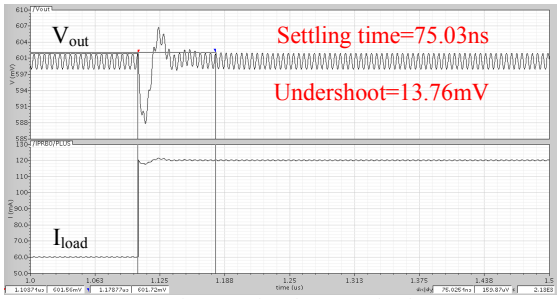

Fig. 10. Step Response of conventional DC-DC buck converter (PM=30°)

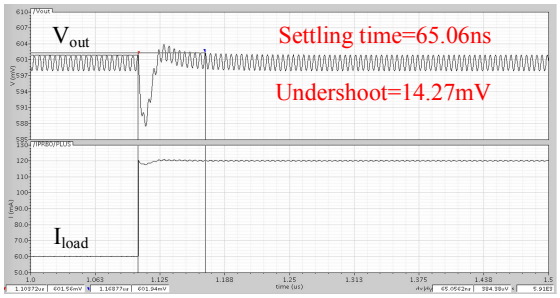

Fig. 11. Step Response of conventional DC-DC buck converter (PM=45°)

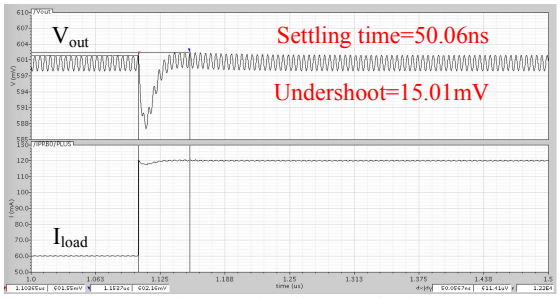

Fig. 12. Step Response of conventional DC-DC buck converter (PM=60°)

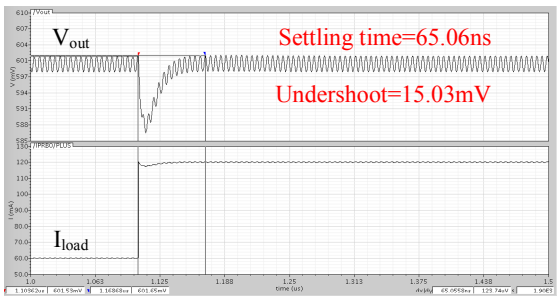

Fig. 13. Step Response of conventional DC-DC buck converter (PM=68°)

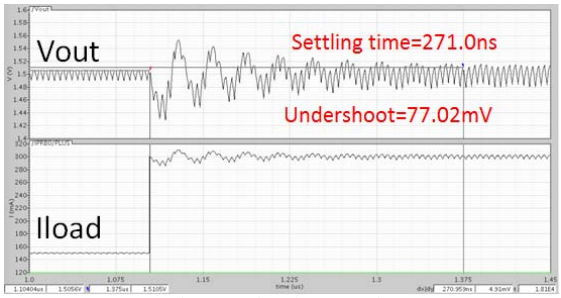

Fig. 14. Step Response of conventional DC-DC boost converter (PM=30°)

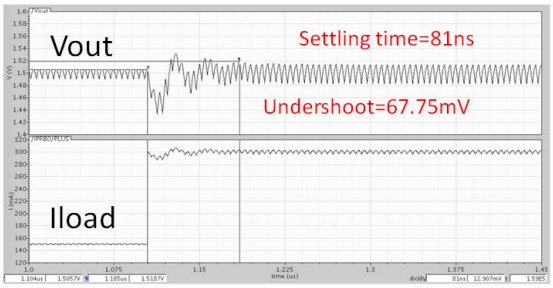

Fig. 15. Step Response of conventional DC-DC boost converter (PM=45°)

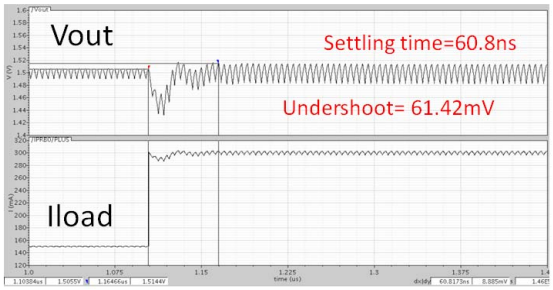

Fig. 16. Step Response of conventional DC-DC boost converter (PM=60°)

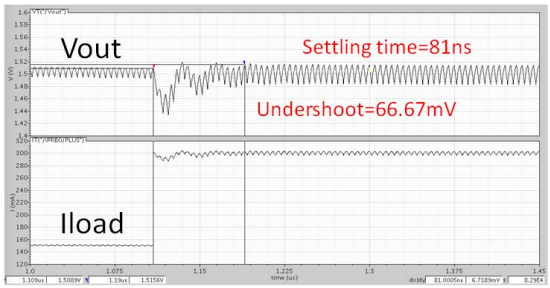

Fig. 17. Step Response of conventional DC-DC boost converter (PM=68°)

V. CONCLUSION

In this paper, the design of the closed-loop Type III controller for DC-DC converters has been presented and discussed. Moreover, a generalized Type III controller parameters design interface for different types DC-DC converters (buck, boost, buck-boost, cuk, etc.) is also constructed in order to calculate the corresponding parameters values (resistors and capacitors) of the Type III compensator in a more convenient and fast way under the design specifications. Then with the help of the design interface, the conventional DC-DC buck and boost converters under different specifications (PM=30°, 45°, 60° and 68°) have been simulated in 65nm CMOS technology, in which the results verified the generalized Type III controller design interface. This interface is also applicable for other DC-DC converters. Moreover, the designed closed-loop Type III controlled DC-DC converter interface can obtain (i) stable, (ii) fast transient response performances and (iii) small steady state error performance for different DC-DC converters.

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