Inter-Stage Gain Error Self-Calibration of a 31.5fJ 10b 470MS/s Pipelined-SAR ADC

Jianyu Zhong, Yan Zhu, Sai-Weng Sin, Seng-Pan U[1], Rui Paulo Martins[2]
State-Key Laboratory of Analog and Mixed Signal VLSI (http://www.fst.umac.mo/en/lab/ans_vlsi/index.html)
Faculty of Science and Technology, University of Macau, Macao, China
E-mail: terryssw@umac.mo
1 - Also with Synopsys - Chipidea Microelectronics (Macau) Limited
2 - On leave from Instituto Superior Técnico/TU of Lisbon, Portuga

***Abstract*—This paper proposes an Inter-Stage Gain Error (ISGE) calibration method devoted to correct the residue gain errors induced by the parasitic effects, non-ideal op-amp gain and capacitor mismatch, and also the mismatches for supply-derived reference voltages between two stages for Pipelined-SAR ADC. The calibration reuses the SAR ADC to estimate the overall inter-stage gain error and compensates it in the 2nd-stage DAC in 2 cycles, and it is implemented in a Pipelined-SAR which achieves 10b 470 MS/s in 65nm CMOS with the FoM of 31.5fJ/conv.-step by consuming only 6% of the total ADC area (0.049mm^2).**

I. Introduction

Many multi-step ADC architectures are sensitive to ISGE which rely on digital calibration to improve the linearity performance [1-4], and Pipelined-SAR ADC has been proven with high power efficiency even at higher operation speed [3-4]. Those designs employ the top-plate sampling technique in both the 1st- and 2nd-stage SAR, which is also commonly used in SAR ADC to achieve high-speed SAR operation with low switching power [5-6], however, the implementation of this technique in the multi-step ADC results in ISGE induced by the top-plate parasitic capacitance. In addition, both designs introduce a split Capacitive DAC (CDAC) structure in the 2nd-stage, which reduces the loading of the op-amp to improve the speed of amplification, and utilize the attenuator to scale down the reference voltage from the supplies, thus avoiding using the reference generator to achieve power saving. However, the mismatch and parasitic of the attenuation capacitor also contribute with ISGE. Therefore, those designs require off-chip ISGE calibration in digital domain to achieve required linearity. The method of digitally-adjusting the feedback factor to compensate ISGE on-chip in pipeline ADC was reported in [2], however, it requires an additional comparator for measuring the gain error, which turns the calibration quite sensitive to the offset errors of the comparator and the op-amp. Moreover, a long calibration period of 56 clock cycles needs to be consumed to correct the gain error of one MDAC stage.

This research work was financially supported by Research Grants of the University of Macau and the Macao Science & Technology Development Fund (FDCT).

This paper proposes an ISGE calibration to improve the conversion linearity of the multi-step ADC architecture. The method is implemented in a PI Pipelined-SAR ADC, which utilizes the 2nd-stage SAR to measure ISGE, and corrects it by adjusting the gain ratio of the CDAC. Moreover, the scheme cancels the offset errors of both the op-amp and the comparator digitally during the gain measurement, thus making the calibration insensitive to offset errors. The scheme uses simple digital circuitry to calibrate the inter-stage gain errors in each channel by only 2 conversion cycles. The experimental results of a pipeline SAR ADC prototype in 65nm CMOS demonstrate the effectiveness of the calibration that achieves a SNDR of 55.71dB and a low figure-of-merit (FoM) of 31.5fJ/conv.-step.

II. ISGE Calibration Technique

A. Conversion nonlinearity from ISGE

Fig. 1 shows a (i+j)-bit two-step SAR ADC with the proposed ISGE calibration and its timing diagram. The ADC architecture is composed of a i-bit SAR ADC in 1st-stage and a j-bit one in 2nd-stage, the op-amp located between two stages is used for the residue amplification. The input signal is sampled at the top-plate of the 1st-stage CDAC. Then, after the coarse i-bit conversion, the 1st-stage residue $V_{out,1}$ at the top plate of the DAC can be calculated as

$$V_{out,1} = V_{in} - (\sum_{n=0}^{i-1} S_{n,1} C_n) \times \frac{V_{ref1}}{C_{sum1} + C_{P1}} , \quad (1)$$

where C_{sum1} is the total sampling capacitance of the 1st-stage CDAC, $S_{n,1}$ ($S_{n,1} \in \{0,1\}$) is n-th bit decision, C_{P1} is the top-plate parasitic of the 1st-stage CDAC. It can be observed that C_{P1} in the denominator reduces the SNR and contributes with a gain error γ_1 ($\gamma_1 = C_{sum1}/(C_{sum1} + C_{P1})$) of the reference voltage.

When the amplification phase Φ_{RA} is enabled, the 1st-stage CDAC feeds back C_{fb} to the op-amp's output to obtain $A_V \times V_{out,1}$ amplification. The closed loop gain is determined by the open loop gain and the feedback factor. Owing to the fact that top-plate parasitics of both stages contribute with the major part of ISGE, here for simplicity, let us assume that the open loop gain of the op-amp is sufficiently large

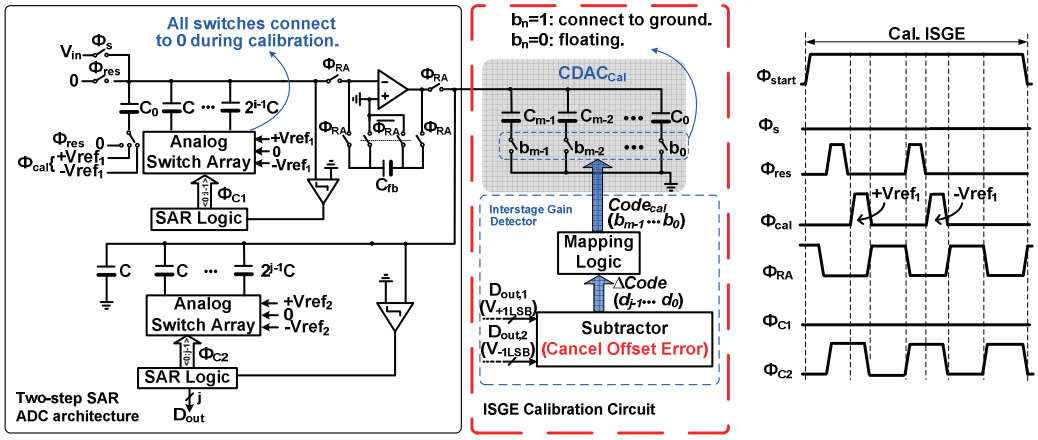


Fig. 1 Two-step SAR ADC with the ISGE calibration and timing diagram.

and the gain error caused by the inherent capacitor mismatch of C_{sum1} and C_{fb} is not considered in the following analysis, although they will be calibrated inherently during the calibration process. Thus, after the 2nd-stage fine 5b conversion, the output voltage $V_{out,2}$ of the DAC can be deduced as

$$V_{out,2} = A_V \times V_{out,1} - (\sum_{n=0}^{j-1} S_{n,2} C_n) \times \frac{V_{ref2}}{C_{sum2} + C_{P2}}, \quad (2)$$

where C_{sum2} is the total capacitance of 2nd-stage CDAC, and C_{P2} is the top-plate parasitic of 2nd-stage CDAC. Similar to the effect of C_{P1} in the 1st-stage, C_{P2} in the denominator is uncorrelated with the bit decision and only causes a reference gain error γ_2 ($\gamma_2 = C_{sum2}/(C_{sum2}+C_{P2})$) in the 2nd-stage conversion.

The reference mismatch between two stages causes a conversion nonlinearity that happens periodically at the carry from $\underbrace{0\cdots0}_{i}\underbrace{1\cdots1}_{j}$ to $\underbrace{0\cdots01}_{i}\underbrace{0\cdots0}_{j}$, which can be seen from the input-output characteristic of Fig.2.

B. ISGE calibration technique

Based on the above discussion, the parasitic effect of C_{P1} and C_{P2} can be equivalent to an inter-stage gain error α ($\alpha=\gamma_1/\gamma_2$), which directly reflects the reference mismatch error between two stages. Ideally, α=1, indicates that the references of both stages are scaled-down by the same ratio. While α>1 or α<1 means that the scaling-down ratio is unbalanced. To implement a monotonic calibration scheme, α is initially set to >1, which means the scaling factor of 2nd-stage $V_{ref\text{-}2nd}$ is smaller than the one of the 1st-stage. This is implemented by enlarging the reference voltage of 2nd-stage. To adjust α back to 1, the additional calibration capacitive array ($CDAC_{Cal}$) is added onto the top-plate of 2nd-CDAC and enabled or disabled partially according to the desired gain ratio.

As seen from Fig. 1, the calibration circuit is composed of a calibration capacitive array and an ISGE detector including the subtractor and the mapping logic. When the start phase Φ_{start} is enabled, the $CDAC_{Cal}$ and the top plate of 1st-stage CDAC are reset to *Gnd* in the phase Φ_{res}. When the gain measurement phase Φ_{cal} is enabled, one unit capacitor C_0 (C_0=C) is switched to *+Vref* to generate a reference voltage of +1LSB (V_{+1LSB}) at the top plate of 1st-stage. Then the signal V_{+1LSB} is amplified by A_V and passed to the next stage DAC. The 2nd-stage SAR quantizes the $A_V \times V_{+1LSB}$ to *j*-bit digital code which is stored in a bit register for calibration processing. Then, after the next reset phase, a V_{-1LSB} is generated by switching C_0 to *–Vref* and the above operation repeats once until the second *j*-bit code ($D_{out,2}$) is acquired. The offset is cancelled by subtracting two output codes ($D_{out,1}$ and $D_{out,2}$) and the subtraction result ΔCode will enter the mapping logic to feed back the corresponding control logic to $CDAC_{Cal}$. The mapping logic contains several cases to compensate different α according to the measured *ΔCode* as shown in Fig.2. The number of calibration cases is determined by process variation, and the step resolution in each calibration case is determined by the ADC accuracy requirement, which will be analyzed next.

III. Implementation Method

The proposed ISGE calibration technique is implemented on a 10-bit 470MS/s PI Pipelined-SAR architecture in 65nm CMOS technology. As shown in Fig.3, the ADC consists of a front-end shared 6bit 2b/cycle SAR, 2×TI Residue Amplification CDACs (RAC), a residue amplifier and 2×TI 5b SAR ADCs. Two stages have one bit overlapping for digital error correction. The additional bit performed by the 2nd-stage SAR is used for offset and gain calibrations.

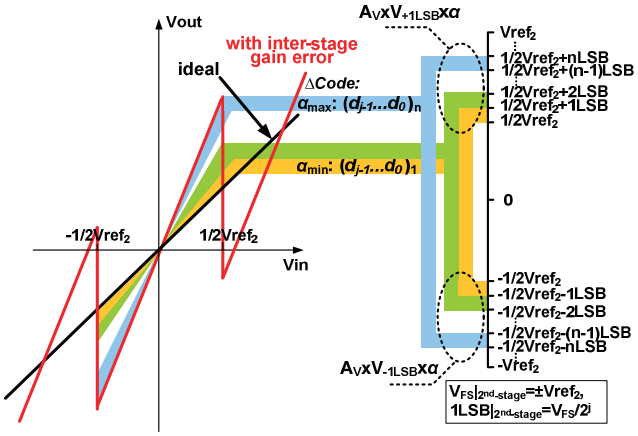


Fig.2 Input-output characteristic w/ ISGE and the digital measurement of α.

During the sampling phase Φ_s, the input signal is sampled at the top-plate of the 1st-stage 6b DAC and RAC_1. In the conversion phase Φ_1, the 1st-stage SAR solves the coarse 6b, and when the conversion is completed, RAC_1 disconnects from the 6b SAR and connects to the input of the op-amp to perform the 4×residue amplification. Meanwhile the 6b SAR connects to RAC_2 to start a new conversion. In the subsequent pipelined phase Φ_2, the 2nd-stage determines the remaining fine 5b code that is passed to the digital error correction logic for the final 10b output. In this architecture, two stages sample the signal at the top-plate of the DAC, which implies that the conversion is quite sensitive to the parasitic capacitance. Moreover, the attenuation solution used in 2nd-stage also introduces ISGE due to the mismatch and parasitic of the attenuator. Thus the ISGE can be calculated as,

$$\alpha = \frac{C_{sum1}\cdot[C_a(C_{sub,2}+C_{P,B}+C_{vd}+C_{P,C})+(C_{sub,2}+C_{P,C})(C_{vd}+C_{P,B})]}{(C_{sum1}+C_{P,A})\cdot[C_a(C_{sub,2}+C_{vd})+C_{sub,2}C_{vd}]}, \quad (3)$$

where C_{sum1} is the total sampling capacitance including 1st-stage CDAC and RAC, $C_{sub,2}$ is the total capacitance of sub-array in the split-CDAC, $C_{P,A}$, $C_{P,B}$ and $C_{P,C}$ are the top-plate parasitic capacitance from 1st-stage CDAC and both sides of the 2nd-stage split-CDAC respectively. After the layout routing α is approximated to 1.127, considering the mismatches of C_a and process variation, the calibration range covers the variation of α from α_{min}=1.05 to α_{max}=1.25.

The calibration is implemented in the time-interleaving fashion without changing the ADC control logic. To ensure α>1, the $V_{ref\text{-}2nd}$ is scaled up initially by enlarging C_a from 2.13C to 2.46C and reducing C_{vd} from 30C to 29C. The 1st-stage CDAC is used to generate $V_{\pm 1LSB}$ for ISGE measurement and the 2nd-stage SAR ADC is used to quantize ISGE, the mapping logic determines the corresponding calibration code based on the subtraction result ΔCode, and feeds it back to control $CDAC_{cal}$. Note that the offsets of the op-amp and the 2nd-stage comparator need to be suppressed within $1/4V_{ref\text{-}2nd}$, otherwise the 2nd-stage comparison will saturate its full scale.

Obviously, the estimation accuracy of α is directly related with the resolution of 2nd-stage SAR. Assuming that the estimated value with error is $\alpha(1\pm\varepsilon_\alpha)$, then enlarging $V_{ref\text{-}2nd}$ by $\alpha(1\pm\varepsilon_\alpha)$ results in the ISGE of $1\cdot(1\pm\varepsilon_\alpha)$ after calibration. Since the peak-to-peak residue swing in 2nd-stage is $\pm 1/32V_{ref}$, and considering 1b overlap for digital error correction, it requires the $V_{ref\text{-}2nd}$ equal to $\pm 1/16V_{ref}$, and the 2nd-stage SAR resolves 5-bit within $V_{ref\text{-}2nd}$, leading to $0.5LSB_{2nd}=1/2^9 Vref$. So the tolerable error ε_α can be derived as,

$$\frac{1}{8}\cdot V_{ref}\cdot\varepsilon_\alpha < \frac{V_{ref}}{2^9} \Rightarrow \varepsilon_\alpha < 1.563\% . \quad (4)$$

This determines the resolution of 2nd-stage DAC for ISGE estimation,

$$\frac{V_{ref}}{2^{N+1}} < V_{ref}\times\alpha_{min}\times 1.563\% \Rightarrow N > 4.79 . \quad (5)$$

Thus the 5-bit split-CDAC can satisfy the accuracy requirement. In addition, since $\Delta Code$ is acquired from the subtraction of the two digital codes, the split DAC with 1 more bit resolution is needed. In the calibration range from 1.05 to 1.25, there are totally 6 calibration logics which are pre-set in the mapping logic to control $CDAC_{Cal}$.

Meanwhile, the step size of $CDAC_{Cal}$ is also determined by the calibration accuracy. Their relationship can be expressed as,

$$\Delta C_{cal} = (\pm 1.563\%)\times\frac{C_a(C_{sub,2nd}+C_{vd})+C_{sub,2nd}C_{vd}}{C_a+C_{sub,2nd}} = \pm 0.5C \quad (6)$$

Thus, disconnecting 1C of $CDAC_{Cal}$ from *Gnd* enlarges $V_{ref\text{-}2nd}$ by around 3.125%. The structure of $CDAC_{Cal}$ is designed as shown in Fig.3. It is a binary-weighted capacitor array with the custom designed unit capacitor (2μm×2.4μm equivalent to 5.5fF), which is identical to the unit capacitor of both stages, thus the calibration is immune to the capacitance process corners. In the case of α_{min}=1.05, the capacitance to be removed from $CDAC_{Cal}$ after calibration is 4C, while the one in the case of α_{max}=1.25 is 9C.

To ensure the calibration accuracy, the capacitor mismatch in $CDAC_{cal}$ should be less than 6% based on the Matlab Monte-Carlo simulations. By careful layout less than 1% capacitor mismatch is easily achieved, thus ensuring the

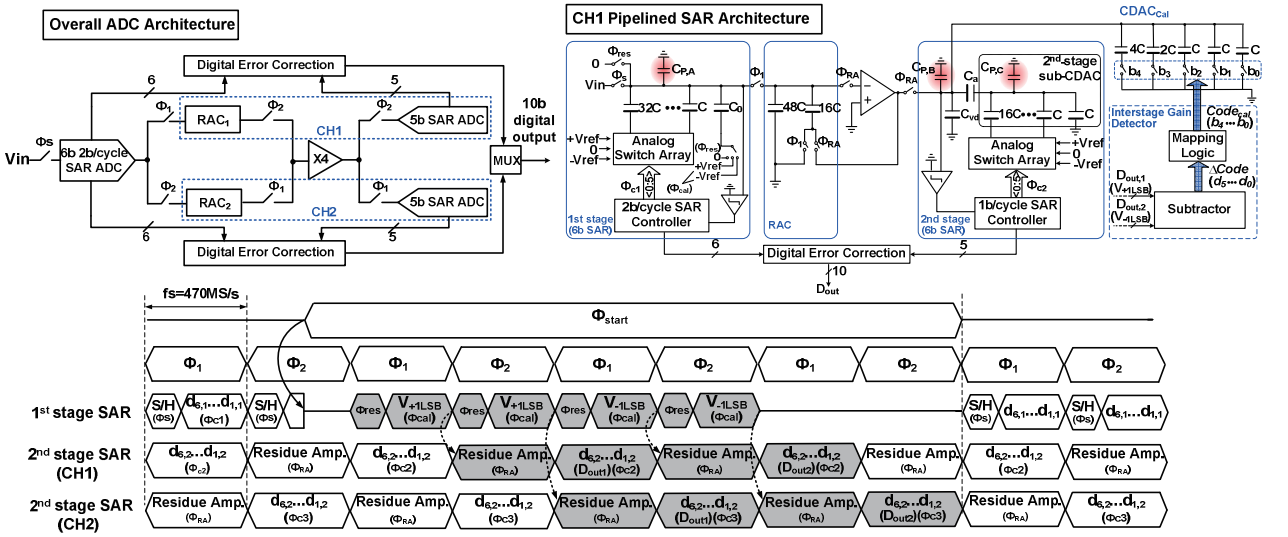


Fig. 3 PI Pipelined SAR ADC with the implementation of the ISGE calibration and timing diagram.

calibration accuracy. In addition, the switches in $CDAC_{Cal}$ may also affect the calibration accuracy, because the "floating" capacitor cannot be treated as "non-existent" since the gate-source parasitic capacitance C_{gs} is still connected to the capacitor in series when the switch is off. As a result, a minimum-size switch is used to reduce C_{gs} to about 0.1fF, which can be tolerated to ensure the calibration accuracy.

The accuracy of $\pm$1LSB residue generated for ISGE estimation is also of concern. The capacitor mismatch of the 1st-stage CDAC is 10b based on the ADC resolution requirement. The calibration precision can be guaranteed as long as the capacitor mismatch accuracy can satisfy the ADC's overall requirement.

IV. Measurement Results

The PI pipeline-SAR with the proposed ISGE calibration technique has been fabricated in 1P7M 65nm CMOS with low-V_T option. The chip micrograph is illustrated in Fig.4. The active area is 0.049mm^2 with the calibration circuit occupying only 6% of the total area. Fig.5 shows the SNDR histogram of 20 measured chips. Compared to the work [3] which used the off-chip code histogram statistic to calibrate ISGE, the proposed calibration can effectively improve the SNDR to a similar value. This is because the main limitation of the ADC is from the noise instead of ISGE. A chip with peak SNDR has been selected to be measured and it exhibits the following results. Fig.6 shows the static performances with calibration, where the DNL/INL is 0.475/0.782LSB, and Fig.7 exhibits the ADC's dynamic performance, which achieves a SNDR of 55.71dB with a 1.2MHz input and 54.76dB at Nyquist frequency. Fig.8 shows both the measured FFT @DC and near Nyquist input. Table I summarizes the overall measured performance and also the benchmark with state-of-the-art ADCs.

V. Conclusions

A robust digital foreground inter-stage gain error self-calibrating scheme implemented in a two-channel Pipelined SAR ADC has been presented in this paper. This technique achieves on-chip self-calibration, it is offset-insensitive, and allows fast detection and accurate correction. The measurement results demonstrate the effectiveness of this gain error calibration technique which improves SNDR and FoM.

Acknowledgment

The authors would like to thank Hou-Lou Choi (Justin) for the measurement support.

References

[1] Shin, M.-S., Kwon, O.-K., "14-bit two-step successive approximation ADC with calibration circuit for high-resolution CMOS imagers," in *Electronics Letters*, vol.47, no.14, pp.790-791, Jul. 2011.

[2] Hung-Wei Chen, Wei-Ting Shen, Wei-Chih Cheng; et al., "A 10b 320MS/s self-calibrated pipeline ADC," in *Proceedings of IEEE A-SSCC*, pp.1-4, 8-10, Nov. 2010.

[3] Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, et al., "A 34fJ 500 MS/s Partial-Interleaving Pipelined SAR ADC," to appear soon in *VLSI Dig. Tech. Papers,* Jun. 2012.

[4] Verbruggen, B., Iriguchi, M., Craninckx, J. , "A 1.7mW 11b 250MS/s 2× interleaved fully dynamic pipelined SAR ADC in 40nm digital CMOS," in *ISSCC Dig. Tech. Papers*, pp.466-468, Feb. 2012.

[5] Liu, Chun-Cheng, Chang, Soon-Jyh, Huang, Guan-Ying, et al., "A 0.92mW 10-bit 50-MS/s SAR ADC in 0.13µm CMOS process," in *VLSI Dig. Tech. Papers,* pp.236-237, Jun. 2009.

[6] Ginsburg, B.P., Chandrakasan, A.P., "Highly Interleaved 5-bit, 250-MSample/s, 1.2-mW ADC With Redundant Channels in 65-nm CMOS," in *IEEE JSSC*, vol.43, no.12, pp.2641-2650, Dec. 2008.

[7] J. Mulder, et al.,"An 800MS/s Dual-Residue Pipeline ADC in 40nm CMOS," in *ISSCC Dig. Tech. Papers*, pp. 184-185, Feb. 2011.

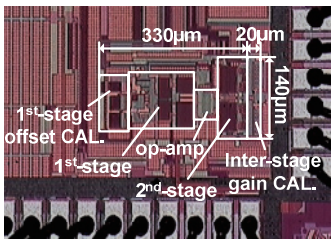


Fig.4 Chip photograph.

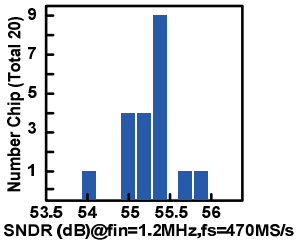
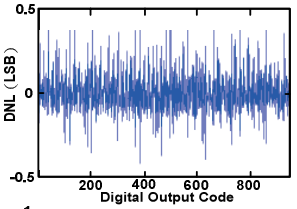
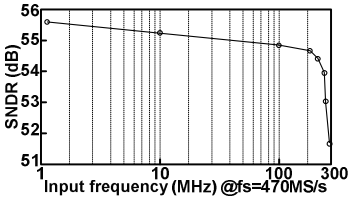
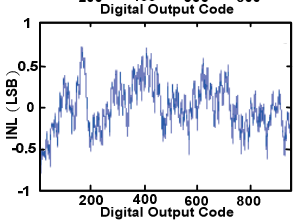


Fig.5 Measured SNDR Histogram.







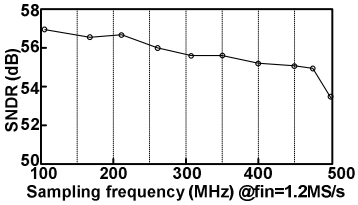


Fig.6 Measured DNL and INL. Fig.7 Measured Dynamic Performances.

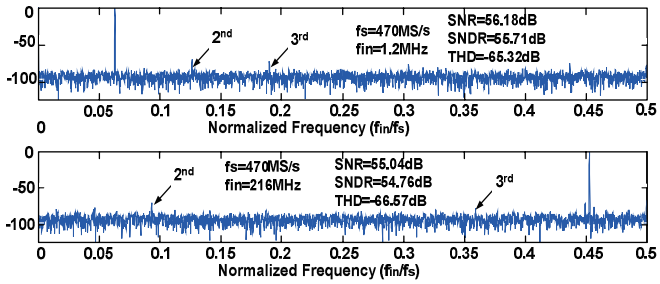


Fig.8 FFT spectrum with 1.2- and 216- MHz inputs (decimated by 25).

TABLE I. Performance Summary and Benchmark

	[2] ASSCC' 10	[3] VLSI' 12	[4] ISSCC' 12	[7] ISSCC' 11	This Work
Architecture	Pipeline	Pipeline-SAR	Pipeline-SAR	Pipeline	Pipeline-SAR
Technology (nm)	90	65	40	40	65
Resolution (bit)	10	10	11	12	10
Sampling Rate (MS/s)	320	500	250	800	470
Supply Voltage (V)	N/A	1.2	1.1	1/2.5	1.2
Area (mm^2)	0.21	0.046	0.066	0.88	0.049
Power (mW)	42	8.2	1.7	105	7.4 (Cal. Power included)
DNL/INL (LSB)	0.7/0.9	0.48/1.1	0.8/1.5	0.4/2.1	0.47/0.78
SNDR (dB)	54.2	55.4	58.7	59	55.7
FoM =Power/(2$^{ENOB@DC}$fs) (fJ/conv.-step)	313	34	10	180	31.5
Gain Calibration	Onchip	Offchip	Offchip	Onchip	Onchip