# MODELING OF NOISE SOURCES IN REFERENCE VOLTAGE GENERATOR FOR VERY-HIGH-SPEED PIPELINED ADC

Weng-Ieng Mok [1], Pui-In Mak, Seng-Pan U [1] and R.P. Martins [2]

Analog and Mixed-Signal VLSI Laboratory, FST, University of Macau, Macao, China (E-mail: benspu@umac.mo)
1 – Also with Chipidea Microelectronics (Macao) Ltd., 2 – On leave from Instituto Superior Técnico, Lisbon, Portual

***Abstract*-In very high-speed pipelined analog-to-digital converters (ADC's), stabilizing the reference voltage with large off-chip capacitor is no longer appropriate, as such capacitor will resonate with the effective inductance of the bondwire. However, creating a stable and high-speed reference internally not only consumes a lot of power and area, but also makes the reference highly sensitive to internal noises. This paper presents the process of analytical modeling and the characterization of the significant noise sources, which comprisse: 1) Sample-variant error voltage due to dynamic loading fluctuations, 2) Static offset voltage due to finite precision of bandgap reference, mismatches in resistor ladder and driving buffer, 3) Random noise modulation. The resulting effects are discussed in terms of the key parameters, ENOB and SFDR. The effectiveness of the modeling methods and deduced equations are also verified either by behavioral or circuit simulations which are particularly helpful in the determination of circuit-level specifications and in compromising different design trade-offs.**

## I. INTRODUCTION

High-speed and medium-resolution pipelined A/D converters (ADC's) are usually applied in modern communication systems such as high IF-sampling receivers, digital-IF multi-standard broadcast TV receivers, and electronics equipments like RGB flat panel displayers [1]-[4], with current sampling rates in the range of 120 - 220 MHz. To achieve such stringent speed requirements and to determine rapidly the circuit-level specifications in the design process, a complete systematic modeling, providing enough degree of extraction of systems' performance, is undoubtedly mandatory. Previously, comprehensive modeling methods of pipelined ADC non-idealities have been well established, focusing, namely in, the op-amp finite gain, the gain-bandwidth product (GBW), the slew-rate limitation, components mismatch and clock-jitter noise, etc. [5]-[6]. And several background calibration methods for those errors have also been proposed [7]-[9]. However, the causes and effects of unsteady reference voltage generator are still lacking in-depth investigation, since its influence is traditionally insignificant when the sampling rate is low, and such reference can be effectively stabilized by using a large off-chip capacitor [10]. Unfortunately, when the sampling rate is raised to higher values, the resonant problem results from the bondwire inductance (in the package) and such capacitor will highly degrade the effectiveness of such approach. Moreover, since such noise is input dependent, it would be difficult to correct or calibrate it off-chip. Then, purely on-chip stabilization is therefore mandatory, although that is power and area hungry, as well as sensitive to internal noise sources.

This paper provides an analysis of those aspects and proposes their effective modeling in order to characterize those internal noise sources and their resulting impacts

In Section II, the stability of the reference voltage with and without off-chip stabilization capacitor is presented. The internal noise sources that include constant dc offset induced error in the A/D conversion curve, and random noise impact on ENOB and SFDR performances are addressed in Section III and Section IV, respectively. The conclusions are drawn in Section V.

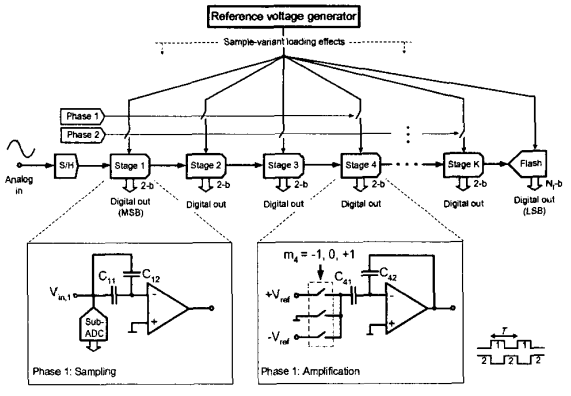


Fig. 1. A generic 1.5-bit/stage pipelined ADC.

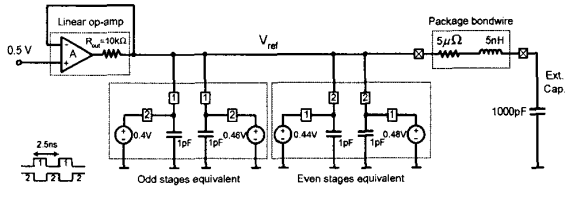


Fig. 2. Equivalent model of $V_{REF}$ generator with and without off-chip stabilization capacitor.

## II. SAMPLE-VARIANT ERROR VOLTAGE IN $V_{REF}$

The origin of sample-variant error voltage in reference voltage $V_{ref}$ is the dynamic loading effects in the two-phase operation of pipelined ADC, which is described in Fig. 1, based on a 1.5-bit/stage pipelined ADC.

In every amplification phases, sampling capacitor requires either $-V_{ref}$, $0$ or $+V_{ref}$ value to control the current stage output signal within the next stage input swing, so as to accomplish the stage-to-stage pipelining digitization. Thus, the loading of $V_{ref}$ driving buffer exhibits a sample-variant fluctuation that implies the lost of its original precision. This effect can be classified as a signal-dependent modulation and results in distortion.

To give an in-sight to the reference fluctuation, an equivalent model of this scenario is proposed in Fig. 2. The highly capacitive loading of the driving buffer's from odd and even stages are considered as two sets of capacitor pairs. Each of the four capacitors is pre-charged with distinct voltage levels, which emulates the previous phase stored charges. For the buffer, the op-amp is modeled as a single-pole system (60-dB DC gain and 1-Grad/s GBW) and the operation is driven by two non-overlap clock phases 1 and 2.

0-7803-8346-X/04/$20.00 

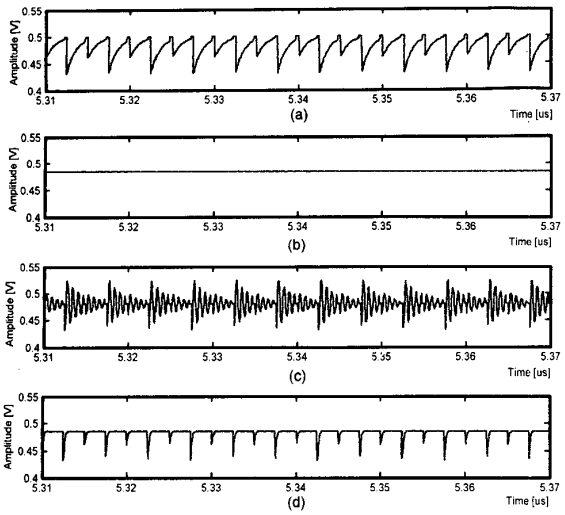


Fig. 3. $V_{ref}$ fluctuation in four cases. (a) With no stabilization capacitor. (b) With 1000-pF stabilization capacitor on-chip. (c) Off-chip implementation of case (b). (c) With added 100-Ω resistor.

Firstly, consider an example based on such model without the bondwire and external capacitor. At phase 1, the odd stage capacitors are charged with 0.4 V and 0.46 V while the even stages one are connected to $V_{ref}$. At phase 2, the operations are reversed with different pre-charged voltages. The operation frequency of the system is assumed to be 200 MHz. The resulted $V_{ref}$ is plotted in Fig. 3(a), which is designed as 0.5 V originally. The initial voltage drop of $V_{ref}$, when the amplification switches are turned on is the average value of the pre-charged voltages. Afterwards, the buffer provides current to compensate such charge loss in the first-order settling. Undoubtedly, the precision is highly degraded due to incomplete settling.

To overcome such initial voltage drop, a relatively large capacitor can be exploited. For instance, by adding a 1000-pF capacitor at the buffer's output, which will be in parallel with the sampling capacitors, a highly stabilized $V_{ref}$ is obtained. Since the behavior of a two non-overlap-phase switching capacitor banks is equivalent to a resistor in high sampling frequency, the stabilized reference voltage is slightly smaller than the generated $V_{ref}$ as shown in Fig. 3(b).

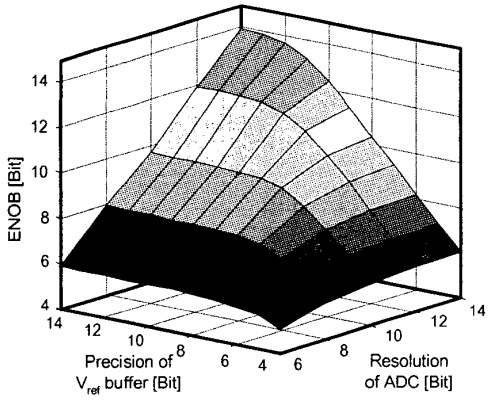


Fig. 4. Influence of reference voltage buffer precision on ENOB for different ADC resolution.

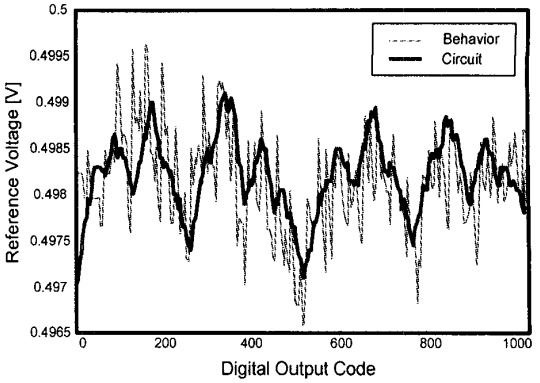


Fig. 5. Reference voltages obtained through behavioral model and schematic simulations.

Nevertheless, such large capacitor occupies a huge chip area, which is only tolerable with an off-chip approach. However, in this case, the inductance of the bond-wire (assuming a typical value of L=5nH) will resonate with such capacitor, as shown in Fig. 3(c). The straight way to damp such oscillation is by adding a resistor $R$ (e.g., 100 Ω) in series with such capacitor, which can decay the amplitude exponentially [Fig. 3(d)]. This will be an effective way to solve the resonance, but not the initial voltage drop.

The above model is rough but simple. To obtain a more accurate result, a mathematical model based on simulation is mandatory since the pre-charged voltage in the sampling capacitor is sample-variant.

The modeling approach can be described as follows: Denote $m_k(nT_s/2)$ as outputs from sub-ADC at stage $k$ in each half sampling period which equals either -1, 0 or +1. The equivalent capacitive loading in each half sampling period is given by,

$$C_{eq}(nT_s/2)=\begin{cases}\sum_{j=1}^{\lceil (N-N_f)/2\rceil}\left(C_{s,2j-1}\cdot\left|m_{2j-1}(nT_s/2)\right|\right) & \text{for } n=1,3,5...\\ \sum_{j=1}^{\lfloor (N-N_f)/2\rfloor}\left(C_{s,2j}\cdot\left|m_{2j}(nT_s/2)\right|\right) & \text{for } n=2,4,6...\end{cases} \quad (1)$$

where, $C_{s,k}$ is the sampling capacitor at stage $k$. $N$ and $N_f$ are the resolution of the entire ADC and the last stage sub-ADC, respectively.

Due to the finite recovery speed of the driving buffer, the initial voltage drop limits the precision of $V_{ref}$ reached at every half-clock period. Moreover, the reference voltage is also affected by input-dependent variations caused by sample-variant capacitive loading. The non-ideal reference voltage, $V_{ref}(nT_s/2)$, reached at the end of each amplification phase can be expressed as,

$$V_{ref}=\left(V_{ref,ideal}-V_{drop}\right)+V_{drop}\cdot\left(1-e^{-t/\tau}\right) \quad (2)$$

where

$$\tau=\frac{1}{2\pi\cdot\beta\cdot GBW} \quad (3)$$

$V_{ref,ideal}$ is the ideal value of reference voltage, $V_{drop}$ is the voltage drop caused by the sample-variant equivalent capacitive loading $C_{eq}(nT_s/2)$ given by (1), $\beta$ is the feedback factor and $GBW$ is the gain-bandwidth product of the buffer.

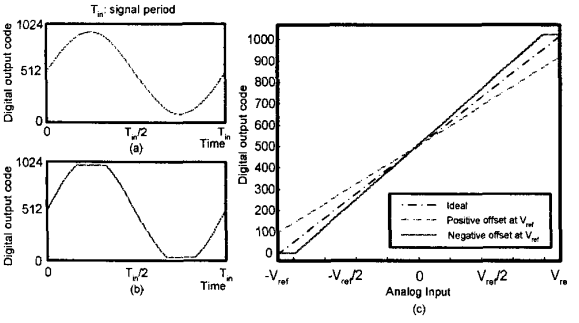


Fig. 6. Time domain of (a) Positive offset. (b) Negative offset. (c) Their corresponding A/D conversion curves.

Founded by (1)-(3), the effective number of bits (ENOB) of the entire converter, in terms of the precision of driving buffer and the entire ADC resolution, is plotted in Fig. 4. It shows that the appropriate precision of the reference voltage is 1 bit less than the required resolution of the ADC, precision higher than that is generally exhausted.

Such model is verified by comparing the behavioral simulations obtained in Matlab™ with the one obtained through circuit simulation in Cadence™. The assumptions include 200-MHz sampling rate, 0.5-V reference voltage and 10-bit resolution with 1.5-bit/stage.

With a ramp signal as the analog input, the reference voltage reached at $nT_s/2$ is plotted in Fig. 5. Such results follow our expectation by assuming that it is a single-pole system with small-signal settling (i.e. the slewing of the op-amp is ignored). As it can be observed that even the accuracy of the model is not high, the tendency is well predicted. Such tendency helps to characterize the magnitude of the distortion components, which is very imperative since it is input-dependent and dynamic in nature.

## III. Constant Offset Voltage in $V_{REF}$

$V_{ref}$ is an imperative parameter to define both the input and output full-scale range, and thus any offset voltages will undoubtedly limit the full-scale (FS) signal that could be applied to the converter. Generally, offset voltage in each sub-ADC is random in polarity, either positive or negative, which frequently exists due to unavoidable components mismatch. Resistor ladder division is the simplest and widely used approach to implement the reference voltage. Thus the offset is mainly caused by resistor mismatch, buffer offset voltage and finite precision of the bandgap reference. However, such kind of error can be considered as a static error and their resulting impacts are illustrated on the A/D conversion curve (10-bit is assumed) Fig. 6(a)-(c). There are two situations of

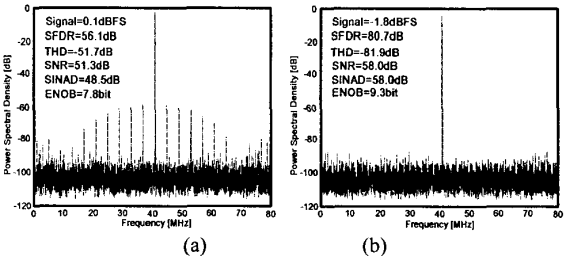


Fig. 7. (a) Influence of offset voltages to the SFDR and ENOB performance of the entire ADC. (a) Negative. (b) Positive.

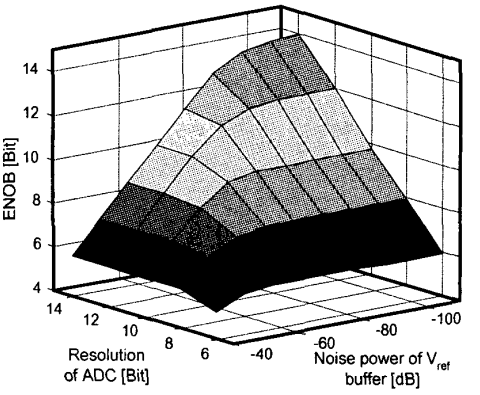


Fig. 8. Influence of reference voltage noise on ENOB for different ADC resolution.

dc offset-induced errors in the reference voltage. On one hand there is the negative offset that reduces the conversion range and leads to saturation in the output, when the input signal amplitude is larger than the current reference voltage as shown in Fig. 7(a). On the other hand, the positive offset that enlarges the conversion range and consequently degrades the signal-to-noise ratio (SNR) as shown in Fig. 7(b). Calibration of such static offset error is possible and should be adopted to minimize the noteworthy influence of this non-ideality.

## IV. Random Noise on $V_{REF}$

Random noise is indubitably the underlying limitation of high-resolution and high-performance pipelined ADC. The existence of random noise on the reference voltage results in a thorough trade-off between resolution and power dissipation. Moreover, noise also limits the minimum signal level that a circuit can process with satisfactory performance. In other words, it bounds the minimum supply voltage and the signal swing to maintain a sufficient SNR for the desired resolution.

Noise that exists in the reference voltage is directly added to the sampled-values when the output of the reference buffer connects to the sampling capacitors during the amplification phase. In order to describe the nature of this effect, the relationship between sampled-input, analog output and non-ideal $V_{ref}$ is derived as follows:

Assuming that $V_{in,k}$ is the input of the $k^{th}$ stage, its corresponding analog output from the multiplying digital-to-analog converter (MDAC) can be expressed as:

$$V_{out,k} = (2^{N_{eff}}) \cdot V_{in,k} - \left[ \sum_{d=1}^{2^{N_{eff}}-1} (m_k(d)) \right] \cdot V_{ref} \tag{4}$$

where $N_{eff}$ is the effective resolution at each stage and $m_k(d)$ is the $d^{th}$ output from $k^{th}$ stage sub-ADC. Considering there are two cases, when random noise exists in $V_{ref}$ and in input signal with variance $\sigma_{ref}^2$ and $\sigma_{in}^2$, respectively. Equation (4) can be re-expressed into,

$$V_{out\_ref,k} = V_{out,k} + \left[ \sum_{d=1}^{2^{N_{eff}}-1} (m_k(d)) \right] \cdot \sigma_{ref} \tag{5a}$$

$$V_{out\_in,k} = V_{out,k} + \left(2^{N_{eff}}\right) \cdot \sigma_{in} \tag{5b}$$

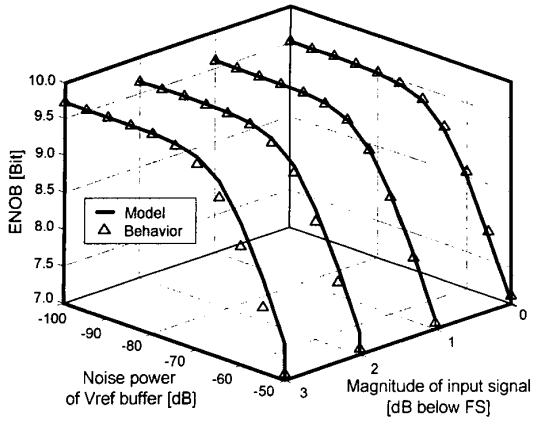


Fig. 9. ENOB as a function of noise power and input magnitude. (10-bit resolution and 0.5-V reference voltage are assumed.)

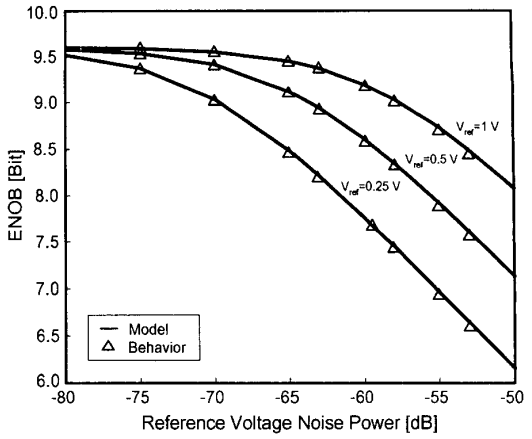


Fig. 10. ENOB as a function of noise power and its input-referred noise. (-1-dBFS input and 10-bit resolution are assumed).

From (5a)-(5b), it is worth to mention that such noise source will not affect the conversion range when the sampling capacitors are connected to signal ground (i.e., $m_k(d) = 0$). Different from reference voltage noise, input noise affects the whole conversion range. However, under consideration of applying a full-scale ramp input signal, the noise in $V_{ref}$ can be quantified and approximated as input referred noise,

$$\sigma_{in\_ref,k} = \left(\sigma_{ref,k}\right) \cdot \frac{\sum_{d=1}^{2^{N_{eff}}-1}\left(1-\frac{d}{2^{N_{eff}+1}}\right)}{2^{N_{eff}}} \qquad (6)$$

The impact to the entire 1.5-bit/stage pipeline ADC performance, of random noise existence in the 0.5 V-Reference Voltage, can be analyzed in Fig. 8 which is based on the proposed model. Focusing on 10-bit resolution, the degrading of ENOB as a function of reference voltage noise is shown in Fig. 9 through behavioral and circuit simulations. Both curves show good agreement to each other. Such figures show the impact of noise existence in $V_{ref}$ is somehow related to input amplitude as mentioned previously, and thus there must be an optimized value for such approximation. It is observed that (6) is an excellent approximation when the input signal is 1 dB below the full-scale. Fig.10 further approves the proposed approximation approach for different value of $V_{ref}$. It is noticed that when the $V_{ref}$ is relatively small, a small increment in the noise power would result in a significant loss in the ENOB. This proved that the noise exists in $V_{ref}$ reduces the headroom to achieve high-speed low-voltage operation at the same time.

## V. CONCLUSIONS

An exhaustive analysis of performance degradation due to unstable reference voltage of very-high-speed pipelined ADC was presented. The significant noise sources in the reference voltage generator, which cannot be simply eliminated through digital error correction logic, include input-dependent error voltage, offsets and random noise. Their impacts can be summarized as follows:

1) Input-dependent and sample-variant error voltage, caused by dynamic loading on the driving buffer, result in high degradation of the ENOB. The traditional solution for correction of this error is no longer effective, and it is difficult to be calibrated off-chip.

2) Positive or negative offsets in the reference voltage have different effects and will highly degrade the SNR or the SFDR performance, respectively. However, both offset problems limit the full-scale input/output signal swings.

3) Random noise also limits the full-scale signal swing and it becomes very critical in low voltage design.

All the derived equations and modeling methods presented were thoroughly verified by computer simulations with real parameters.

## ACKNOWLEDGMENT

This work is in part technical supported by *Chipidea Microelectronics* (Macau) Ltd. Special thanks to to *Gonçalo Minderico* for valuable discussions. This work is financially supported by *University of Macau* under the research grant with Ref No: RG069/02-03S/MR/FST.

## REFERENCES

[1] H. Marie and P. Belin, "R, G, B acquisition interface with line-locked clock generator for flat panel display," *IEEE JSSC*, vol. 33, pp. 1009-1013, July 1998.

[2] M.Waltari, L. Sumanen, T. Korhonen, K. Halonen, "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," *IEEE ISSCC. Digests*, pp. 314-315, Feb. 2002.

[3] Sang-Min Yoo, *et al.*, "A 2.5V 10b 120 MSample/s CMOS pipelined ADC with high SFDR," in *Proc. of IEEE CICC*, pp.441-444, May 2002.

[4] B. Hernes, *et al.*, "A 1.2V 220MS/s 10b pipeline ADC implemented in 0.13$\mu$m digital CMOS," *IEEE ISSCC, Digests*, pp. 256-257, Feb. 2004.

[5] E. Bilhan, *et al.*, "Behavioral model of pipeline ADC by using SIMULINK," *in Proc. of the Southwest Symp. on Mixed-Signal Design*, pp.147-151, Feb. 2001.

[6] M. Taherzadeh-Sani, *et al.*, "An analytical approach to the estimation of dynamic non-linearity parameters in pipeline A/D converters," in *Proc. of the ESSCIRC'03*, pp. 715–718, Step. 2003.

[7] U.K. Moon and B.S. Song, "Background digital calibration techniques for pipelined ADCs," *IEEE Trans. on CAS-II*, vol. 44, no. 2, Feb. 1997.

[8] Ahmed M. Abdelatty Ali and K. Nagaraj, "Background calibration of operational amplifier gain error in pipelined A/D converters," *IEEE Trans. on CAS-II*, vol. 50, no. 8, Step. 2003.

[9] Jipeng Li and Un-Ku Moon, "Background calibration techniques for multistage pipelined ADCs with digital redundancy," *IEEE Trans. on CAS-II*, vol. 50, no. 9, Step. 2003.

[10] Larry Singer, *et al.*, "A 12 b 65 MSample/s CMOS ADC with 82dB SFDR at 120 MHz," *IEEE ISSCC, Digests*, vol. 1, pp. 38 –39, Feb. 2000.