BANDPASS SIGMA-DELTA MODULATOR SIMULINK® NON-IDEALITIES MODEL WITH BEHAVIOR SIMULATION

Chon-In Lao, Seng-Pan U, R.P.Martins[1]

Faculty of Science and Technology, University of Macau,
Avenida Padre Tomás Pereira, S.J., Taipa, Macau SAR, China.
E-mail - benspu@umac.mo (1 - on leave from IST. E-mail - rmartins@umac.mo)

ABSTRACT

This paper presents SIMULINK® modeling of the non-idealities of a bandpass sigma-delta modulator which are appropriate for behavioral simulation. Such non-idealities include clock random jitter, periodic timing-skew, op-amp non-idealities parameters (DC gain, slew-rate, gain-bandwidth, saturation voltage, capacitor mismatch and noise), and also the complete modulator noise analysis. Such modeling will be based on a real design example of a 4th-order switched-capacitor (SC) bandpass sigma-delta modulator with double sampling. Following the top-down design manner, the behavioral simulation targets the necessary design specifications for various building blocks.

1. INTRODUCTION

A top-down approach based on the initial system-level behavior simulation is mandatory for the design of sigma-delta modulators in order to overcome shortage of using spice-like tools, e.g. the long simulation cycle and poor choice of high-level architecture. To realize such design flow an accurate non-idealities model will be indispensable. Previously, a SIMULINK® non-idealities model for BPSDM has already been proposed in [1]. This paper will also present a set of non-idealities models for bandpass sigma-delta modulator, and the MATLAB® programming and SIMULINK® system-level behavior simulation will be used to determine the building block specifications. A more comprehensive SIMULINK® non-idealities model will be defined, including random clock-jitter, time-skew, capacitor mismatch, op-amp parameters (DC gain, slew-rate, gain-bandwidth, saturation voltage, and noise), as well as the modulator noise analysis. The effects of the non-idealities factors will also be analyzed. The bandpass sigma-delta modulator - BPSDM that will be considered in this paper is shown in Fig. 1 and it is composed by a double-sampling two-delay-loop single op-amp SC resonator structure that is suitable for low-voltage operation [2].

2. NON-IDEALITIES IN SC SDM

Usually the non-idealities factors appearing in SC circuitry that must be considered for a very accurate model to be used in behavior simulation are the following:

- Op-amp DC gain
- Op-amp SR and GBW
- Clock-jitter and Timing-Skew
- Noise analysis
- Capacitor Mismatches

They will be thoroughly discussed in the following sections.

3. CLOCK-JITTER AND TIMING-SKEW

The effect of clock jitter can be easily calculated in a lowpass sigma-delta modulator by:

$$x(t+\delta) - x(t) \approx \delta \frac{d}{dt} x(t) \qquad (1)$$

However, this expression is not suitable for a bandpass sigma-delta modulator since the input frequency f_{in} is large and also because $2\pi f_{in}\sigma_j << 1$ [3]. Moreover, timing-skew is also a critical factor in a double-sampling circuit structure since it can generate a mirror signal that can damage the fs/4 BPSDM communication channel. To model these two factors in a precise manner the block-diagram of a "noisy" Sine-generator is shown in Fig. 2. On the other hand, Fig. 3 presents the degradation of the SNR performance when the time-jitter variance increases. Fig. 4 shows the mirror signal caused by different time-skew.

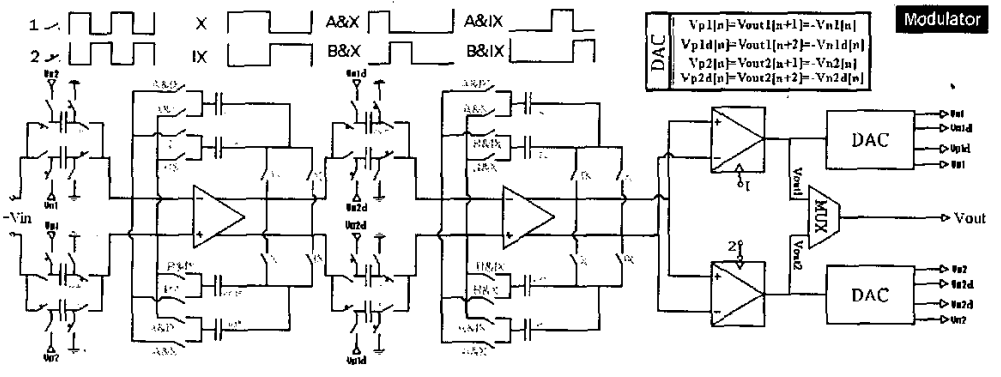

Figure 1: Proposed Bandpass Sigma-Delta Modulator

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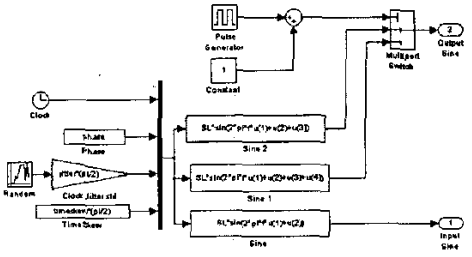

Figure 2: "Noisy" Sine-generators Block-Diagram

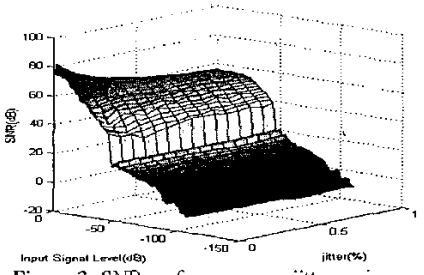

Figure 3: SNR performance vs. jitter variance (100% jitter variance = 1/fs)

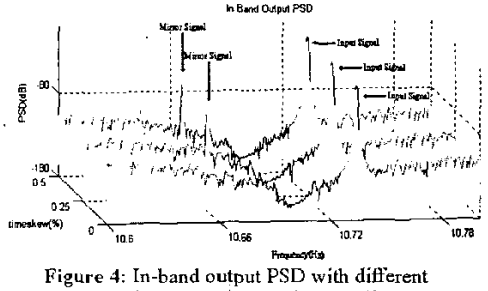

Figure 4: In-band output PSD with different time-skew (100% time-skew = 1/fs)

4. RESONATOR NON-IDEALITIES

The key-block of the BPSDM presented before is a double-delay single op-amp Switched-Capacitor resonator with double-sampling that is shown in Fig. 5. Several non-ideal factors affect the operation of this resonator that can significantly degrade the modulator performance, they are: Op-amp DC gain, Op-amp SR and GBW, Saturation voltage, Capacitor mismatches.

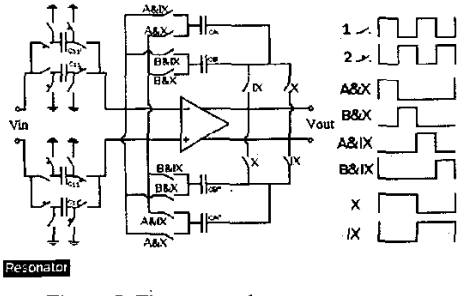

Figure 5: The proposed resonator structure

A resonator model that includes all of those factors is presented in Fig. 6.

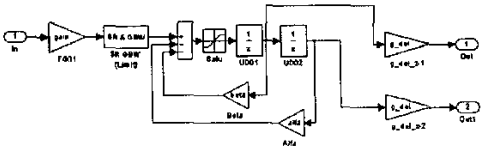

Figure 6: Resonator Model

(1) Op-amp DC gain

Insufficient op-amp DC gain degrades the noise-shaping performance since it shifts the resonator poles (NTF zeros) away from fs/4 (moving them to the sideways or inward of the unit-circuit). In this case, the effect can be expressed by the follow equation:

$$\frac{Vout(z)}{Vin(z)} = \frac{C_s}{C_h} \cdot \frac{\left(\frac{1}{1+\frac{1}{A_{DC}\times\beta}}\right) z^{-1}}{1+z^{-1}\left(\frac{(-\frac{C_{in}}{A_{DC}\times C_h})}{1+\frac{1}{A_{DC}\times\beta}}\right)+z^{-2}\left(\frac{(\frac{1}{A_{DC}}+1)}{1+\frac{1}{A_{DC}\times\beta}}\right)}$$

$$\text{where} \quad \beta = \frac{C_h}{C_s + C_h + C_{in}} \qquad (2)$$

It is clearly shown that insufficient op-amp dc gain will move the resonator poles (modulator zeros) away from fs/4. The shift of the resonator poles will degrade the modulator performance. Fig.7 shows the pole location when op-amp DC gain is changed. Fig. 8 shows the SNR performance degradation when the value of the op-amp DC gain decreases.

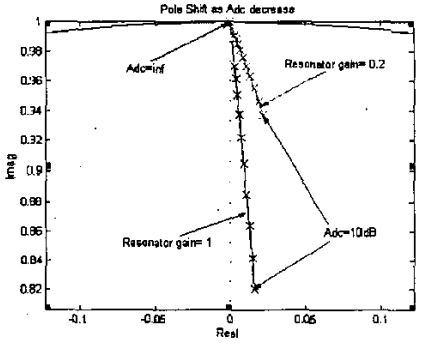

Figure 7: Pole-location vs. op-amp DC gain decrease

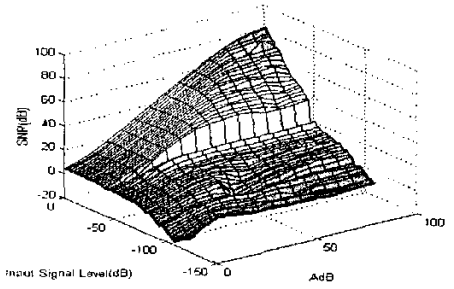

Figure 8: SNR performance vs. DC gain decrease

(2) SR and GBW

The Op-amp SR and GBW can be interpreted as a non-linear gain [4]. Since the resonator here will perform the integration in each clock phase,

$$V_s - V_{out}(nT - 2T) = V_{out}(t)$$
$$where \quad V_s = \frac{C_s}{C_h} V_{in}(nT - T)(1 - e^{-\frac{t}{\tau}}) \tag{3}$$

And the maximum slope is:

$$\frac{d}{dt} V_{out}(t)\Big|_{MAX} = \frac{C_{s1}}{C_B} \frac{V_{in}(nT - T)}{C_B} \tag{4}$$

It is possible to derive the following two cases:

Max Slope <= SR

$$V_s = \frac{C_{s1}}{C_B} V_{in}(nT - T)(1 - e^{-\frac{t}{\tau}}) \tag{5}$$

Max Slope > SR

$$V_s = \frac{C_s}{C_h} V_{in}(nT - T) + (SR \times to - \frac{C_s}{C_h} V_{in}(nT - T)) \times (1 - e^{-\frac{t-to}{\tau}}) \tag{6}$$

$$Where \quad to = \tau \times \ln\left|\frac{C_s}{C_h} \frac{V_{in}[n-1]}{\tau \times SR}\right|$$

Based on this we can implement the SR-GBW model, shown in Fig. 9, where the complete settling relies on both GBW and SR. If the SR is ignored (SR=Inf) then small values of GBW will only affect the resonator gain. The effect is the same when the resonator output is scaled-down [2] which can be recovered by setting the resonator gain. However, if the GBW and SR together are considered together, non-linear gain will be introduce if one or both factors are too small. This non-linear gain will degrade the overall performance as shown in Fig. 10.

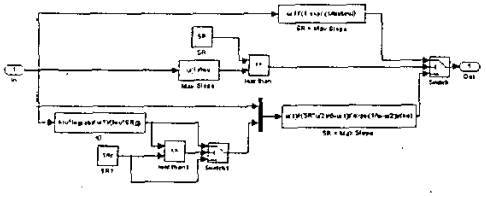

Figure 9: GBW-SR Model

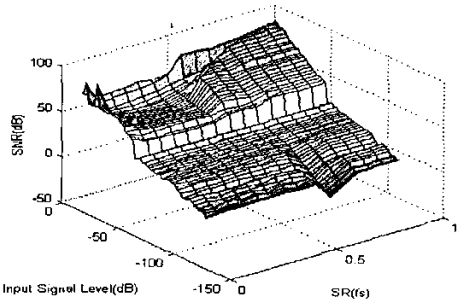

Figure 10: SNR performance vs. SR decrease

(3) Saturation Voltage

The saturation voltage will affect the BPSDM performance since the resonator output will be several times larger than the input. A SIMULINK® saturation block can model this non-idealities. (Fig. 6)

(4) Capacitor Mismatches

Capacitor mismatches can cause also a mismatch in the transfer function. This happens because the operation of the resonator has separate paths, A&B for double-sampling and time-interleaved integration, and X&IX for inversion of each clock cycle by negative feedback. This will cause a mismatch in the resonator transfer function. This effect will create a mirror image, equivalent to a time-skew, and increase the in-band quantization noise, as presented in Fig.11. It can be modeled as a set of transfer functions as represented in the block-diagram of Fig. 12. The capacitor mismatches std. is assumed to have a normal distribution.

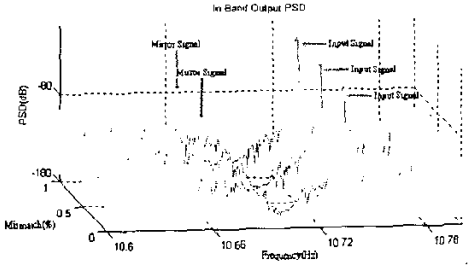

Figure 11: In-band output PSD with different capacitor mismatches std.

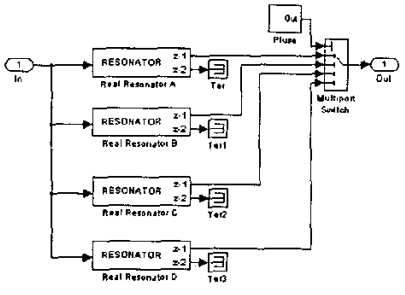

Figure 12: Capacitor mismatches Model

5. MODULATOR NOISE

There are two types of noise that affect the modulator performance, thermal noise from the switches and op-amp thermal noise. The flicker noise won't affect the performance since the desired signal is located away from the baseband. The switches thermal noise is simply the kT/C_s. The effect of the op-amp white noise is calculated by time-domain difference equations and the resonator op-amp white noise transfer function can be expressed as:

$$\frac{V_{out}(z)}{e_{amp}(z)} = \frac{C_h + C_s}{C_h} \frac{1 + \frac{C_h}{Ch+C_s} z^{-2}}{1 + z^{-2}} \qquad (8)$$

By using a SIMULINK® model to implement this filter noise, the complete modulator noise can be calculated by difference equations in the time-domain which will lead to the op-amp white noise transfer functions:

$$\frac{V_{o1}(z)}{V_{i1}(z)} = \frac{C_{s2}}{C_{h2}} \frac{C_{s1} + C_{h1}}{C_{h1}} \frac{z^{-1}(1 + \frac{C_{h1}}{C_{s1} + C_{h1}} z^{-2})}{(1 + (2 - \frac{C_{s2}}{C_{h2}} \frac{C_{s1}}{C_{h1}} - \frac{C_{s2}}{C_{h2}}) z^{-2} + (1 - \frac{C_{s2}}{C_{h2}}) z^{-4})}$$

$$\frac{V_{o2}(z)}{V_{i2}(z)} = \frac{C_{s2} + C_{h2}}{C_{h2}} \frac{(1 + z^{-2})(1 + \frac{C_{h2}}{C_{s2} + C_{h2}} z^{-2})}{(1 + (2 - \frac{C_{s2}}{C_{h2}} \frac{C_{s1}}{C_{h1}} - \frac{C_{s2}}{C_{h2}}) z^{-2} + (1 - \frac{C_{s2}}{C_{h2}}) z^{-4})}$$

(9a) and (9b)

This implies that the resonator noise can be added to the modulator block diagram as filter noise, like it is shown in Fig. 13, where the overall model of the BPSDM is presented. The valid design specifications are shown in Table.1 and more details about the modulator can be found in [2].

6. CONCLUSIONS

This paper describes a more accurate non-idealities model in SIMULINK® for a bandpass sigma-delta modulator. The effects of the non-idealities factors were analyzed and a valid building-block specification design with the models, and respective behavior simulations, of those non-idealities is also presented.

7. REFERENCES

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Table.1 Valid Design Specifications

Specifications			
Centre Frequency		10.7MHz	
Bandwidth		200kHz	
Sampling Frequency		42.8MHz	
Clock Frequency		21.4MHz	
Circuit parameter			
F1	0.2	Cs1	0.5 pF
F2	0.25	Ch1	2.5 pF
B1	1	Cs2	0.5 pF
B2	1	Ch2	2.0 pF
Non-idealities			
DC Gain	90 dB	Jitter	<=0.1 %
Cin	0.288 pF	Time-Skew	<=0.1 %
GBW	220 MHz	Sat. Voltage	1.2 V
SR	280V/μs	Cap.Mismatch	<=0.1%
Cs	Cs=0.5 pF	Op-amp Noise	<=-90dB
Performance			
Peak SNR		79 dB	
DR		83 dB	

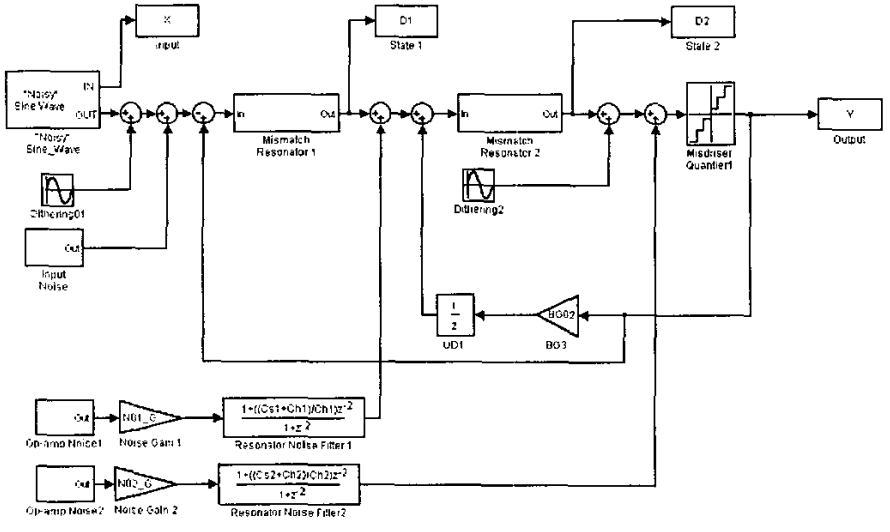

Figure 13 Overall SIMULINK Non-Idealities Model