3.2 A Regulation-Free Sub-0.5V 16/24MHz Crystal Oscillator for Energy-Harvesting BLE Radios with 14.2nJ Startup Energy and 31.8µW Steady-State Power

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This paper reports a regulation-free sub-0.5V crystal oscillator (XO) for Bluetooth Low-Energy (BLE) radios [1] that can be self-powered by harvesting the ambient energies, avoiding the loss and cost of the interim power converters. An ultra-low-voltage *Dual-Mode g_m Scheme* assisted by *Scalable Self-reference Chirp Injection (SSCI)* is proposed (Fig. 3.2.1) for the XO to surmount the operating challenges under an inconstant sub-0.5V V_{DD} (e.g. thermoelectric [2], ~80mV/K dependence) in both startup and steady states. Compatibility with different crystals (16/24MHz) is achieved, together with lower startup energy (14.2nJ) and steady-state power (31.8µW) than the recent art [3-5].

When an energy-limited BLE radio is duty-cycled to save the average power, both the startup energy (E_S) and time (t_S) of its XO are crucial to reduce the response latency and redundant power [3]. Herein, we present two circuit techniques that aid t_S reduction without momentarily raising the startup power, culminating in a lower E_S and relaxed power-source design.

Dual-Mode g_m Scheme: An XO with a 1-stage g_m (A_{XO-1}) is commonly used to optimize the phase noise (PN) [3-5]. As shown in Fig. 3.2.2 (upper-left), its impedance between the I/O (Z_{amp-1}) is given by

$$Z_{amp-1} = -\frac{g_m}{4\omega_0^2 C_L^2} + \frac{1}{j\omega_0 C_L} \ ,$$

where C_L is the crystal's load capacitance and $\omega_0 = 2\pi f_0$, where f_0 is the oscillation frequency. Since Z_{amp} is shunted by the crystal's stray capacitance (C_S), the negative resistance (R_N) of the overall impedance looking from the crystal core (Z_C) is

$$R_N \equiv -Re(Z_c) = -\frac{Re(Z_{amp})}{[\omega_0 C_S Re(Z_{amp})]^2 + [1-\omega_0 C_S Im(Z_{amp})]^2} \ .$$

A large R_N favors t_S reduction [4]. For A_{XO-1} where $Im(Z_{amp-1})$ is negative (capacitive), the maximum R_N is $C_L/[2\omega_0 C_S(C_L+C_S)]$ for $g_m = 4\omega_0 C_L(1+C_L/C_S)$, which is the upper limit if raising only g_m [4,5]. For instance, R_N is limited to 1.2kΩ with a C_S of 2pF, even an oversized g_m of 14.5mS could be applied, under typical f_0=24MHz and C_L=6pF.

To surmount the aforesaid R_N limit, a positive Im(Z_{amp}) is conceived to counteract the effect of C_S. Herein we propose a 3-stage g_m (A_{XO-3}) with designated capacitive loads (Z_{o1-2}) to mimic an inductor during the startup (Fig. 3.2.2, upper-right). Although a multistage g_m has been attempted in [6] to save the steady-state power, its inductive feature has not been revealed for t_S reduction. When Z_{amp-3} behaves inductively, Im(Z_{amp-3})>0 can be achieved over 13 to 46MHz as shown in the locus plot (Fig. 3.2.2, lower-left). For instance, given a small g_m of 2.3mS, R_N of A_{XO-3} is 2.4kΩ after paralleling with a C_S of 2pF (Fig. 3.2.2, lower-right), which is ~9× higher against that of A_{XO-1} with the same g_m. It is clear that A_{XO-3} is inferior to A_{XO-1} in terms of PN. Thus, when the crystal has gained sufficient energy during the startup, A_{XO-3} will be turned off (with an external control signal), leaving A_{XO-1} to sustain the oscillation.

Scalable Self-reference Chirp Injection (SSCI): Signal injection close to f_0 of the crystal is proven efficient and robust for t_s reduction [4]. The XO in [3] exhibits a slashed t_S (<400µs) by dithered-signal injection to the crystal, but entails trimming to handle the PVT variations on the injection oscillator. While chirp-modulated-signal injection [4] averts calibration, the related RC-sweeping unit is area hungry (~90% of the area) due to its large time constant. Also, PVT variations of the ring oscillator (RO) and RC elements hinder its utility. To address those pitfalls, we introduce SSCI to generate a chirping signal accelerating the startup of the XO (Fig. 3.2.3). Unlike the RC-based chirping [4], here a 5-stage uncalibrated RO is incorporated with a finite state machine (FSM) to digitally scale the injection time (t_{CI}), which is decided by the number of exciting cycles at each cap-bank value C_{OSC}. This scalability covers 10 to 38MHz for robustness, and renders the XO compatible with different crystals (i.e., L_M and optimum t_{CI} are package-dependent [4]). To maximize the injection energy (i.e., 50% duty cycle), the chirp-modulated signal is a div-by-2 output from the RO. It serves as the exciting signal for the crystal via an output driver, and trigger signal for the FSM. The FSM counts the pulses, and sequentially raises C_{OSC} by sending the control f_{ctrl} to RO. The RO is powered down by the FSM automatically after the injection.

For sub-0.5V operation, subthreshold common-source (CS) amplifiers with resistive loads are applied for both A_{XO-1} and A_{XO-3}. Unlike the current-source load [3,5], the resistive load aids to uphold a moderate g_m even when V_{DD}<0.35V, under a small bias current (simulated at I_{dc}=100µA). For instance, the simulated g_m of A_{XO-1} is 1.3mS at V_{DD}=0.3V and –40°C, being 4× higher than the current-source load (assume an identical g_m with V_{DD}=0.35V at 20°C). The resistive load has a tradeoff of f_0 variation, but is manageable for the BLE standard: <±50ppm.

A_{XO-3} is an ac-coupled 3-stage CS amplifier (Fig. 3.2.4) assisted by a constant-g_m bias circuit. The latter secures A_{XO-3} to be inductive and a stable R_N for robust-and-fast startup against PVT. Only the micro-current (<5µA) digital and constant-g_m bias circuits entail a 0.7V that can be generated by an on-chip charge pump as in [1]. As the constant-g_m bias circuit is off after startup, the power and noise overheads are negligible. Monte-Carlo-simulated R_N (mean) of A_{XO-3} is >9.1× higher than that of A_{XO-1}, and the boosting factor is immune to C_s from 1 to 3pF. For the RO of the SSCI, it is realized by a source-degenerated CS stage to reduce its frequency deviation against PVT, while enabling sub-0.5V operation.

The XO was fabricated in 65nm CMOS with on-chip C_L of 6pF. f_0 is flexible between 16 and 24MHz. Tested with a 24MHz crystal, t_S is 530µs if only the A_{XO-3} technique is enabled during the startup (Fig. 3.2.5). With both A_{XO-3} and SSCI enabled, t_S is further shortened to 400µs (3.3× reduction) and E_S is 14.2nJ (2.8× reduction), for a 90% oscillation amplitude [4]. Note that t_S faces nonlinear reduction with respect to the achieved R_N-boosting factor of 9.6 (A_{XO-3}'s R_N over A_{XO-1}'s R_N); since g_m of M_{1-3} (Fig. 3.2.4, right) deviate from their small-signal values when the oscillation swing is developing, resulting in an aggravated R_N. Also, the XO entails an overhead time to enter the steady-state after switching to A_{XO-1} (i.e., 240µs for the case of A_{XO-3} + SSCI). The A_{XO-3}-to-A_{XO-1} switching time can tolerate ±50% uncertainty for t_S variation <10%. The XO takes ~300µs to settle for a ±20ppm f_0 accuracy [5]. The steady-state power is 31.8µW at 0.35V and the PN is -134dBc/Hz at 1kHz offset adequate for the BLE standard.

For robustness, the XO upholds a steady-state output swing >80% of V_{DD} at 0.3 to 0.5V, and t_S variation is <25% from its mean (400µs). Only the RO of the SSCI fails to start when V_{DD} is down to 0.25V, but A_{XO-3} is still in place to aid t_S reduction. Over -40 to 90°C, t_S variation is <7.5%, being 4.7× less than [3]. The frequency deviation ($\Delta f_0/f_0$) is ≤19.7 and ≤14.1ppm, respectively, over such V_{DD} and temperature ranges.

This XO succeeds in conforming to the BLE standard with adequate margin for aging (Fig. 3.2.6). The achieved E_S and area efficiency are >2.6× and >3.1× better than [3-5], respectively. The experimental setup and chip micrograph are depicted in Fig. 3.2.7-left, where the contribution of E_S and t_s reduction by each technique is appended in Fig. 3.2.7-right. By combining two startup techniques (A_{XO-3} + SSCI), the startup energy E_S and time t_S are reduced by 2.8× (40 → 14.2nJ) and 3.3× (1.3 → 0.4ms), respectively. Consistent results are measured for different crystals (16/24MHz), demonstrating a regulation-free sub-0.5V BLE-compliant XO.

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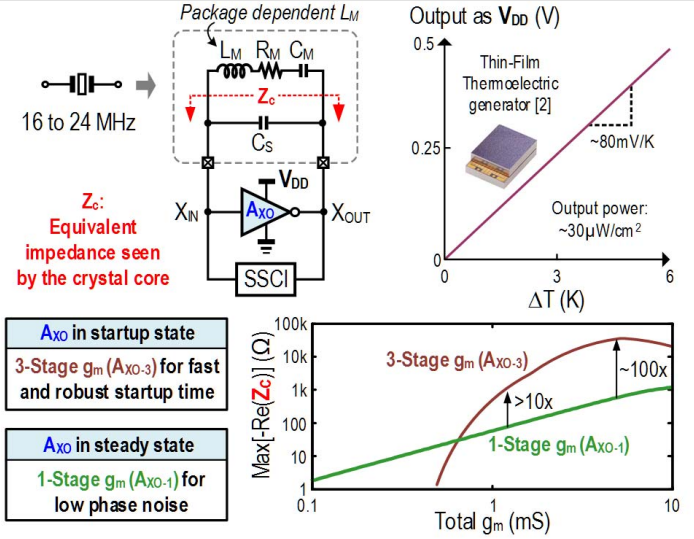


Figure 3.2.1: A 16/24MHz BLE-compliant crystal oscillator to operate from an unregulated sub-0.5V energy source, e.g. thermoelectric [2].

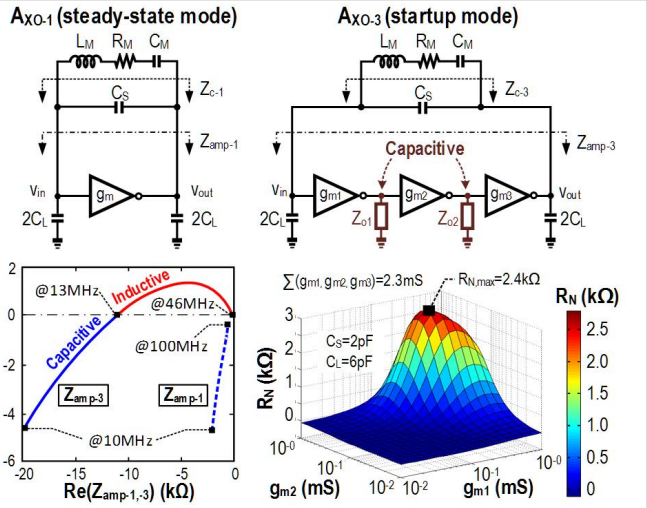
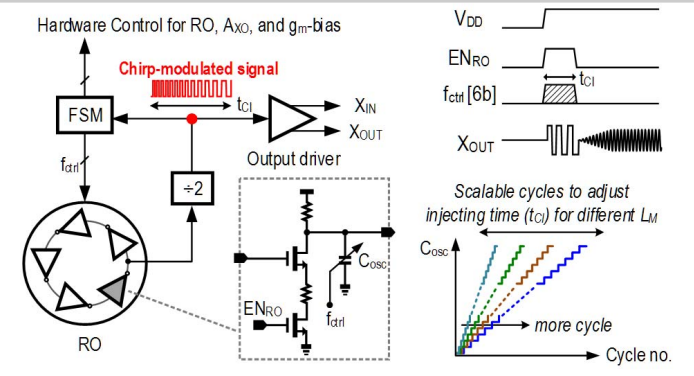


Figure 3.2.2: (Top) Schematics of crystal+A_{X0-1} for steady state and crystal+A_{X0-3} for startup. (Bottom) Simulated locus plot of $Z_{amp-1,-3}$, and A_{X0-3} shows a much higher $R_{N,max}$ at 24MHz.



Signal-injection techniques to kick-start the XO

	t_S reduction effectiveness	E_S reduction effectiveness	Trimming on auxiliary oscillator	Precision of auxiliary oscillator
Constant frequency	✓✓✓	✓✓✓	Required	Very Critical
Dithering	✓✓	✓✓	Required	Critical
Chirping	✓	✓	**Not Required**	**Relax**

Figure 3.2.3: SSCI generates a chirping signal to kick-start the XO using an untrimmed RO with relaxed precision. The FSM provides feasibility to scale t_{CI}, accommodating different crystal packages (i.e., L_M).

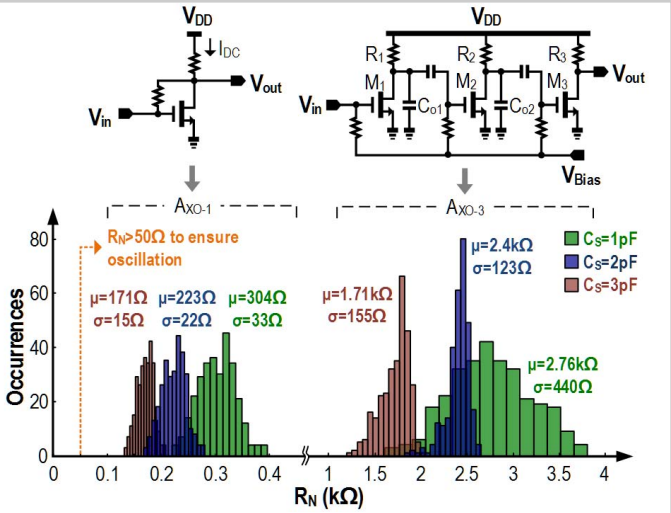


Figure 3.2.4: ULV 1-stage (left) and 3-stage (right) g_m implementation, and their Monte-Carlo-simulated R_N (N=300, V_{DD}=0.35V). For the 3-stage g_m, $C_{o1,2}$ renders Z_{amp-3} inductive.

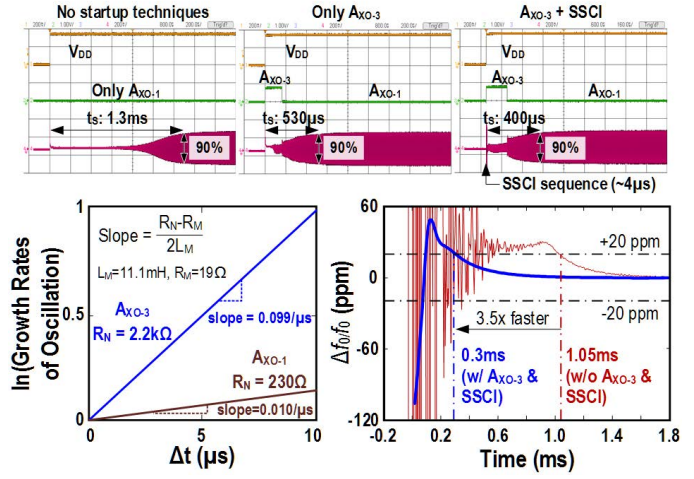


Figure 3.2.5: (Top) Measured startup times with and without proposed techniques. (Bottom, left) Estimated R_N from the exponential growth of X_{OUT}'s amplitude before the transistors enter triode region. (Bottom, right) Transient f_0 profiles of the XO (V_{DD}=0.35V, T=20°C).

		This work		JSSC'16 [4]	ISSCC'16 [3]		ISSCC'17 [5]
Applications		BLE		Bluetooth	BLE		BLE
Fast-startup techniques		ULV inductive 3-stage g_m + SSCI		Chirp injection + g_m-boosting	Dithered injection		Dynamic load + g_m-boosting
Steady-state techniques		ULV 1-stage g_m + resistive load		1-stage inverter	1-stage g_m + current-source load		
CMOS process (nm)		65		180	65		90
Active area (mm²)		**0.023**		0.12	0.08		0.072
Supply voltage, V_{DD} (V)		**0.35***		1.5	1.68		1.0
Temperature, T_{Range} (°C)		-40 to 90		-30 to 125	-40 to 90		-40 to 90
Load capacitance, C_L (pF)		6		6 (off-chip)	6	9	10
Frequency, f_0 (MHz)		**16**	**24**	39.25	24	24	24
Startup energy, E_S (nJ)		**15.8**	**14.2**	349	--	--	36.7
Startup time, t_S (μs)		460	400	158	64	435	200†
$\Delta t_S/t_S$ over T_{range}		9.8%	7.5%	7%	±35%	±20%	26.6%
XO inaccuracy $\Delta f_0/f_0$ (ppm)	versus T_{Range} (@ 0.35V)	< -14.7 / +7.2 # (-40 to 90°C)		±5.5 (-30 to 125°C)	N/A		N/A
	versus V_{DD} (@ 20°C)	< -13.0 / +4.9 # (0.3 to 0.5V)		±0.6 (1.2 to 1.8V)	N/A		N/A
Steady-state power (μW)		**31.6**	**31.8**	181	393	693	95

* Digital & constant-g_m bias circuits are at 0.7V (current budget: 5μA) to be generated by an on-chip charge pump as [1]. † Amplitude >90% and $\Delta f_0/f_0$ <±20ppm. # worse values from 16/24MHz crystals, the BLE spec. is <±50ppm.

Figure 3.2.6: Performance summary and comparison with the recent art [3-5].

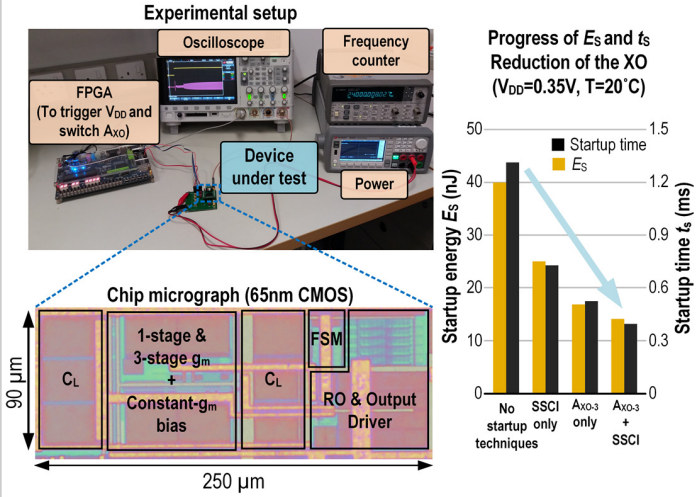


Figure 3.2.7: (Left) Experimental setup and die micrograph in 65nm CMOS. (Right) By A_{XO-3} + SSCI techniques, the startup energy E_S and time t_S are reduced by 2.8× and 3.3×, respectively.

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