A Dual-Output SC Converter with Dynamic Power Allocation for Multi-Core Application Processors

Junmin Jiang[1, 2], Yan Lu[1], Xun Liu[2], Wing-Hung Ki[2], Philip K. T. Mok[2], Seng-Pan U[1] and Rui P. Martins[1]
[1]State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China
[2]Dept. of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong
Email: jjiangah@connect.ust.hk, yanlu@umac.mo, eeki@ust.hk

Abstract–A fully integrated single-input dual-output switched-capacitor converter with dynamic power-cell allocation for application processors is presented in this summary. The power cells can be dynamically allocated according to the loads, and the efficiency is improved by 4.8%. A dual-path voltage-control oscillator (VCO) that works independently of the power-cell allocation is proposed to achieve a fast and stable regulation loop. The converter achieved peak efficiency of 83.3% and maximum combined load-currents of 100mA while maintaining minimized cross regulation.

I. Introduction

In recent years, the multi-core application processors have been widely used in smart-phone/-watch applications. To reduce the power consumption and to extend battery cycle, power saving techniques such as dynamic voltage and frequency scaling (DVFS) [1] are adopted. In such case, for each processor core, an individual power converter is needed to provide a different supply voltage, as shown in Fig. 1(a).

Fully-integrated Switched-capacitor (SC) converters with no external component are exactly suitable for multi-core processors. In typical applications, SC converters work independently and are designed with different specifications, which may lead to a large area and power overheads, as redundant area (e.g. on-chip flying capacitors) has to be reserved to handle the peak output power. For the case of two imbalanced loads (Fig. 1(b) with I_{O1} being light and I_{O2} heavy), it is a waste of on-chip resources if two power converters are identical. Many multi-output SC converters were reported to deal with this issue. In [2] and [3], two output voltages with different loading ranges are provided, but the outputs are not interchangeable. In [4], the controller is shared, but the three output voltages are still from three individual SC converters without sharing the power resources.

To tackle the above issues, we designed and tested a fully integrated dual-output SC converter with dynamic power-cell allocation [5]. The power cells are shared by two outputs and can be dynamically allocated according to load demands. The benefits are reduced area overhead, increased capacitor utilization and increased overall power efficiency.

II. Dual-Output SC Converter

A. Strategy of Dynamic Power Allocation

The strategy of dynamic power-cell allocation is shown in Fig. 2. The converter has two output channels CH_1 and CH_2 providing output voltages V_{O1} and V_{O2}, respectively. The capacitors in the power stages are shared by both channels. Each output is regulated through frequency modulation, and the switching frequencies of the two channels (f_1 and f_2) reflect the loading conditions. The target is to adjust f_1 and f_2 to be equal, so that both channels have the same power density, and the converter achieves the best overall efficiency.

Assume that the two channels start with the same number of power cells, but I_{O1} is larger than I_{O2}. To regulate the outputs properly, initially we have $f_1 > f_2$. The control loop is to make f_1 equal to f_2 by assigning more power cells to CH_1 cycle by cycle, moving the physical boundary right, until $f_1 \approx f_2$. By balancing the power densities of the two channels with an optimal switching frequency, both switching and parasitic losses are reduced. By dynamically adjusting both the number of power cells and the optimal switching frequency, the channels are ensured to provide sufficient power to the loads, and the utilization of capacitors is maximized.

B. Circuit Implementation

The system architecture is shown in Fig. 3. The power cells are connected to the channel selection switches, thus they are in either CH_1 or CH_2. The selection switches are controlled by a bi-directional shift register (SR), whose direction is decided by the frequency comparator. In this design, the left part, where $sel_{[1:n]}$ are 0, is CH_1; and the right, where $sel_{[n+1:n+m]}$ are 1, is CH_2. After each comparison, the SR will shift by 1 bit to left or right according to the comparison result, so the boundary of the two channels will shift along adjacent power cells.

As shown in Fig. 4, a dual-path voltage controlled oscillator (VCO) is used to enable the power allocation. The VCO generates the clock phases for each power cell with 82 delay cells. One delay cell in CH_1 ($DC_{1[n]}$) has a complementary delay cell in CH_2 ($DC_{2[n]}$). If $sel_{[n]} = 1$, $DC_{1[n]}$ of VCO (CH_1) is enabled. At the same time, $DC_{2[n]}$ will be shorted and the clock phase is redirected to the next cell. In this way, the number of delay cells in each VCO is equal to the number of its power cells. The phases $\varphi_{1[n]}$ and $\varphi_{2[n]}$ are chosen by the MUX and then distributed to the power cell. So the output voltage ripple can also be reduced by multi-phase interleaving.

The two frequencies of the VCO are controlled by the two error amplifiers as shown in Fig. 4. The two outputs are regulated independently, regardless of the power-cell arrangement, therefore cross regulation is minimized. The speed of the regulation loop is much faster than the power-cell allocation, so the stability is ensured. For each power cell, it is composed of 2 flying capacitors and 8 power transistors with VCRs of 2/3x and 1/2x.

III. Measurement Results

The proposed SC converter was fabricated in a 28nm CMOS process, occupying an active area of 1.2mm x 0.5mm. Fig. 5 shows the chip micrograph and testing setup. Fig. 6 shows the measured waveforms of the steady state outputs, and the load transient response. It verified that the two output voltages could be independently regulated and the two

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switching frequencies were adjusted to be very close. With the load at V_{O1} switched from 4mA to 40mA, the settling time was within 500ns. The cross regulation at V_{O2} was less than 10mV at the rising edge and negligible at the falling edge, verifying that the dual-path VCO control could achieve minimized cross regulation.

Fig. 7 shows the measured efficiencies vs. I_{O1} and I_{O2}. The peak efficiency was 83.3% with the load currents of 50mA for both channels. Due to the proposed dynamic power-cell allocation, the converter achieved over 80% efficiency when I_{O1} and I_{O2} were larger than 15mA. The efficiency with allocation is improved by 4.8% than without allocation. Table I compiles performance comparison with prior-art SC converter works [2], [3], and [4].

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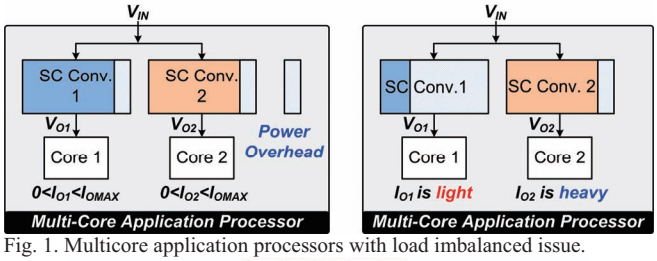

Fig. 1. Multicore application processors with load imbalanced issue.

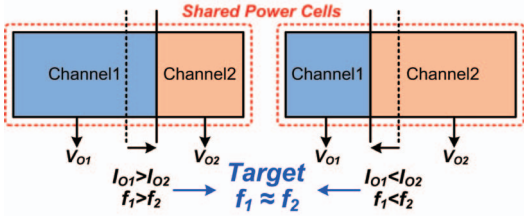

Fig. 2. Strategy of dynamic power-cell allocation.

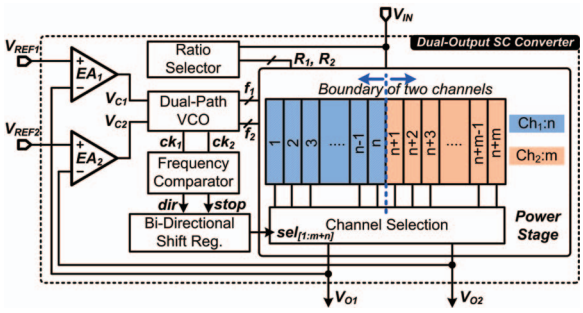

Fig. 3. System architecture.

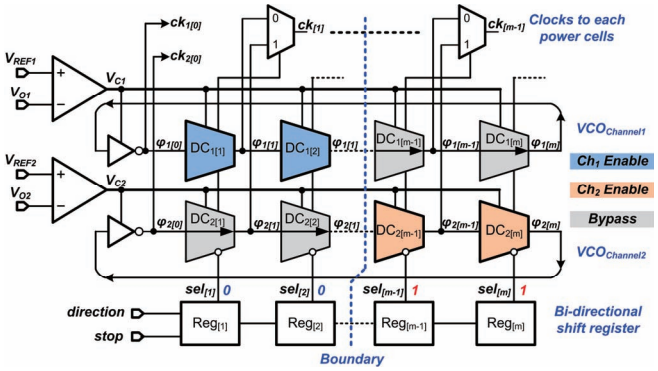

Fig. 4. Circuit implementation of dual-path VCO.

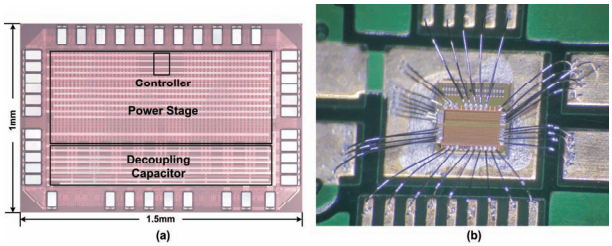

Fig. 5. (a) Chip micrograph, (b) top and bottom view of PCB.

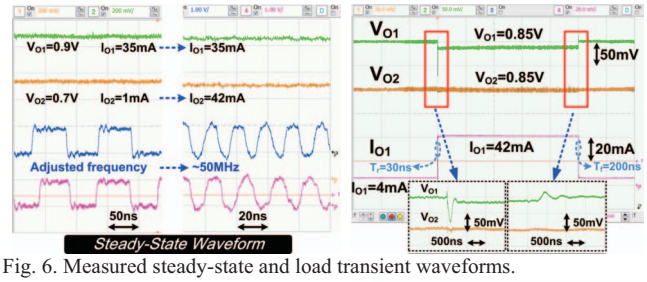

Fig. 6. Measured steady-state and load transient waveforms.

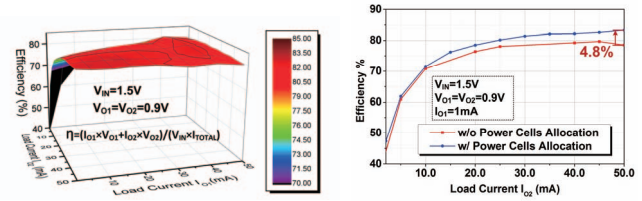

Fig. 7. Measured efficiency versus loading currents.

TABLE I PERFORMANCE COMPARISON

Work	ISSCC`16 [2]	JSSC`15 [3]	ISSCC`16 [4]	This work [5]
Technology	65nm	0.35µm	180nm	**28nm**
Topology	Step-Up/Down	Step-Up	Step-Down	**Step-Down**
Number of Outputs	2	2	3	**2**
Passive Type	On-chip Off-chip	Off-chip	On-chip (MIM+MOS)	**On-chip (MOM+MOS)**
V_{IN}	0.85-3.6V	1.1-1.8V	0.9-4V	**1.3-1.6V**
V_{OUT}	0.1-1.9V	2V, 3V	0.6V, 1.2V, 3.3V	**0.4-0.9V**
$I_{O,MAX}$	10mA	24mA	100uA	**100mA**
Total C_{FLY}	1µF	9.4µF	3nF	**8.1nF**
η_{peak}	95.8%	89.5%	81%	**83.3%**
Power Density	N/A	N/A	250µW/mm²	**150mW/mm²**
Max. Load per Output	V_{O1}: 1mA V_{O2}: 10mA	V_{O1}: 12mA V_{O2}: 12mA	V_{O1}: 33µA V_{O2}: 33µA V_{O3}: 33µA	**V_{O1}: 0-100mA V_{O2}: 100-0mA**
Symmetrical Outputs	No	No	No	**Yes**