A 550µW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental Converter with 256-cycles in 65nm CMOS

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Abstract

This paper presents an incremental A/D converter with a two-phase linear-exponential accumulation loop. In the linear phase, the loop works as a first-order structure. The noise coupling path is then enabled in the exponential phase thus boosting the SQNR exponentially with a few number of clock cycles. The uniform-exponential weight function allows data weighted averaging (DWA) to work well suppressing the DAC mismatch error. Fabricated in 65nm CMOS under 1.2V supply, the ADC achieves an SNDR/DR of 100.8dB/101.8dB with 20kHz BW, 550µW & 0.134mm^2, resulting in FoM$_W$ and FoM$_S$ of 153fJ/176.4dB (SNDR), respectively.

Introduction

The incremental ADC (IADC) has drawn attention as an alternative candidate to the sigma-delta ADC for application in sensors, wearable devices and instrumentation for its low-latency, easy multiplexing and Nyquist-like properties that relax the digital post-processing filter [1]. However, when compared with sigma-delta modulators of similar order, the intrinsic sample-variant weights of high-order IADCs degrade the performance on thermal noise and simple dynamic element matching (for multi-bit DACs). For example, a 2nd-order 5-level IADC in [2] with simple DWA, and a 2nd-order 9-level IADC in [3] with a complicated DEM, both achieve a harmonic-limited SNDR of <92dB. The DEM and DAC in [4] have a fine-stage with large OSR=2k, thus relaxing the mismatch errors. This paper presents for the first time an exponential-incremental converter which accumulates the residue in a fast and stable approach. The proposed single-loop two-phase exponential accumulation sequence combines the benefits of thermal noise and DAC mismatches suppression from the first order linear phase and the SQNR boosting capability for the following next accumulation phase.

Linear-Exponential Incremental Converter

By increasing the number of clock cycles per conversion (or oversampling ratio, OSR), the signal is accumulated linearly to bi-quadratically in 1st to 4th order incremental architectures, respectively. However, an exponential accumulation would be considerably faster, corresponding to the block diagram of Fig.1 with integrator transfer function given by $\frac{z^{-1}}{1-(1+k)z^{-1}}$. Unlike the sigma-delta converters, the loop suffers less from stability issues using exponential accumulation due to the resetting action of the IADC. The larger the coefficient k, the faster the accumulation leading to higher resolution. However, such scheme is not effective in suppressing the thermal noise, because the sampling capacitor weights are sample-variant and decrease exponentially rather than gradually like in conventional high-order IADCs [2-4], or are kept constant like in 1st-order IADCs [1]. For example, at an OSR=256, the effective reduction of thermal noise by OSR (i.e. OSR$_{eff}$) is also

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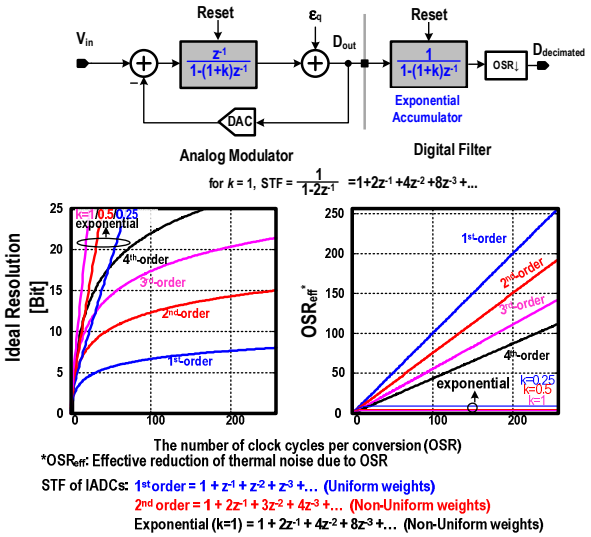

Fig. 1 Conceptual diagram of an exponential-incremental converter, and its trends of resolution and effective OSR$_{eff}$.

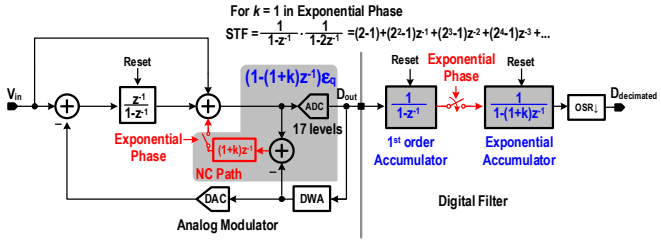

Fig. 2 Block diagram of the linear-exponential incremental converter

256 for 1st-order structure thus retaining the full benefit of the oversampling, but the 2nd, 4th-order and exponential (k=1) would have the OSR$_{eff}$ decreased by 23%, 57% and 99%, respectively, as Fig. 1 shows. For a given OSR and k=1, the sample-variant weights decrease by half for every increasing clock cycle, penalizing the effective OSR$_{eff}$ for input-referred thermal noise in the exponential-incremental converter.

The proposed two-phase scheme resolves such thermal noise limitation in exponential IADCs, by periodically deactivating the exponential accumulation at the beginning of the conversion. As Fig. 2 illustrates, only a 1st-order integrator is utilized at the beginning of the linear phase with the loop working as a 1st-order structure for equal weights of 246 cycles, and the oversampling will fully contribute to the reduction of the thermal noise. In the exponential phase, an extra noise-coupling (NC) path is activated which creates an exponentially accumulating loop in the remaining 10 cycles. Compared to Fig. 1, the overall STF changes to $\frac{z^{-1}}{1-z^{-1}}\frac{1}{1-(1+k)z^{-1}}$ which doesn't affect the exponential accumulation since the 1st-order term is too weak when compared with the exponential term. Behavioral study of the thermal noise performance reveals the optimum choice of 246 cycles of linear phase. Thus, the scheme with linear-exponential accumulation, works complementarily, combining the best features of thermal noise

suppression and SQNR boosting. Considering the loop stability and the Opamp swing, since a larger coefficient would affect the input range, we selected a coefficient k=1. It is arguable that the capacitor mismatch would affect the coefficient k thus limiting the performance. However, the 246-cycle linear phase with a 17-level quantizer has already resolved 12-bit resolution which relaxes the matching requirement in the remaining 2nd exponential phase. The 10-cycle exponential phase resolves the residue rapidly to the final resolution.

Similarly, the proposed two-phase solution can also help suppress the multi-bit DAC mismatch problem in exponential IADCs. The weights of the DAC mismatch errors in the linear phase are homogeneous and can be averaged through simple DWA. The weights, although not uniform in the exponential phase, are decreasing exponentially. Therefore, the effect of the DAC nonlinearity in the exponential phase will have a small impact on the overall performance. With the multi-bit quantizer, the loop processes the quantization noise with a much smaller swing, implying that the opamps, especially in the first integrator, can use an energy-efficient complementary gain-boosted telescopic-cascode topology to reduce the power dissipation further. Fig. 3 exhibits the circuit implementation. The capacitors C_{ho}/C_{he}, sampling the adder output in a ping-pong manner, work with the C_{ff3} DAC to archive the noise coupling. The sampling capacitor is 8pF which is thermal-noise limited. We use the chopping technique to improve the 1/f noise performance and reduce the offset.

Measurement Results

The ADC has been fabricated in 65nm CMOS with an active area of 0.134 mm^2, as shown in the die photo of Fig. 4. Fig. 4 also shows the spectrum of the design after the digital filter with a 1.95kHz, -0.9dBFS input sinusoidal signal. The measured SNDR shows that the performance can improve from 73.0dB to 100.8dB when the exponential accumulation is turned on. Fig. 4 also indicates the effectiveness of the DWA, increasing the SNDR by 28.0dB. The ADC achieves 101.8dB of DR. Fig. 5 shows the measured 17b DNL/INL of 0.27LSB/0.84LSB, respectively. The measured SNDR variation among 15 chip samples, as well as from -20°C to 85°C and from V_{DD}=1.1V to 1.3V, are all within 1.2dB variations. The total power consumption is 550µW under 1.2V supply achieving FoM_S(SNDR)/FoM_W of 176.4dB/153fJ, respectively. Table I lists the performance summary and the comparison with the state-of-art. Fig. 6 also exhibits a benchmark. This work, improving the SQNR, and reducing the thermal noise/DAC mismatch penalty, achieved a peak SNDR exceeding 100 dB under a supply as low as 1.2V.

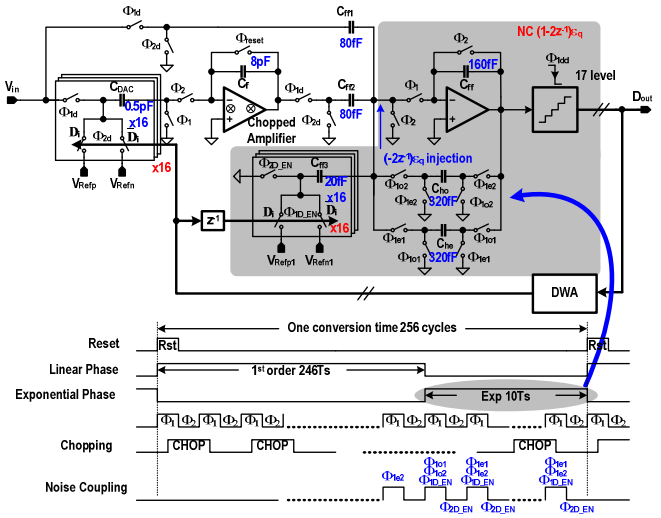

Fig. 3 Circuit diagram of the linear-exponential incremental

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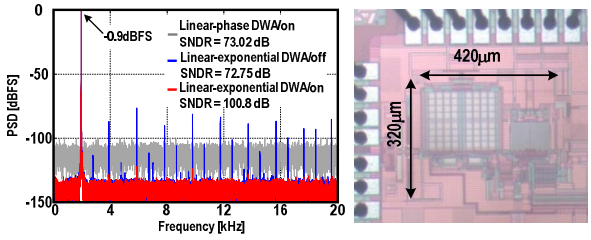

Fig. 4 Measured power spectrum and die photo.

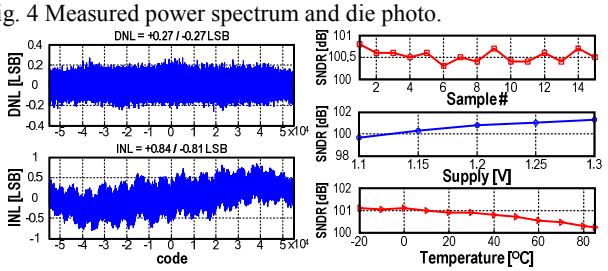

Fig. 5 Measured 17b DNL/INL, and SNDR vs. samples, V_{DD} & temp.

Table I Performance summary and comparison with the state-of-the-art

	This Work	JSSC'15 Chen [2]	JSSC'17 Zhang [1]	ISSCC'16 Gönen [5]	VLSI'17 [6] Hummerston	ISSCC'16 Shu [7]
Architecture	Linear-exponential Incremental	Two-step Incremental	Multi-step Incremental	Zoom ADC	Pipelined-SAR	Oversampling SAR
Process	65nm	65nm	180nm	160nm	180nm	55nm
Supply	1.2V	1.2V	1.5V	1.8V	1.8V/5V	1.2V
Fs	10.24MHz	192kHz	642kHz	11MHz	2MHz	1MHz
Bandwidth	20kHz	250Hz	1kHz	20kHz	1MHz	1kHz
Power	550µW	10.7µW	34.6µW	1.6mW	11.35mW	15.7µW
Peak SNDR	100.8dB	90.8dB	96.8dB	98.3dB	99.2dB*	101dB
Dynamic Range	101.8dB	99.8dB	99.7dB	107.5dB	100.5dB	N/A
FoM_W(pJ/conv.)#	0.153	0.76	0.32	0.61	0.07*	0.0856
FoM_S(dB)#	176.4	164.5	171.4	169.1	178.7*	179
Area [mm^2]	0.134	0.2	0.5	0.16	3.87	0.072

* Evaluated from data in [6]: SNR=100dB and THD = -107dB

FoM_W = Power/(2^{ENOB}*2*BW) ; FoM_S = SNDR+10log$_{10}$(BW/Power)

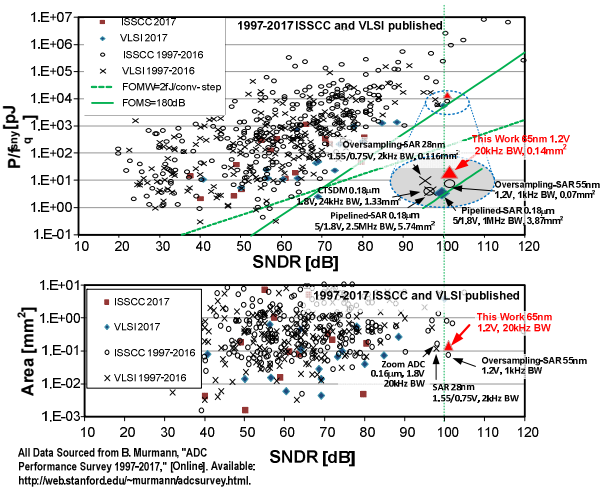

Fig. 6 Comparison to ADCs published at ISSCC/VLSI in 1997-2017.