A High-Q Spiral Inductor with Dual-Layer Patterned Floating Shield in a Class-B VCO Achieving a 190.5-dBc/Hz FoM

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Abstract—**This paper proposes a dual-layer patterned floating shield (DL-PFS) technique for Silicon-based on-chip spiral inductors. By optimally utilizing the two lowest metal layer strips to shield the inductor from the substrate, electromagnetic (EM) simulations show 40% improvement of the Q factor when compared with the conventional approach. Designed and simulated in 0.13-µm CMOS, the DL-PFS inductor in a class-B VCO achieves 6.6-dB lower phase noise, and 34% power savings. The VCO also exhibits 9.7-to-10.93 GHz tunability, and −123-dBc/Hz phase noise at a 3 MHz offset. The power consumption is 1.64 mW at 0.6 V, leading to a state-of-the-art FoM of 190.5 dBc/Hz.**

Keywords—Inductor, RFIC, VCO, Dual-layer Patterned Floating Shield

I. INTRODUCTION

With the incessant market demand of low-power and high-performance wireless transceivers the design of on-chip spiral inductors, being one of the most fundamental passive components for RF/mmWave CMOS circuits, remains a challenge. Specifically, the phase noise performance of the voltage-controlled oscillator (VCO) is severely limited by the limited Q factor of the inductor, which is accompanied by losses due to DC resistance of the inductor's metal trace, current-crowding effect and electromagnetic coupling to the substrate. Although the DC resistance can be alleviated by exploiting a thick top metal [1], and the current-crowding effect can be minimized by proper geometrical design [2], the substrate loss is still a major concern.

Generally, substrate loss arises from the inductive and capacitive coupling between the inductor and substrate. Yet, inductive loss is negligible with a Si-substrate conductivity smaller than 10 S/m, leaving the capacitive loss to dominate [3]. It can be interpreted as a displacement current flowing through the dielectric underneath the inductor to the substrate, due to the time varying electric field.

Several approaches have been reported to reduce the capacitive coupling to the substrate without extra fabrication steps. One approach was to use the patterned ground shield (PGS) inserted between the inductor and substrate [4]-[5]. However, PGS requires a relatively perfect 0 V ground voltage on the Si-chip, which is physically unrealizable due to non-zero resistivity of the metal interconnections. The shielding performance further aggravates, when the inductor is dealing with mmWave frequency due to the parasitic inductance on the ground, or when noise is coupled from other grounded circuitry.

Multi-layered PGS has also been reported [6] but it does not address the aforementioned issues. On the other hand, patterned floating shield (PFS) has been demonstrated with better performance when compared with PGS [7]-[8]. This paper proposes an improved PFS, by using two metal layers which significantly reduce the capacitive-induced substrate current, thereby boosting the Q factor by as much as 40% when compared with the conventional PFS. To demonstrate the improvement of the Q factor, a class-B VCO is also incorporated in the design, offering a 6.6-dB enhancement of the phase noise performance.

II. PROPOSED DUAL-LAYER PFS (DL-PFS)

A. Surface Current Density Induced on the Substrate

Conventionally, the orientation of the metal strips for PFS are orthogonal to the current flow in the inductor [7] as illustrated in Fig. 1. However, such shielding orientation is only effective for square inductors but not for octagonal inductors. This can be justified by the capacitive induced current density flowing in X ($\mathbf{J_x}$) and Y ($\mathbf{J_y}$) directions on the surface of the substrate at 10 GHz, when the inductor is driven differentially as illustrated in Fig. 2. Here, $\mathbf{J_x}$ and $\mathbf{J_y}$ are vector quantities which flow radially out of the inductor turns. The current flow also obeys Ohm's law, described by $\mathbf{J_{x,y}} = \sigma \cdot \mathbf{E_{x,y}}$, where σ is the substrate conductivity (S/m) and $\mathbf{E_{x,y}}$ represents the electric field tangential to the surface of the substrate. It can be observed that there are X and Y-directed current flowing along the diago-
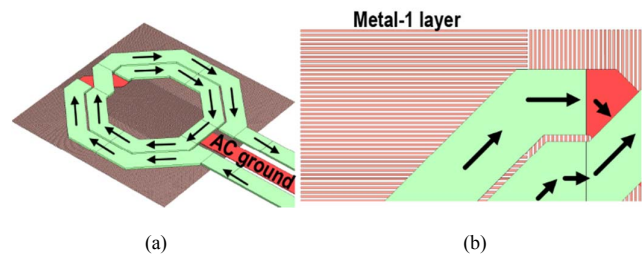

(a)   (b)

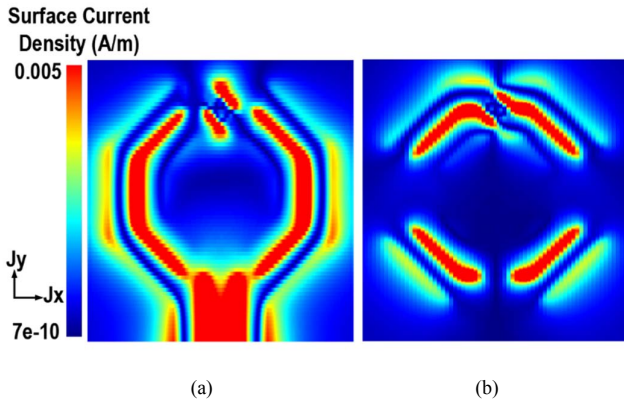Fig. 1. (a) Layout of the inductor with conventional PFS; (b) zoom-in view of the PFS.

Fig 2. Simulated surface current density on the substrate in: (a) X direction; (b) Y direction.

Fig. 3. (a) Layout of the inductor with the proposed DL-PFS; (b) zoom-in view of the proposed DL-PFS.

-nal path underneath the octagonal spiral inductor. Based on the simulated induced surface current density, this work proposes an idea of blocking the capacitive induced current flowing in the Y-direction by vertical metal strips, and the X-direction by horizontal metal strips, effectively covering the affected area induced by the capacitive coupling.

B. *DL-PFS*

The inductors are designed using 0.13-μm CMOS with thick top metal layer. Fig. 3 shows the layout of the inductor with DL-PFS. The horizontal metal strips are realized using the lowest metal-l, while the vertical metal strips are realized using metal-2 layer. The strips are 1-μm wide, separated by a 1-μm gap. Three sets of inductors, i.e. unshielded, with conventional PFS and the proposed DL-PFS are simulated using Sonnet EM for comparison. The resultant differential Q factor, Q_{diff} and its differential inductance, L_{diff} are plotted in Figs. 4 and 5, respectively, using the simulated S-parameter data defined by,

$$Q_{diff} = \frac{Im\,(Z_d)}{Re\,(Z_d)} \tag{1}$$

$$L_{diff} = \frac{Im\,(Z_d)}{2 \cdot \pi \cdot f} \tag{2}$$

where

$$Z_d = 2 \cdot Z_O \cdot \frac{1 + \dfrac{S_{11} - S_{12} - S_{21} + S_{22}}{2}}{1 - \dfrac{S_{11} - S_{12} - S_{21} + S_{22}}{2}} \tag{3}$$

and Z_O is the characteristic impedance of 50 Ω. EM simulation result reveals that the inductor with DL-PFS exhibits the highest peak Q of 38. At 10 GHz, the Q factors of the inductor without shield, with conventional PFS and DL-PFS are 21.5, 26.9 and 37.5, respectively, where the DL-PFS exhibits a Q factor improvement of 74.4% and 40% when compared with the inductor without shield and conventional PFS, respectively. By effectively blocking the electric field from penetrating into the substrate, L_{diff} of the inductor with DL-PFS also increases as shown in Fig. 5, indicating an increased ability to hold the mag-
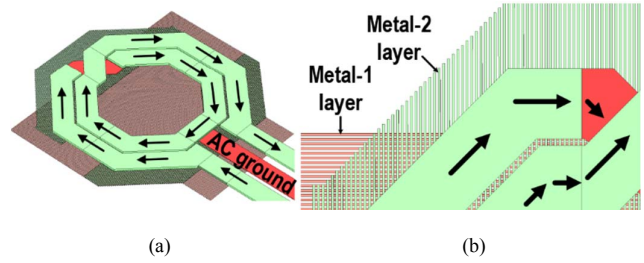
-netic field. Fig. 6 shows the comparison of the current density J_{xy} induced on the surface of the substrate at 10 GHz. For the unshielded inductor, the induced current is concentrated under-
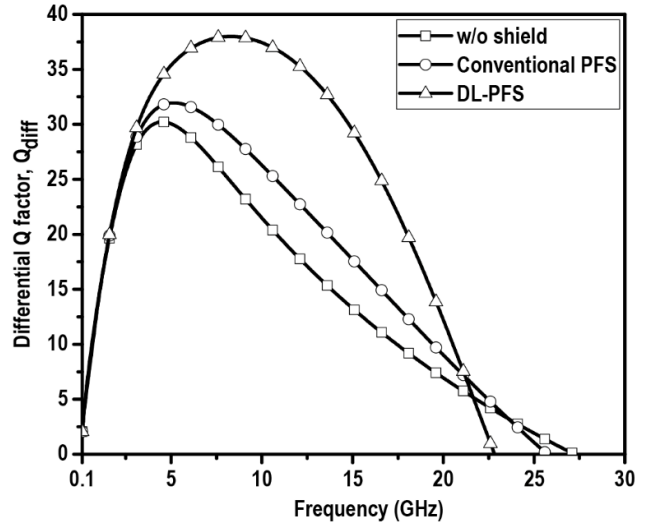

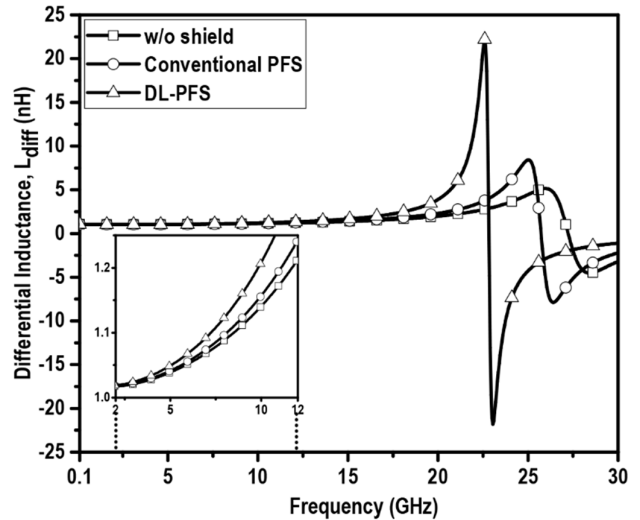Fig. 4. Simulated Q_{diff} of the 3 inductors.

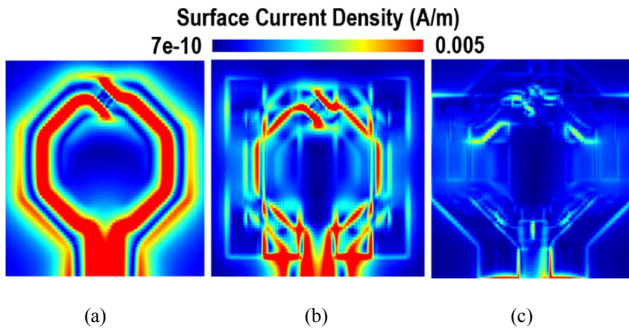Fig. 5. Simulated L_{diff} of the 3 inductors.

Fig. 6. Magnitude of the surface current density on the substrate for the (a) unshielded inductor; (b) conventional PFS; and (c) DL-PFS.

-neath the gap between the two inductor traces in parallel. The inductor with conventional PFS is not effective in reducing the capacitive induced current. Yet, for the proposed DL-PFS, the induced current is greatly suppressed not only along the horizontal and vertical traces, but also along the diagonal trace which consists of J_x and J_y as described earlier.

III. IMPLEMENTATION OF A DL-PFS INDUCTOR IN A CLASS-B VCO

In order to verify the impact of the inductor's Q factor, three inductors are implemented in a class-B VCO, whose structure is shown in Fig. 7(a), which can be tuned from 9.7 to 10.93 GHz, corresponding to a tuning range of 12%. It occupies a core area of 400 μm × 520 μm as shown in Fig. 7(b). Theoretically, the relationship between the Q and phase noise can be predicted by Leeson's Equation [9] as

$$L(\Delta f) = 10 \; \log_{10}\left[\frac{2FkT}{Q^2 P_{diss}} \cdot \left(\frac{f_0}{\Delta f}\right)^2\right] \tag{4}$$

where F is the device noise contribution factor, k is the Boltzmann's constant, T is the absolute temperature, P_{diss} is the average resistive power dissipation of the VCO across the LC tank or $P_{diss} = V_p^2/R_p$ and Δf is the offset frequency. Based on (4), a 74.4% enhancement of the Q factor directly boosts the phase
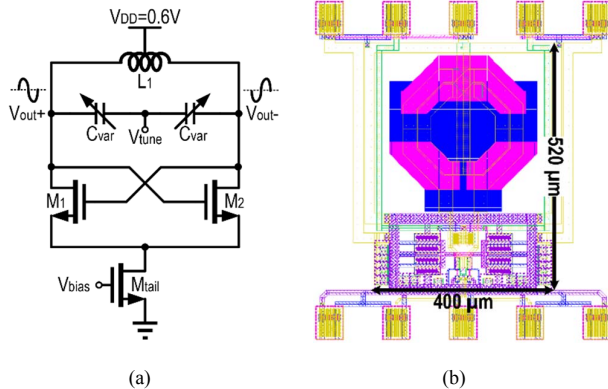

(a)   (b)

Fig. 7. (a) Schematic and (b) layout of the class-B VCO.

noise performance by at least 4.8 dB. Fig. 8 shows the phase noise plot of the VCO at 9.7 GHz. The inductor with DL-PFS shows an improved phase noise performance of at least 5dB at a frequency offset higher than 1 MHz. Specifically, the difference in phase noise at 3 MHz is the highest, when the bias current is 3 mA. As such, the inductor with DL-PFS achieves 122.9 dBc/Hz, which is better than that using the inductor without shield (-116.5 dBc/Hz) and with conventional PFS (-116.8 dBc/Hz), as shown in Fig. 9. This bias point also corresponds to the boundary between the current- and voltage-limited regimes, where the output oscillation amplitude swings at the limit set by $V_{DD} = 0.6$ V, thereby maximizing the Figure-of-Merit (FoM), defined by

$$\text{FoM} = L(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{0.001}\right) \tag{5}$$
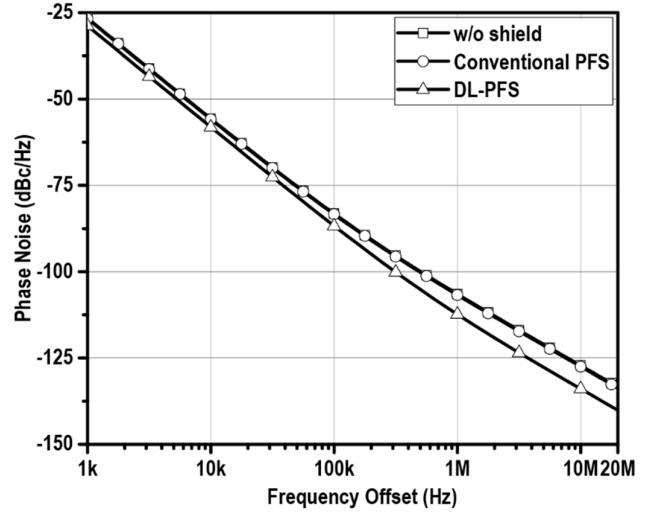

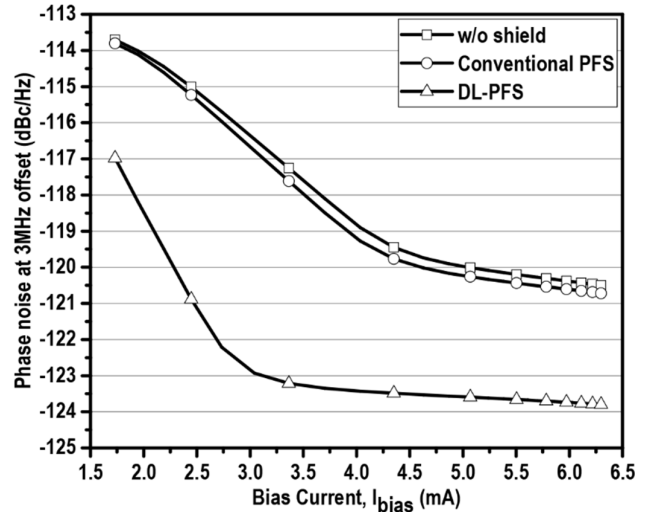Fig. 8. Simulated phase noise of the class-B VCO at 9.7 GHz.

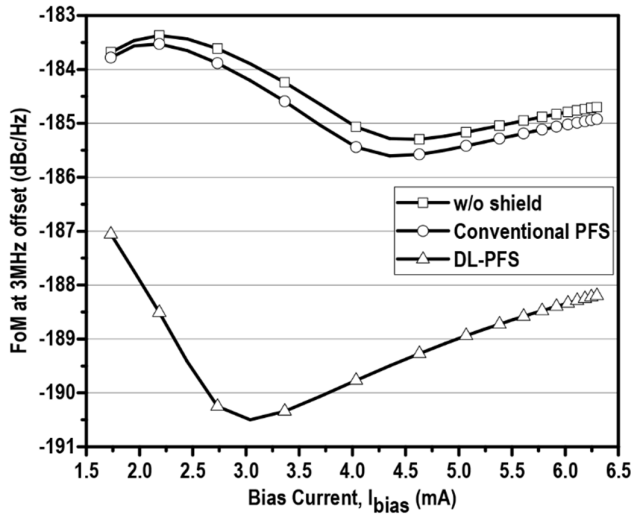Fig. 9. Comparison of phase noise at the 3-MHz offset as a function of the bias current.

Fig. 10. Comparison of FoM at the 3-MHz offset as a function of the bias current.

where P_{DC} is the DC power consumption. Due to the higher Q, DL-PFS is able to achieve the highest FoM using the least amount of current, since the tank impedance, $R_p \cong 2\pi f_0 LQ$ now increases. As shown in Fig. 10, at 3 mA, the VCO with DL-PFS demonstrates a better FoM enhancement, namely of 6.6 and 6.3 dB, corresponding to a FoM of -190.5 dBc/Hz better than the other two designs (i.e., -183.9 and -184.2 dBc/Hz). Even if the VCO with an unshielded inductor and with conventional PFS can achieve an optimum FoM by consuming extra bias current of 4.63 mA, the FoM still loses out a value of 5 dB when compared with the proposed DL-PFS. The results are in line with Leeson's phase noise equation (4). In other words, DL-PFS attains the maximum FoM as well as 34.5% in power savings, simultaneously. The comparison with the state-of-the-art VCOs [10-12] is given in Table I.

IV. CONCLUSION

It has been demonstrated that the proposed DL-PFS technique is an effective shielding solution when compared to the conventional PFS method. By reducing the capacitive induced current in X and Y direction on the substrate using two metal layers, the inductor with DL-PFS boosts the Q factor by 40% if compared with the conventional PFS. Through the implementation of the inductor in a class-B VCO, the DL-PFS enables an FoM improvement of 6.6 dB and 34.5% reduction in power consumption concurrently.

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