IMPULSE SAMPLED INTERMITTENT POLYPHASE SC FIR RATIONAL DECIMATORS WITH DOUBLE-SAMPLING

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ABSTRACT

The conventional scheme for sampled-data analog decimation with rational conversion ratio of *L/M (M>L)* suffers from undesired distortion due to the input sample-and-hold filtering effect in the front interpolation stage. Two new impulse sampled SC FIR rational decimator architectures are proposed in this paper employing the efficient Intermittent Polyphase Structures with Double-Sampled Active-Delayed Blocks (ADB's) which not only render them immune to the above distortion effect but also allow a significant relaxation of the amplifiers settling.

I. INTRODUCTION

Various types of Switched-Capacitor (SC) decimators and interpolators have been proposed in the past for applications in multirate analog-digital signal processing [1-8]. Rational sampling rate converters, in particular, are necessary in practical interfacing systems operating at different sampling rates which are not always a multiple integer. They make also possible the implementation of efficient and practical multistage converters especially for systems with prime number sampling alteration ratio and, however, stringent specifications. The *L/M*-fold analog sampling rate converters can be realised in a conventional scheme by an integer *L*-fold interpolator followed by a simple output *M*-fold downsampler, as shown in Fig.1.

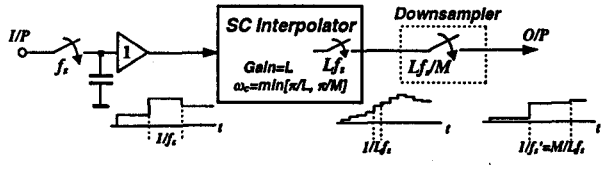

Fig.1 Conventional Scheme Implementation of Sampled-Data Analog Sampling Rate Conversion with a Rational Factor L/M

The previously available integer SC interpolators suffer from the errors caused by the sample-and-hold (S/H) filtering effect at the input lower sampling rate, thus introducing an additional distortion in the overall response of a rational analog rate converter [4-6]. The recently proposed *L*-fold Impulse Sampled SC interpolators followed by an *M*-fold downsampler are appropriate for implementing such rational decimator without the input S/H effect [9-10]. Proposed in this paper is an even more efficient form of implementation which possesses less stringent speed requirements than before and which therefore is rather more economical from the viewpoint of power dissipation. Such implementation uses a new intermittent polyphase structure with double-sampled common delay blocks and with either *L* slow output accumulators or only *1* fast output accumulator.

II. INTERMITTENT POLYPHASE STRUCTURE WITH DOUBLE-SAMPLING

We first consider the design example of an FIR decimator with *200KHz* bandwidth and frequency downsampling from *2.5MHz* to *1.5MHz*. Thus, the rational conversion ratio is *L/M=3/5* and the stopband frequency must be *1.5MHz-200kHz=1.3MHz* (alias is allowed in the non-care transition bands). The resulting impulse response coefficients are given in the following table.

Table I : Impulse Response Coefficients of Rational Decimator

h_0, h_{10}	h_1, h_9	h_2, h_8	h_3, h_7	h_4, h_6	h_5
0.0335	0.1134	0.2334	0.3682	0.4753	0.5164

In a conventional impulse sampled rational decimator, the front stage *L*-fold interpolation filter produces *L* output interpolated samples during each input sampling period $1/f_s$, but the output downsampler keeps only every M^{th} such output samples, as shown in Fig.2. Thus, this suggests it is not necessary to compute all *L* interpolated outputs between input samples, but rather compute only those interpolated values that correspond to the output time grid.

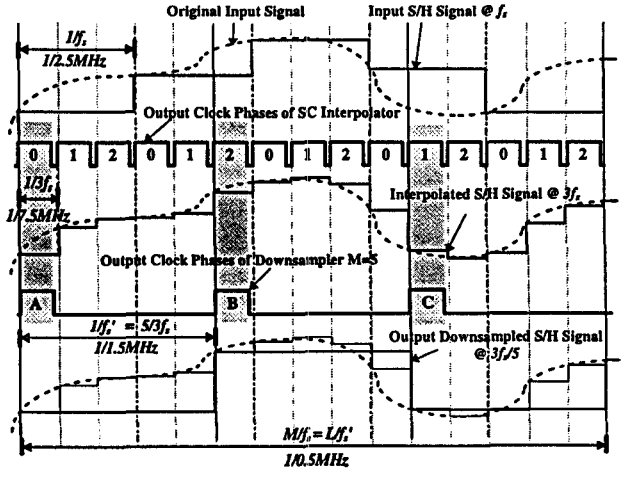

Fig.2 Input, Interpolated and Output Downsampled Signals in One Time Block for Rational Conventional Decimation of L/M=3/5

In other words, each polyphase filter operating at f_s in the interpolator produces one sample during the input sampling period at clock phase 0, 1 and 2. However, in the time block of M/f_s or L/f_s' the output downsampler samples each polyphase filter only once with the indices $m=0$, 2 and 1 at clock phase A, B and C, even though each polyphase filter has already generated 5 samples.

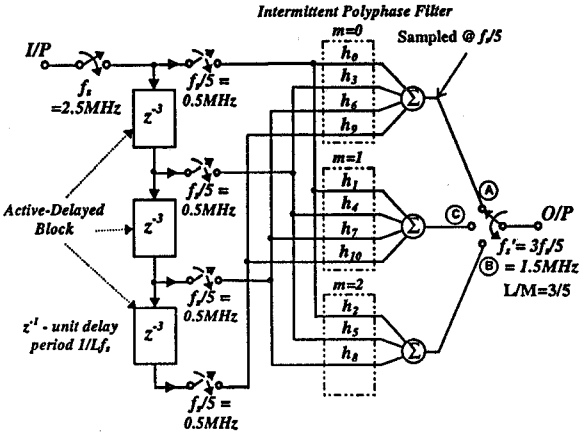

Fig.3 Intermittent ADB Polyphase Structures for Rational Decimation of L/M=3/5

The new efficient approach illustrated in Fig.3 ensures that each polyphase filter operates at $f_s/5$ for delivering only one sample during one time block, while in the remaining they are in an "idle" status, hence designated as intermittent sampling. Thus, the settling time for charge transfer in the accumulator will be extended to about one time block. Such distinguished feature also leads to an improvement of allowing the amplifier settling in SC ADB's to be increased to half of input sampling cycle [11].

The Double-Sampling Scheme (DSS) which will use both two clock phases as sampling phases is practical for high frequency applications because it doubles the frequency range of bi-phase SC filters by doubling the effective settling time of the amplifiers [12-13]. The adoption of this technique for realising SC ADB's is due to the fact that sampling time of SC branches in intermittent polyphase filters can be arranged flexibly in their long effective operation period M/f_s. Efficiency becomes obvious : the input and feedback/reset branches need only to be doubled in the double-sampled SC ADB but not in the intermittent polyphase filters since the amplifiers in accumulators are active during almost the whole effective period.

III. One Slow Output Accumulator for Each Intermittent Polyphase Filter

The corresponding SC realisation with its respective clock phases for intermittent polyphase structure of Fig.3 with double sampling has been illustrated in Fig.4.

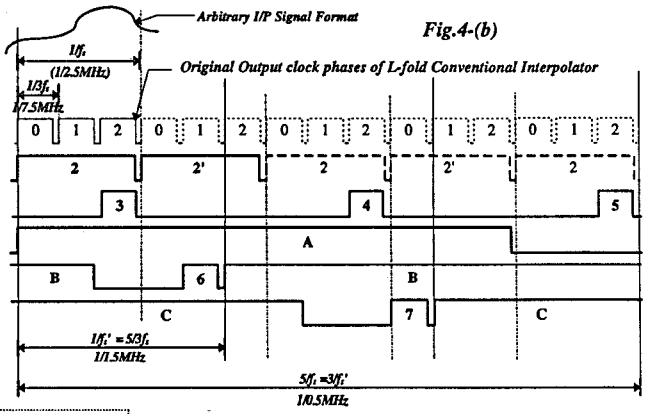

Fig.4-(b)

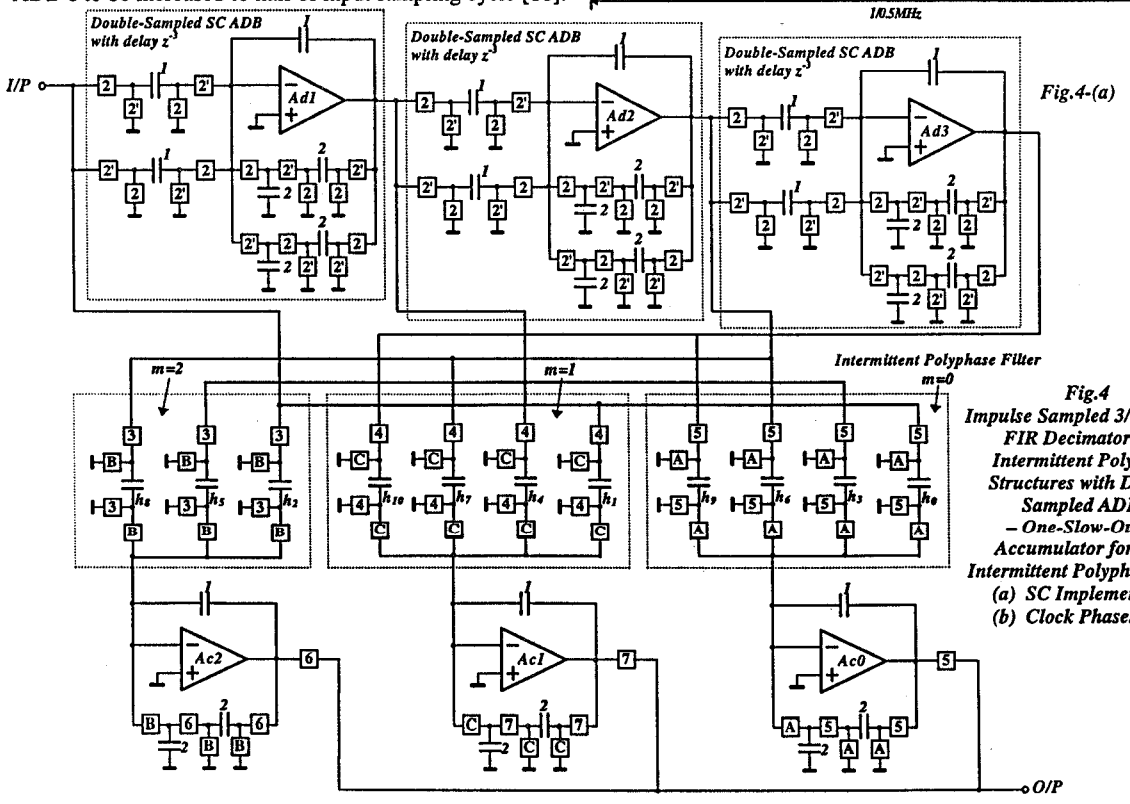

Fig.4-(a)

Fig.4 Impulse Sampled 3/5-fold SC FIR Decimator with Intermittent Polyphase Structures with Double-Sampled ADB's – One-Slow-Output-Accumulator for Each Intermittent Polyphase Filter (a) SC Implementation (b) Clock Phases

As shown in Fig.4, the input and feedback/reset SC branches are doubled for operation in the complementary phases in each of the upper *3* double-sampled SC ADB's which produce a series delay line for delaying every input sample to a full input sampling period z^{-L}. Since the double-sampled SC ADB's restrict to provide the settled output only at the end of every clock phase 2 and 2', the sampling instant of input SC branches in the intermittent polyphase filters must be constrained at the end of input sampling period, i.e. in phase 3, 4 and 5. The price for overcoming these constraints is the relative reduction of the output charge transfer time of accumulators. Therefore, the charge transfer time in ADB's is doubled to $1/f_s$, while the settling time in the output accumulator is $(ML-L)/Lf_s$ or even larger, i.e. settling time of the amplifier in polyphase filter $m=0$ can be extended to $(ML-1)/Lf_s$ because clock phase A needs to fall only before phase 5; and the settling time in filter $m=1$ becomes $(ML-2)/Lf_s$ due to the fact that the corresponding trailing edge of phase C can be shifted until the rising edge of sampling phase 4.

IV. One Fast Output Accumulator for L Intermittent Polyphase Filters

The previously mentioned structure takes advantage of slower amplifier in output accumulators and smaller total capacitance area. However, it needs L amplifiers, and its accuracy will be slightly affected by unavoidable parallel path mismatch problems. Then, a one-output-fast-accumulator structure becomes attractive since it needs less components and can reduce the nonideal mismatch property at the cost of relative increase in the total capacitance area and decrease of the charge transfer time to the output sampling period. There, each polyphase filter waits for its turn to transfer charge to the same output accumulator. The previous charges stored in the accumulator have to be reset when the next polyphase filter is activated, thus the longest charge transfer time of the amplifier is at most $1/f_s'=5/3f_s$ which is inherently longer than the input sampling period in the decimation process. The overall circuit architecture by employing one fast output accumulator with multi-reset/feedback SC branches is derived in Fig.5 with the corresponding clock phases.

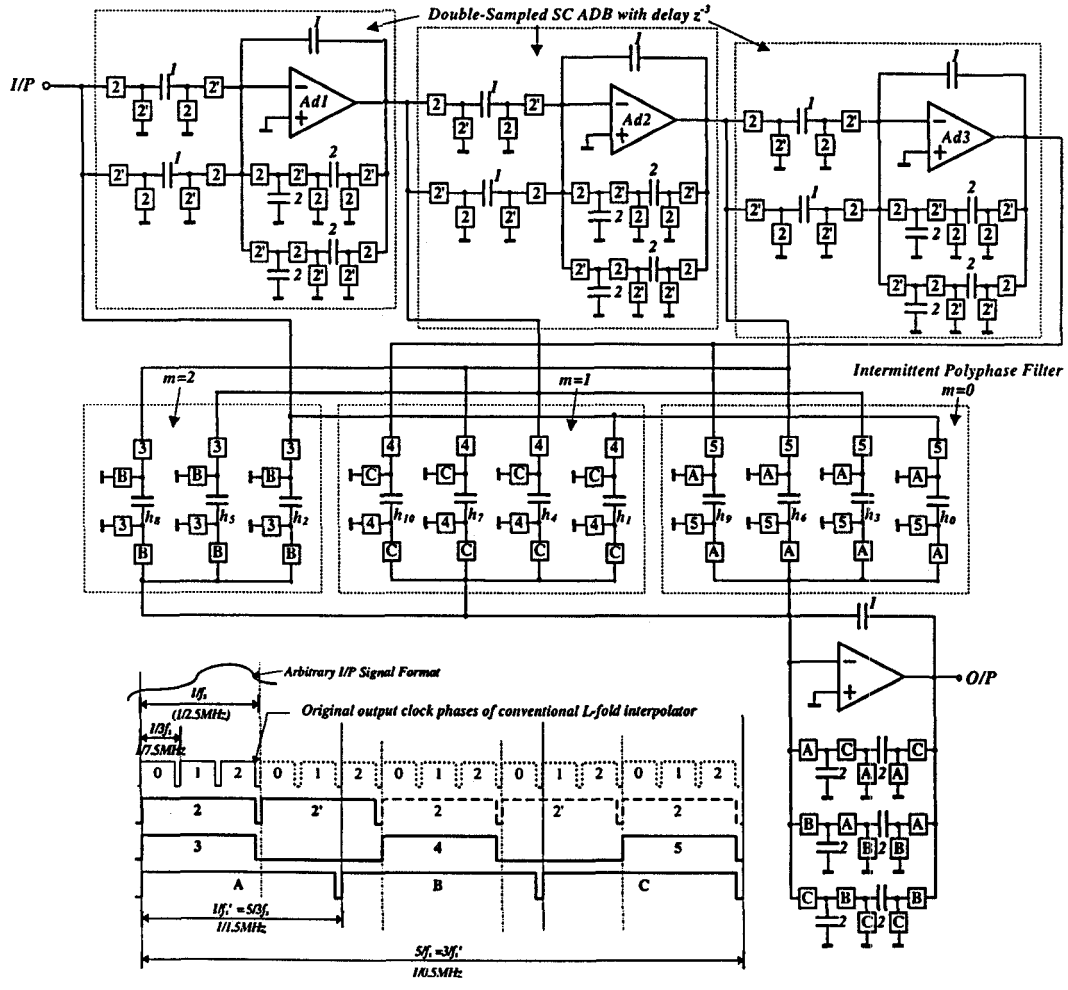

Fig.5 Impulse Sampled 3/5-fold SC FIR Decimator with Clock Phases in Intermittent Polyphase Structures with Double-Sampled ADB's – One Fast Output Accumulator for L Intermittent Polyphase Filters

V. Computer Simulated Results

For both circuit architectures presented before, the computer simulated results of the above rational decimator (coefficients in Table I) are provided in Fig.6. Curve I of Fig.6(a) is the overall amplitude response obtained with arbitrary input signal formats while curve II includes additional notch frequencies at multiples of output sampling rate *1.5MHz* due to the sole output S/H filtering effect. Since the input, intermediate and output sampling rates of such rational decimation are all different, for further investigation in the circuit operation, a spectrum analysis is also presented in Fig.6(b) and (c). The spectra of output decimated signals with the corresponding input signal frequency ranging from *DC* to *0.75MHz* in Fig.6(b) indicate that the frequency-translated image components replicate at the multiples of output sampling rate f_s'=*1.5MHz*. Furthermore, the detailed output spectra including the aliased components obtained with a *375kHz* input signal are also illustrated in Fig.6(c). For instance, the frequency translated imaging component at *2.875MHz* by sampling the original *375kHz* input signal at input rate f_s=*2.5MHz* has already been first attenuated by the interpolation filter to *-61.6dB* and then aliased into signal baseband by the output downsampling operation at *1.5MHz*, i.e. the aliased spectra at *125kHz* and *1.675MHz* are image components of *2.875MHz* at *3.0MHz* and *4.5MHz* respectively.

VI. Conclusions

Recently, proposed impulse sampled SC interpolators can be utilised for rational decimation with frequency responses no longer affected by additional distortion due to the input S/H filtering effect. To optimise the speed of operation of amplifiers, new efficient intermittent polyphase structures with double-sampled ADB's have been presented in this paper which are especially adequate to arbitrary rational sampling rate converters due to their enlarged effective operation period. Two extra branches are additionally needed in each double-sampled SC ADB for doubling the settling time of amplifiers to the full input sampling cycle, but the intermittent polyphase filters remain unchanged. Computer simulated results in terms of amplitude response and spectrum analysis have been obtained to verify the behaviour of such novel rational decimator.

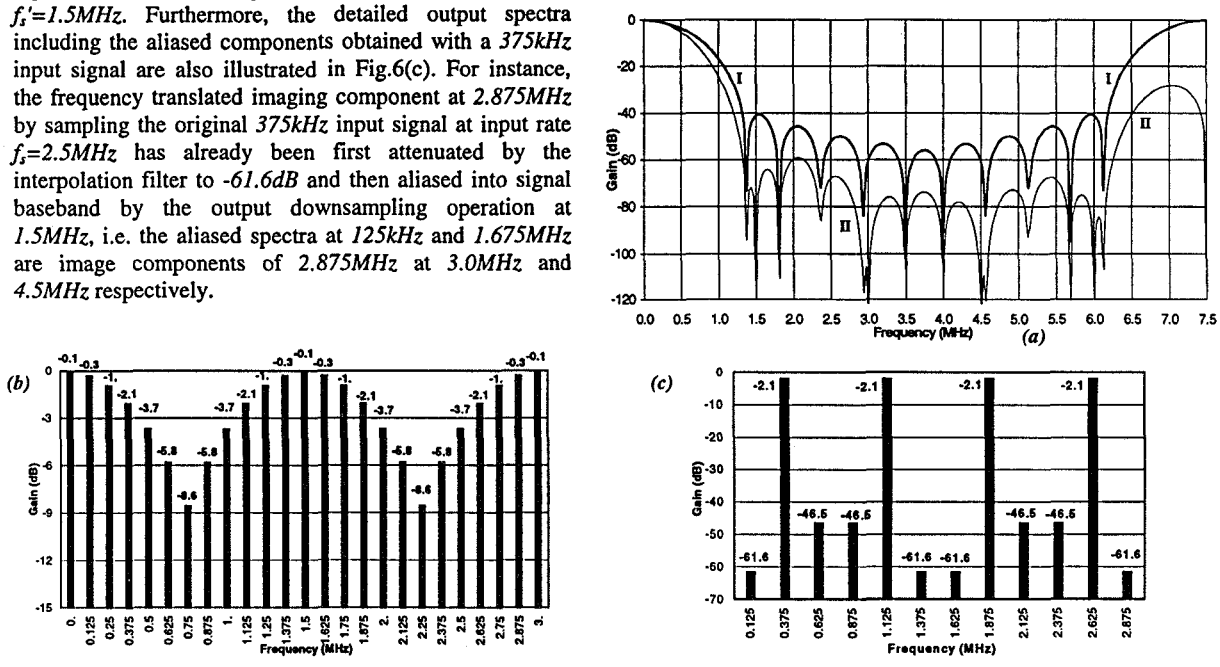

Fig.6 Computer Simulated Results of SC FIR Rational Decimator with Conversion Factor of L/M=3/5
(a) Overall Amplitude Response of Interpolation Filter
(b) Output Spectra with DC-0.75MHz Input Signals *(c) Output Spectra with a 375KHz Input Signal*

References

[1] R.E.Crochiere, L.R.Rabiner, *Multirate Digital Signal Processing*, Prentice-Hall, Inc., NJ, 1983.

[2] J.E.Franca, S.K.Mitra, A.Petraglia, "Recent Developments and Future Trends of Multirate Analog-Digital Systems," in *Proc. IEEE ISCAS'93*, pp.1042-1045, Chicago, USA, May 1993.

[3] R. Gregorian, W.E.Nicholson "Switched-Capacitor Decimation and Interpolation Circuits," *IEEE Trans. Circuits and Systems*, Vol.CAS-27, No.6, pp.509-514, Jun. 1980.

[4] J.E.Franca, "Non-recursive Polyphase Switched-Capacitor Decimators and Interpolators," *IEEE Trans. Circuits and Systems*, Vol.CAS-32, pp.877-887, 1985.

[5] R.P.Martins, J.E.Franca, "Infinite Impulse Response Switched-Capacitor Interpolators with Optimum Implementation," in *Proc. IEEE ISCAS'90*, Louisiana, USA, May 1990

[6] R.P.Martins, J.E.Franca, "Novel Second-Order Switched-Capacitor Interpolator," *Electronics Letters*, Vol.28, No.2, pp.348-350, Feb. 92.

[7] Gregory T. Uehara, Paul R. Gray, "Practical Aspects of High Speed Switched-Capacitor Decimation Filter Implementation" in *Proc. IEEE ISCAS'92*, USA, 1992.

[8] R.P.Martins, J.E.Franca, Franco Maloberti "An Optimum CMOS Switched-Capacitor Antialiasing Decimating Filter" *IEEE Journal of Solid-State Circuits*, Vol.28, No.9, pp.962-970, Sep. 1993.

[9] U Seng Pan, R.P.Martins, J.E.Franca, "Switched-Capacitor Interpolators Without the Input Sample-and-Hold Effect" *Electronics Letters*, Vol.32, No.10, pp.879-881, 9th May 1996.

[10] U Seng Pan, R.P.Martins, J.E.Franca, "Switched-Capacitor Finite Impulse Response Interpolators Without the Input Sample-and-Hold Effect" in *Proc. 1996 Midwest Symposium on Circuits and Systems*, pp.145-148, Ames, Iowa, USA. Aug. 18-21, 1996.

[11] U Seng Pan, R.P.Martins, J.E.Franca, "Intermittent Polyphase SC Structures for FIR Rational Interpolation," in *Proc. IEEE ISCAS'97*, pp.121-124, Hong Kong, Jun. 9-12, 1997.

[12] J.J.F.Rjins and H.Wallinga, "Spectral Analysis of Double-Sampling Switched-Capacitor Filters", *IEEE Trans. Circuits and Systems*, Vol.38, No.11, pp.1269-1279, 1991.

[13] A. Baschirotto, R. Castello, and F. Montecchi "IIR Double-Sampled Switched-Capacitor Decimators for High-Frequency Applications" *IEEE Trans. on Circuits and Systems*, Vol.CAS-I 39, No.4, pp.300-304, Apr. 1992.