

16.3 A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation

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Multi-GS/s ADCs are key blocks for ADC-based serial links and mm-wave 5G receivers. The fastest architecture is the flash ADC [1], but the exponentially growing complexity with resolution makes it energy and area inefficient. Interpolation techniques [2] can reduce the number of comparators but result in lower conversion speeds, while an aggressive interpolation factor in [3] also increases the calibration complexity. SAR ADCs are by far the most power efficient, but only with time interleaving can they reach the required speeds. Hence, pipelined architectures are the preferred choice, but also here clock speeds above 1GS/s are not readily achieved, and the power consumption of the residue amplifier is critical. Previous work [5] explores the option of the fully dynamic pipelined architecture, which only operates up to a relatively low sampling rate of 550MS/s (per channel) owing to its complex residue-transferring realization and calibration. In this work, the pipelined approach is revisited. Different from the conventional architecture that executes 3 serial operations (sampling, quantization and residue amplification) in one clock cycle, a post-amplification residue generation scheme is presented that allows the amplification and conversion to run in parallel. Leveraging a linearized dynamic amplifier and on-chip gain and offset calibration, the prototype achieves 34.2dB SNDR with a Nyquist input at 3.3GS/s. The 6b ADC consumes 5.5mW and 0.0166mm² (including calibration), leading to a Walden FoM of 40fJ/conv.-step.

As illustrated in Fig. 16.3.1, the prototype ADC utilizes a simple architecture consisting of six 1b stages without backend flash, aggregating 6b resolution. Unlike the classical pipeline stage where the amplification must wait for the quantizer decision and the DAC feedback, in this work the reference subtraction is performed at the DAC of the next stage after signal amplification as in [6]. Instead of amplifying the residue, the full signal is amplified, and afterwards a correspondingly larger DAC reference is subtracted to create the desired pipeline residue. With the proposed arrangement, the comparator and residue amplifier (RA) in the same stage can be triggered in parallel. At the falling edge of ϕ_s , stage[N] ends its tracking phase and enters hold mode. Simultaneously, the quantization result from stage[N-1] is set up and fed to the DAC, generating the residue in stage[N] with a proper feedback voltage. After the corresponding DAC switching settles, the quantizer and amplifier in stage[N] are triggered together. In this configuration, the amplifier amplifies the sampled input of the current stage rather than the residue, unlike in the conventional counterpart. In parallel with the quantization and amplification in stage[N], the output of the current stage amplifier is sampled in stage[N+1] during ϕ_a . Concurrently, the quantization result D[N] is fed to DAC[N+1] to generate the amplified version of residue[N] in stage[N+1], and the procedure is repeated in each stage. The proposed parallelized operation accelerates overall speed by allowing each stage to accommodate only two basic operations—sampling and conversion/amplification, thereby reducing idle time for high-speed pipeline operation.

As the amplifier needs to interface with a larger input signal, its linearity becomes critical. The dynamic amplifier (DA) is used due to its good power efficiency, but its conventional implementation suffers from relatively poor linearity for large input swings. Such nonlinearity is mainly originated by the differential current ($I_{D1} - I_{D2}$) failing to linearly follow the input as described by eq. 1 in Fig. 16.3.2, which shows that the differential current doesn't increase proportionally to the input amplitude due to a nonlinear term. While a time-domain scheme [4] demonstrates a promising linearized result, it is not applicable to high-speed designs due to its relatively large delay (20~30ps), originating from the adaptive common-mode detection circuit. Therefore, a current-based linearization technique is proposed as shown in Fig. 16.3.2. On top of the basic DA structure, an auxiliary pseudo-differential input pair $M_3 - M_4$ is added in parallel, which shares the same main clock through M_5 and M_6 , providing the compensation currents I_{D1Aux} & I_{D2Aux} , as depicted in Fig. 16.3.2. According to the square-law model, the summation of I_{D1Aux} and I_{D2Aux} is approximately a constant plus a 2nd-order term ($V_{i+}^2 + V_{i-}^2$), which is used to partially compensate the nonlinearity following eq. 2

in Fig. 16.3.2. Together with source degeneration (RD_1 & RD_2), simulation results show that the proposed DA can maintain a relatively high and flat G_m across a large input swing, leading to a 16dB SFDR improvement in this design and allowing an amplification time under 80ps. The linearized DA with 1.5 \times gain is only used in the first two stages, while a conventional DA with 2 \times gain is used in the remaining stages for lower input capacitance and better CMRR. The small inter-stage gain (1.5 \times / 2 \times) also ensures the enlarged references are still within supply.

To save power, the offset and gain of all stages are foreground-calibrated on-chip (Fig. 16.3.3). During calibration, the differential inputs are shorted, and the comparator offsets are tuned through calibration voltages (V_{cal}) from a dedicated R2R DAC with an auxiliary input pair. This offset calibration is done one-comparator at a time and the comparator decisions are determined by an 8-time majority voting logic. The adjustment of V_{cal} stops when an equal probability of ones and zeros is reached. After compensation of the comparator offsets, the RAs undergo a similar calibration scheme, but with offset compensated by a tunable loading, which avoids any calibration-induced interference on the RA gain and linearity. The stage[N] comparator is used to observe the offset of the stage[N-1] RA and the offset of the latter is tuned by adding/removing capacitors in a 6b capacitor bank (Cbank). The references in each stage are matched by the RA gain, which is controlled by a digital tunable amplification time. The inter-stage gains are calibrated from the last to the first stage. To detect the gain of stage[N], with nulled offsets in comparator and amplifier, a half-LSB voltage is generated in the DAC of stage[N]. Then, it is amplified and quantized by the current and/or subsequent stages. The quantization result D[N:5] is ideally $2^{(6-N)} - 1$, which is the full-scale of stage[N] to stage[5]. The calibration starts with a minimum gain configuration and increases the gain until D[N:5] reaches its target. As the output common-mode of the DA has a strong correlation with the gain, such calibration also ensures proper internal common-mode values.

The ADC, fabricated in 28nm CMOS, with ~40fF input capacitance (excluding ESD), occupies an active area of 0.0166mm², including on-chip calibration circuits (Fig. 16.3.7). During measurements, the foreground on-chip calibration is performed, and the obtained values are frozen throughout all measurements. Figure 16.3.4 plots the measured SFDR/SNDR and power vs. input frequency at 3.3GS/s, and vs. power supply (sample #2), as well as the Nyquist performance at 3.3GS/s for 3 randomly selected samples. The prototype consumes a purely dynamic power, which can be recognized by the linear proportional relationship between the power and clock frequency with a slope of 1.5 μ W/MHz. SNDR is 34dB up to 3.5GHz (2.12 \times Nyquist) and drops 1dB from 3.5GHz to 6GHz. With a fixed calibration set obtained at 0.9V supply and no re-cal., the SNDR degrades less than 3dB for a \pm 5% supply change. Figure 16.3.5 illustrates the measured spectrum (decimated by 225) at 3.3GS/s for a Nyquist 1.649GHz input, w/ and w/o calibration. Measured DNL and INL after calibration are +1.08 / -0.85 LSB, +1.11 / -1.04 LSB for a 6.25mV LSB. Figure 16.3.6 compares the design with ADCs above 2GS/s, indicating this work achieves state-of-the-art FOM_w.

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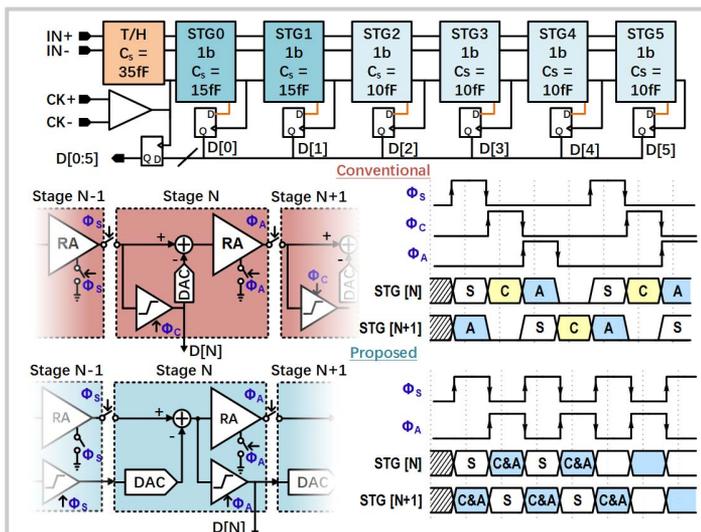
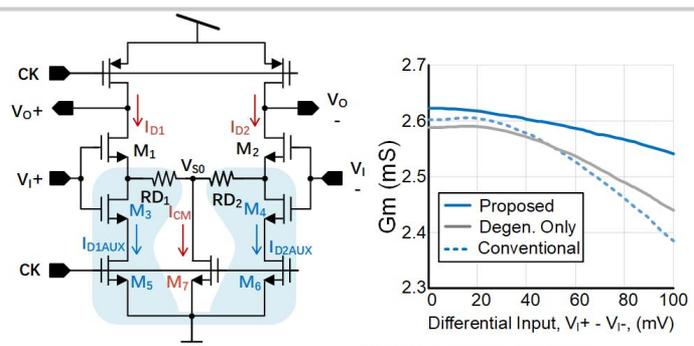


Figure 16.3.1: ADC Architecture (top) and conventional (middle) and proposed (bottom) pipelined stages.



Conventional :

$$I_{D1} - I_{D2} = k(V_{I+} - V_{I-}) \sqrt{\frac{4(I_{CM})}{k} - (V_{I+} - V_{I-})^2} \quad (eq. 1)$$

Proposed :

$$I_{D1} - I_{D2} = k(V_{I+} - V_{I-}) \sqrt{\frac{4(I_{CM} + c + \alpha k_1(V_{I+}^2 + V_{I-}^2))}{k} - (V_{I+} - V_{I-})^2} \quad (eq. 2)$$

Compensation for 2nd order terms from auxiliary path

$$I_{D1AUX} + I_{D2AUX} = c + \alpha k_1(V_{I+}^2 + V_{I-}^2)$$

Figure 16.3.2: Proposed linearized dynamic amplifier.

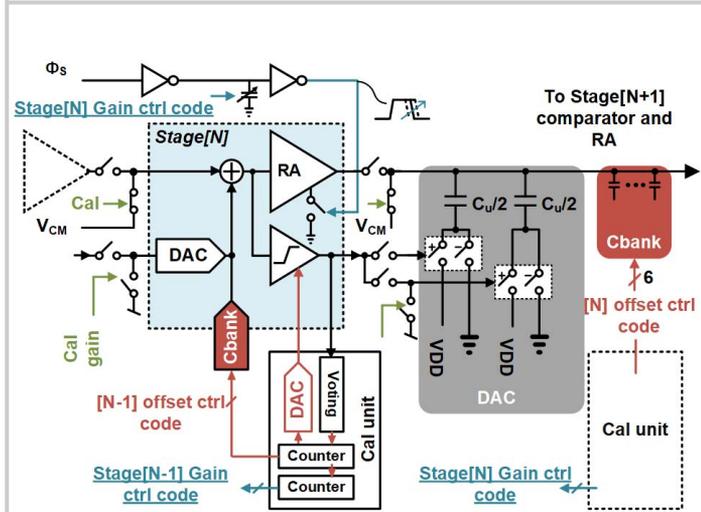


Figure 16.3.3: Detailed architecture of the proposed pipelined stage.

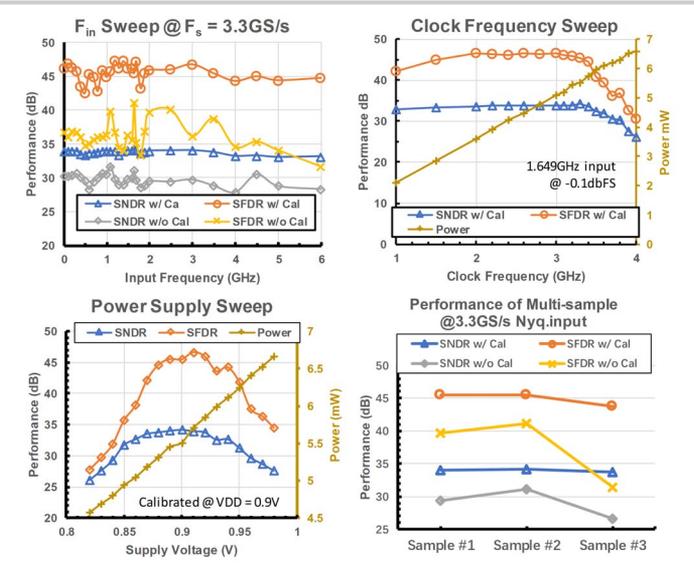


Figure 16.3.4: Measured performance.

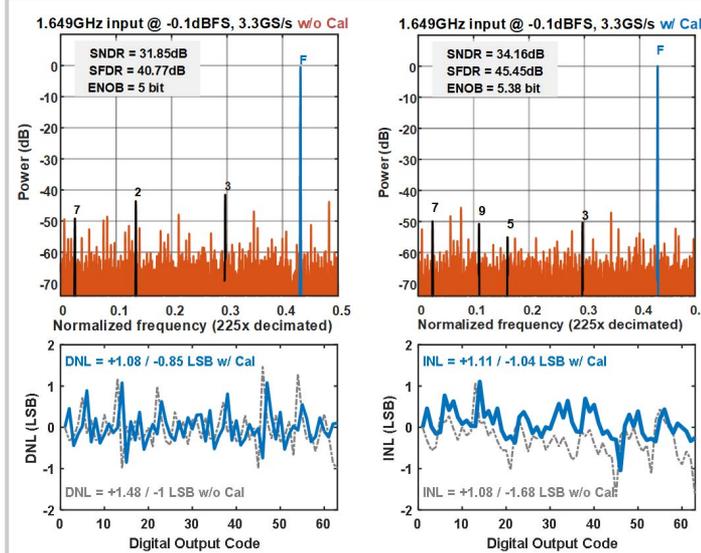


Figure 16.3.5: Measured spectrum and DNL/INL.

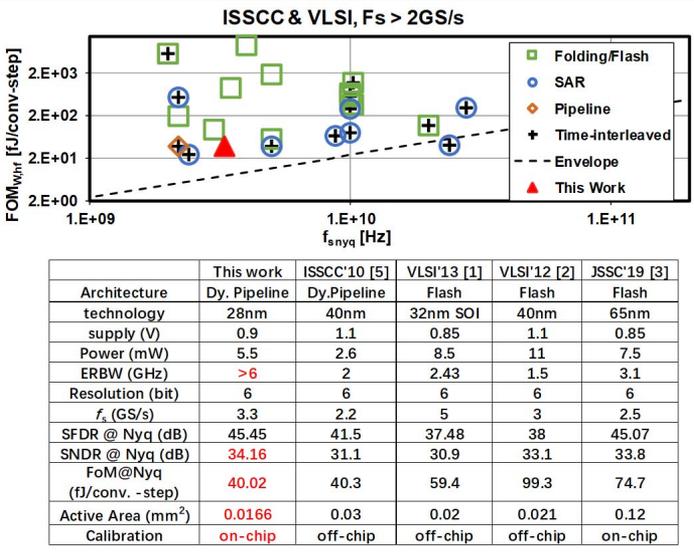


Figure 16.3.6: Comparison with state-of-the-art.

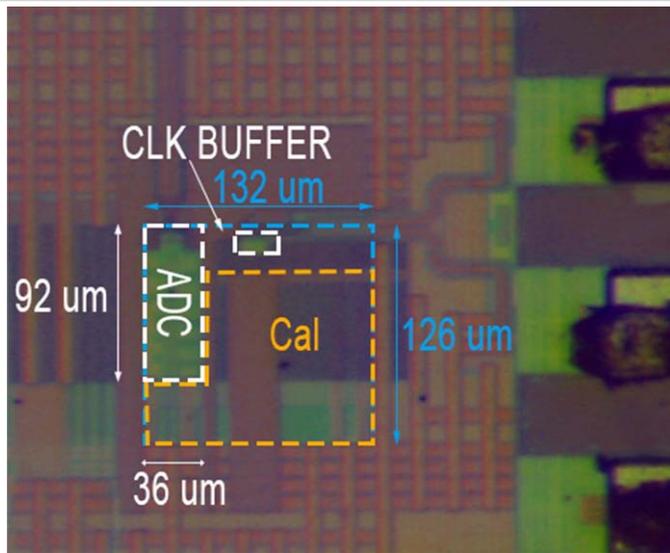


Figure 16.3.7: Die photo.

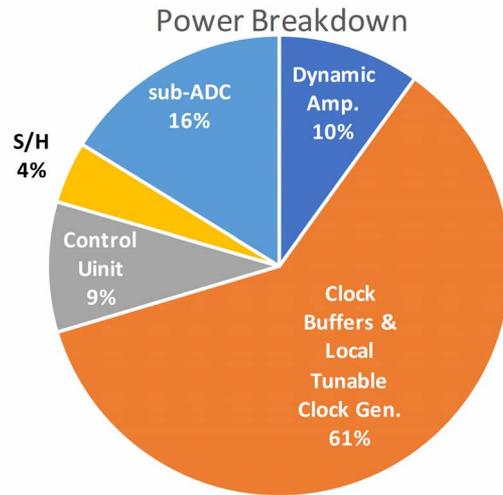


Figure 16.3.S1: Power breakdown.

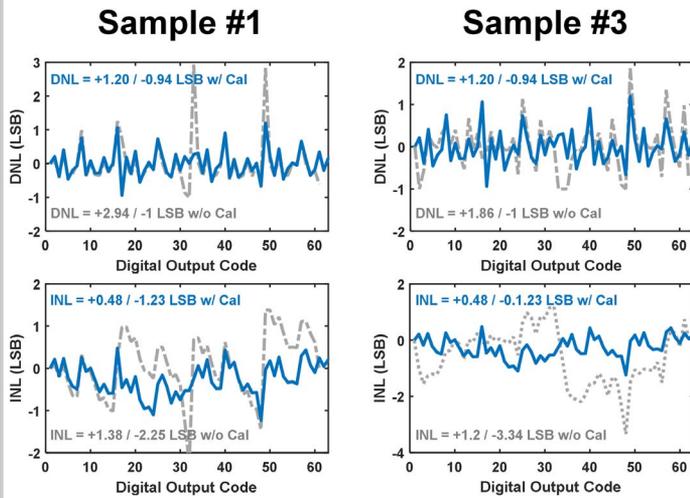


Figure 16.3.S2: Measured DNL of sample #1 and sample #3.

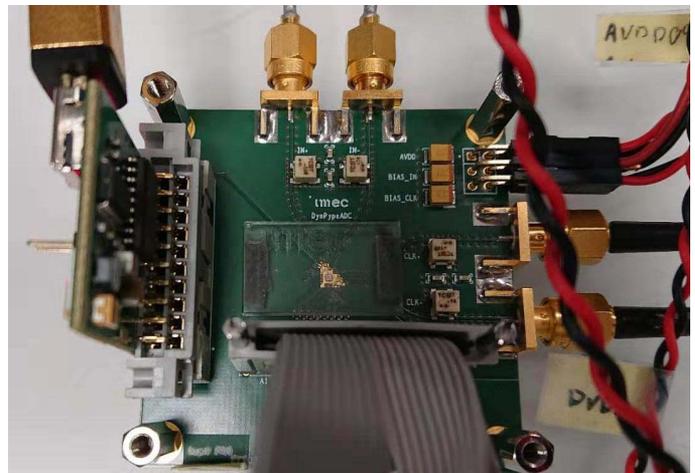


Figure 16.3.S3: Measurement setup.