A Fast-Transient-Response Fully-Integrated Digital LDO with Adaptive Current Step Size Control

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***Abstract*—A 0.6-V 100-mA fully-integrated digital low-dropout regulator (DLDO) with adaptive current step size control is presented in this paper. By dividing the main power PMOSs into ten blocks with different unit-cell sizes, the proposed DLDO can turn-on/-off small power PMOSs in light load and large ones in heavy load conditions. High regulation accuracy in a wide load range and fast transient response are hence achieved. In addition, an auxiliary power MOS block, which consists of both PMOS and NMOS transistors, is adopted to eliminate the limit cycle oscillation (LCO) in light load condition and to further accelerate the response speed. The proposed DLDO is fabricated in a 65-nm low-power CMOS technology with an active area of 0.17 mm^2 including an on-chip output capacitor of 1nF. The measured undershoot and overshoot voltages are only 53 mV and 37 mV, respectively, when the load current changes between 0 and 100 mA. The quiescent current is 34.6 µA, while the maximum current efficiency is 99.96%.**

Keywords—digital low-dropout regulator (DLDO), adaptive current step size control, wide load range, fully-integrated, fast transient response.

I. Introduction

Low-dropout regulators (LDOs) are widely used in system-on-a-chip (SoC) designs for its small voltage ripple, fast transient response, small area requirement and low cost. Recently, energy-efficient digital circuits are designed with near-/sub-threshold supply voltage to reduce the power consumption. However, low supply voltage brings design challenges to the traditional analog LDO (ALDO) that consists of analog amplifiers. Meanwhile, shrinking the channel length and gate-oxide thickness in advanced CMOS technology greatly increases the design difficulty of analog circuits. Therefore, digital LDO (DLDO) was proposed to be an alternative solution [1], and has attracted enormous attentions. However, many existing DLDOs suffer from a limited load current range [1-4], or demand a large decoupling capacitor [5-6], limiting their applications. Techniques such as reduced dynamic stability [2], event-driven control [4] and burst mode technique [5] have been proposed to improve the transient response, but the effects are not optimal. The analog-assisted loop scheme in [7] reduces the output variation when the load current changes from 2 to 12 mA, but is not very effective for a small initial load current.

In this paper, we present a fully-integrated DLDO with adaptive current step size control. It achieves wide load range, good regulation accuracy and fast transient response without using large quiescent current. In addition, the limit cycle oscillation (LCO) in light load is alleviated and even eliminated without a large dead-zone. The working principle and circuit implementation of the proposed DLDO are discussed in Section II. Section III shows the measurement results and Section IV draws the conclusion.

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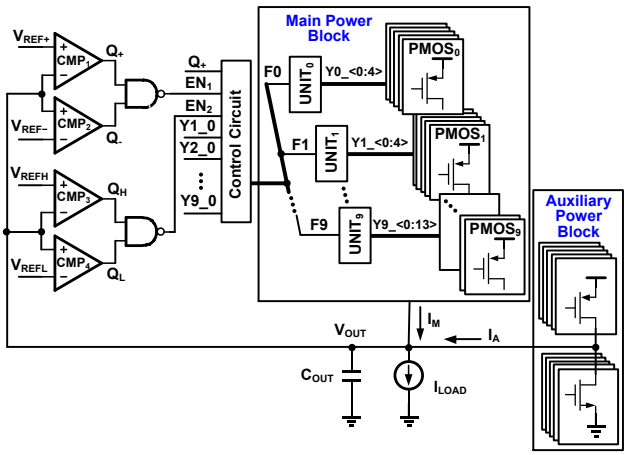

Fig. 1 Block diagram of the proposed DLDO.

II. Operation Principle and Circiut Implementation

A. Operation Principle

DLDO turns on/off one or more power MOSs per clock cycle to charge/discharge the output voltage V_{OUT} to make it close to the reference voltage V_{REF}. However, turning-on/-off the same power MOS in different load conditions has different effects on V_{OUT}. Specifically, turning-on/-off small-size power MOSs is fine in light load but has small effect in heavy load, which affects the regulation speed. On the other hand, turning-on/-off large-size power MOSs is OK in heavy load but may lead to limit cycle oscillation (LCO) and stability problems in light load. Therefore, we propose to use adaptive power MOS sizes per load conditions.

Fig. 1 shows the block diagram of the proposed DLDO, which consists of 4 comparators, a control circuit, a main power block, an auxiliary power block, and an output capacitor C_{OUT}. Among the four reference voltages, $V_{REF+} = V_{REF} + \Delta V_1$, $V_{REF-} = V_{REF} - \Delta V_1$, $V_{REFH} = V_{REF} + \Delta V_2$ and $V_{REFL} = V_{REF} - \Delta V_2$, and $\Delta V_1 < \Delta V_2$. When V_{OUT} runs out of the range of [V_{REF-} : V_{REF+}], signal EN_1 is set to 1, otherwise $EN_1 = 0$. Similarly, When V_{OUT}

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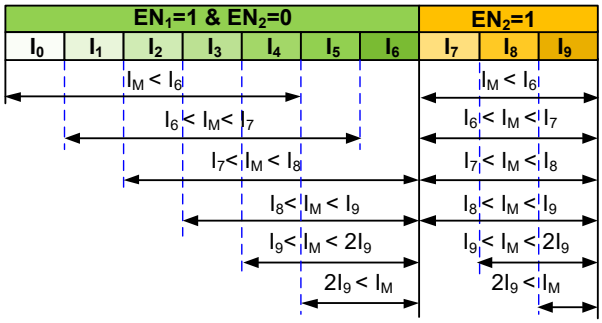

Fig. 2 Available current step sizes in different load condition and current step sizes selecting strategy.

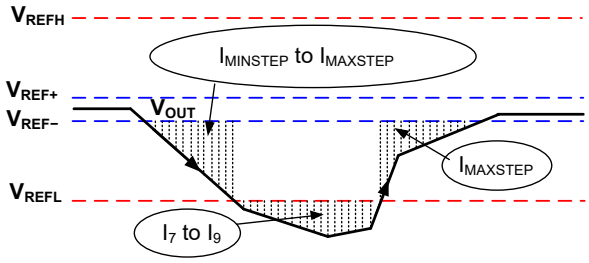

Fig. 3 Illustration of current step size selecting strategy.

is not within the range of [V_{REFL} : V_{REFH}], meaning that a large overshoot/undershoot is detected, signal EN_2 is set to 1, otherwise $EN_2 = 0$. Only two comparators CMP1 and CMP2 are active at steady state, i.e., when $V_{REF-} < V_{OUT} < V_{REF+}$ and $EN_1 = 0$, while other blocks are in freeze mode , which significantly reduces quiescent current consumption. In the main power block, the power PMOSs are divided into 10 sub-blocks $PMOS_0$ to $PMOS_9$ with different sizes. The unit current relationship between the power blocks is that $I_X = 2I_{X-1}$ ($0 < X \leq 9$). Furthermore, in this design, there are 5 power PMOS transistors in each block of $PMOS_0$ – $PMOS_8$ blocks and 14 power PMOS transistors in the $PMOS_9$ block, to achieve a high-resolution control. The auxiliary power block consists of 5 power PMOS transistors and 5 power NMOS transistors, directly controlled by the comparator outputs.

Fig. 2 shows the available current step sizes and step size selecting strategy based on V_{OUT} and the supply current of the main power block I_M, which equals to the load current I_{LOAD} in steady state. The current step sizes are divided into two parts according to the deviation of V_{OUT}. $I_0 – I_6$ are for $EN_1 = 1$ & $EN_2 = 0$, and $I_7 – I_9$ are for $EN_1 = 1$ & $EN_2 = 1$, i.e., small current step sizes for small voltage deviation and large current step sizes for large voltage deviation. In addition, the available current step sizes are also controlled by current status of I_M, as discussed previously, small current step sizes are preferred in light load while large ones in heavy load. For example, when $I_M < I_6$, the minimum current step size $I_{MINSTEP}$ is I_0 and the maximum current step size $I_{MAXSTEP}$ is I_4 for $EN_1 = 1$ & $EN_2 = 0$ and $I_{MINSTEP} = I_7$ and $I_{MAXSTEP} = I_9$ for $EN_2 = 1$. When $I_9 < I_M < 2I_9$, for $EN_1 = 1$ & $EN_2 = 0$, $I_{MINSTEP}$ is I_4 because small current steps like I_0, I_1 etc. have negligible effect on charging/discharging V_{OUT} back to [V_{REF-} : V_{REF+}]. In the same way, $I_{MINSTEP}$ is I_8 for $EN_2 = 1$.

Fig. 3 illustrates the current step size selecting strategy. When $EN_1 = 1$, the step size will increase from $I_{MINSTEP}$ to

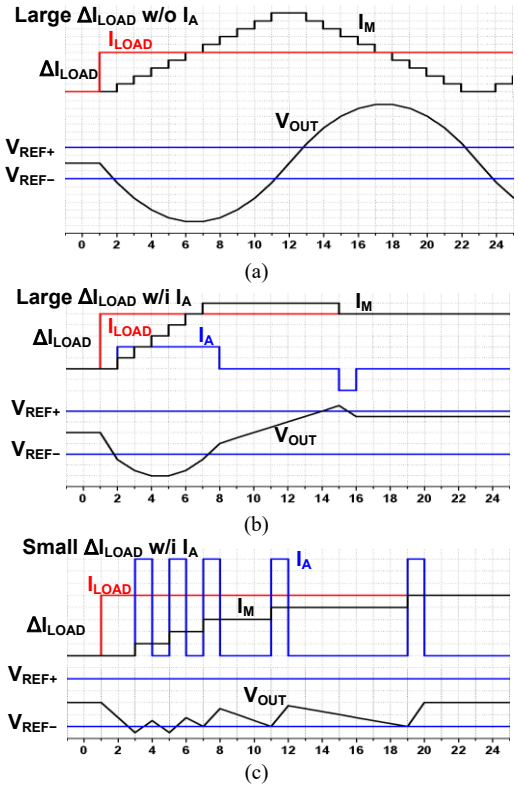

Fig. 4 V_{OUT} response (a) large ΔI_{LOAD} without I_A; (b) large ΔI_{LOAD} with I_A and (c) small ΔI_{LOAD} with I_A.

$I_{MAXSTEP}$ until V_{OUT} returns to [V_{REF-} : V_{REF+}]. When $V_{OUT} < V_{REFL}$ or $V_{OUT} > V_{REFH}$, $I_7 – I_9$ will be selected to recover V_{OUT}. After that, $I_{MAXSTEP}$ will be used to quickly and efficiently charge/discharge V_{OUT} back to [V_{REF-} : V_{REF+}] without over charge or over discharge. For example, when $I_M < I_6$, at the beginning, I_0 is chosen to charge/discharge V_{OUT} back to [V_{REF-} : V_{REF+}]. If in the next clock cycle, V_{OUT} remains in $V_{REFL} < V_{OUT} < V_{REF-}$ or $V_{REF+} < V_{OUT} < V_{REFH}$, then a larger current step size I_1 is chosen, and then I_2, I_3, I_4, until $V_{REF-} < V_{OUT} < V_{REF+}$. Therefore, the current step size sequence might be $I_0 \rightarrow I_1 \rightarrow I_2 \rightarrow I_3 \rightarrow I_4 \rightarrow I_4 \rightarrow \ldots$ For another example, if V_{OUT} goes beyond the range of [V_{REFL} : V_{REFH}] in the 3rd cycle and returns back in the 5st cycle, then the step size sequence might be $I_0 \rightarrow I_1 \rightarrow I_7 \rightarrow I_8 \rightarrow I_6 \rightarrow I_6 \rightarrow \ldots$ Notice that, since $I_8 < I_M < I_9$ after turning on one $PMOS_7$ and one $PMOS_8$, $I_{MAXSTEP}$ is set to be I_6. With the adaptive current step size control, the transient speed can be effectively increased without requiring large quiescent current or compromising the stability.

Moreover, an auxiliary power block is employed in the proposed DLDO to accelerate the regulation speed and alleviate and even eliminate LCO in light load condition. When V_{OUT} runs out of the range of [V_{REF-} : V_{REF+}], not only the main power block will act but also the auxiliary power block will offer an additional current I_A to speed up charging/discharging V_{OUT} back to [V_{REF-} : V_{REF+}].

Fig. 4 illustrates how I_A helps to reduce the undershoot and eliminate LCO in light load. In fig. 4 (a), when the load current I_{LOAD} increases by large ΔI_{LOAD}, V_{OUT} drops until $I_M \geq I_{LOAD}$. However, I_M has to keep increasing to charge V_{OUT} back to [V_{REF-} : V_{REF+}], which may cause overshoot in turn and lead to

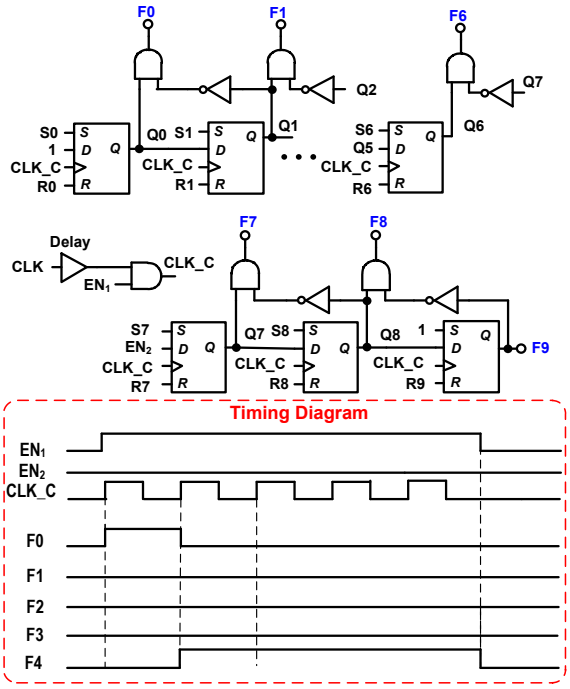

Fig. 5 Simplified schematic of the control circuit and timing diagram.

LCO problem. The key reason of the LCO problem is that V_{OUT} cannot be charged/discharged to $V_{REF-} < V_{OUT} < V_{REF+}$ when $I_M = I_{LOAD}$. Therefore, an additional current I_A is used to prevent it. As shown in Fig. 4 (b), with the help of I_A, V_{OUT} is pulled back to [V_{REF-} : V_{REF+}] faster than that without I_A. The overshoot/ undershoot are alleviated and V_{OUT} stabilized after a few cycles. For the case of small ΔI_{LOAD} shown in Fig. 4 (c), each time V_{OUT} deviates from the range of [V_{REF-} : V_{REF+}], I_A will charge V_{OUT} back immediately and I_M increases by $I_{MINSTEP}$. To avoid I_A overcharging V_{OUT} from $V_{OUT} < V_{REF-}$ to $V_{OUT} > V_{REF+}$ within one clock cycle in light load, the initial value of I_A is limited to $I_A < \Delta V_1 C_{OUT} f$, where f is the clock frequency. In heavy load, there is no LCO problem and the transient speed is fast enough, hence the auxiliary power block will be disabled.

Considering the additional current supplied by auxiliary power block, the current size choosing strategy can be further improved. When the additional current I_A cannot charge/ discharge V_{OUT} back to [V_{REF-} : V_{REF+}] within one clock cycle, which means that $\Delta I_{LOAD} \times 2T > I_A \times T$, or $\Delta I_{LOAD} > I_A/2$, , the second current step size can be set to close to $I_A/2$, rather than increasing it one by one. For example, when $I_M < I_6$, in this design, $I_A/2 \approx I_4$, the current step size sequence is set to be $I_0 \rightarrow I_4 \rightarrow I_4 \cdots$, while the former current step size sequence is $I_0 \rightarrow I_1 \rightarrow I_2 \rightarrow I_3 \rightarrow I_4 \cdots$. The regulate speed is improved by this current step size boost.

B. Circuit Implementation

Fig. 5 shows the simplified control circuit used to select the current step size, which is a DFF-based unidirectional shift-register (SR). Fn = 1 means I_n is selected in this clock cycle. The set signal Sn and reset signal Rn of each DFF is determined by EN_1, EN_2, and I_M. As we can see in Fig. 5, with the step size burst, F4 will be set to 1 at the 2nd clock, indicating a current step size sequence of $I_0 \rightarrow I_4 \rightarrow I_4 \cdots$. Fig. 6 shows a simulated step size

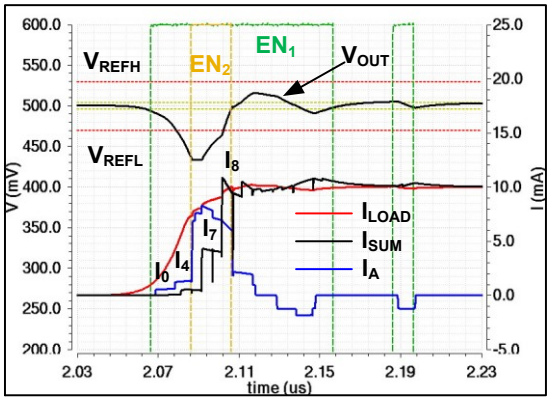

Fig. 6. Simulated current step size sequence with I_{LOAD} changes from 0 to 10 mA.

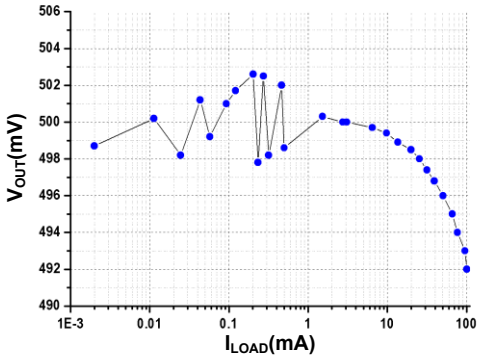

Fig. 7 Measured load regulation.

sequence for example when I_{LOAD} has 10 mA step up, the current step size sequence is $I_0 \rightarrow I_4 \rightarrow I_7 \rightarrow I_8 \cdots$. Quick recovery of V_{OUT} is achieved due to the fast size sequencing.

The UNIT block used to control the power transistors in each PMOSn block is a bidirectional SR. A CLKn generator is used to generate a pulse in the falling edge of CLK for carry and borrow operation. In this design, I_A increases step by step when $EN_1 = 1$ to effectively charge/discharge V_{OUT} back to [V_{REF-} : V_{REF+}]. Furthermore, one standby clock period is inserted to avoid turning on a PMOS (NMOS) right after turning off a NMOS (PMOS).

III. Measurement Results

The proposed DLDO is fabricated in a 65-nm low-power CMOS process. V_{OUT} is regulated to 0.5 V with a 0.6 V V_{IN}. Operating at a clock frequency of 100 MHz, the quiescent current is 34.6 µA with a maximum load current of 100 mA, achieving a peak current efficiency of 99.96%. As shown in Fig. 7, the proposed DLDO achieves good load regulation over a wide load range. In practice, V_{REF+}, V_{REF-}, V_{REFH} and V_{REFL} can be calibrated to accommodate for the comparators' offset voltages. In this design, $\Delta V_1 = 5$ mV, and V_{OUT} is regulated to the range of [495 mV : 505 mV]. The DC voltage drop in heavy load is mainly due to the IR drop on the bonding wire parasitic resistor. Fig. 8 and Fig. 9 show the measured load transient responses with ΔI_{LOAD} of 100 mA and 18 mA, respectively. With the adaptive current step size control and auxiliary current I_A, the undershoot and overshoot are 53 mV and 37 mV, respectively, for the 100 mA ΔI_{LOAD} case. Moreover, the LCO

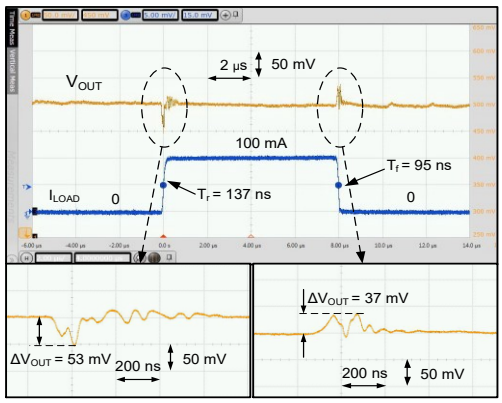

Fig. 8 Measured load transient response with load current changes between 0 and 100 mA.

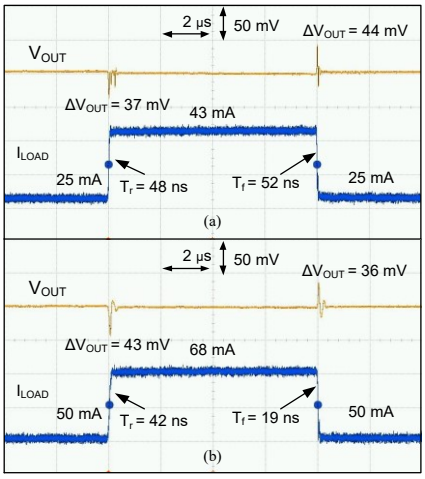

Fig. 9 Measured load transient response with I_{LAOD} changes between (a) 25 mA and 43 mA and (b) 50 mA and 68 mA.

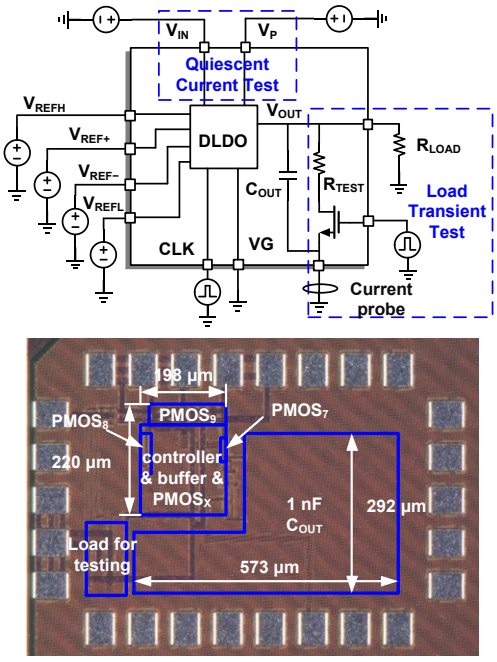

Fig. 10 Measurement setup and chip micrograph.

TABLE I PERFORMANCE COMPARISON WITH PRIOR-ARTS

	[3] 2018	[4] 2017	[5] 2018	[6] 2017	**This work**
Technology (nm)	65	65	40	40	**65**
V_{IN} (V)	0.5-0.9	0.45-1	0.6-1.1	0.6-1.1	**0.6**
V_{OUT} (V)	0.3-0.8	0.4-0.95	0.5-1	0.5-1	**0.5**
$I_{LOAD(MAX)}$ (mA)	3.3	3.356	20	210	**100**
I_Q (µA)	48.4	8.1-258	9.2	22.6-98.5	**34.6**
Peak current efficiency (%)	99.3	99.2	99.8	N/A	**99.96**
ΔI_{LOAD} (mA)	3.25	1.44	19	200	**100**
Edge time Δt(ns)	< 0.2	N/A	400	1000	**137**
C_{OUT} (nF)	0.365	0.1	4.7	20	**1**
ΔV_{OUT} (mV)	20.5	34	40	36	**53**
FOM_1 (pF)	0.16	0.064	0.19	0.16	**0.037**
FOM_2 (ps)	36.9	20	5.21	11	**0.183**

$$FOM_1 = \frac{I_Q}{\Delta I_{LOAD}} \cdot \frac{\Delta V_{OUT}}{V_{OUT}} \cdot C_{OUT} \; ; \; FOM_2 = \frac{I_Q}{\Delta I_{LOAD}} \cdot \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} \cdot C_{OUT}$$

in light load is eliminated. Fig. 10 shows the measurement setup and chip micrograph. The DLDO takes an active area of 0.17 mm^2, including the 1nF C_{OUT} (the core takes 0.044 mm^2). Table I compares the proposed DLDO with state-of-the-arts. Thanks to the adaptive step control scheme, the proposed DLDO achieves 0.037-pF FOM_1 and 0.183-ps FOM_2 which are the smallest among the designs.

IV. CONCLUSION

A 100-mA fully-integrated DLDO with adaptive current step size control for accurate and fast regulation has been presented. A current step size selecting strategy based on I_M and V_{OUT} is developed to achieve high accuracy and fast transient responses. In addition, LCO in light load is alleviated and even eliminated, and the transient speed is further enhanced by the auxiliary power block without degrading system stability, while consuming small quiescent current. The proposed DLDO achieves the smallest FOMs among the published ones.

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