Design of a Low-Power Low-Noise Bio-Potential Readout Front-End in CMOS

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***Abstract*—In modern clinical applications, Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG) waves are normally recorded by massive and power-hungry instruments. In order to enhance the portability of bio-potential signal measurements, in this paper, we describe the design and implementation of a low-power and low-noise bio-potential signal readout front-end (RFE). Designed in 90-nm CMOS with thick-oxide transistors, the RFE consists of an instrumentation amplifier (IA) with both chopper and AC-coupling techniques for: dc-offset removals; filtering the transistors' flicker noise and boosting the CMRR. Following the IA there is a spike filter, which is clocked accurately to suppress the chopping spikes. The final stage is a gain-bandwidth-controllable amplifier, which further boosts the gain and enables different bio-potential signal measurements through simple digital controls. Simulation results showed that the RFE can successfully eliminate the differential electrode offset up to ±50 mV, while achieving 140-dB CMRR and 60.2-nV/√Hz input-referred noise spectral density. The entire RFE consumes 16.55 µA from a single 3-V supply.**

***Index Terms*—Bio-potential readout front-end, Chopping stabilization, Instrumentation amplifier, Spike tracking clock.**

I. Introduction

BIO-POTENTIAL signals, such as Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG), can be categorized according to their voltage level, frequency range and bandwidth (BW), as shown in Fig. 1. In order to accurately measure them against various contaminating signals (e.g., electrode offset) in portable biomedical monitoring systems, a low-power high-performance bio-potential readout front-end (RFE) is demanded. A standalone RFE implemented in 0.5-µm CMOS process has been reported [1]. The front stage is an instrumentation amplifier (IA) that exhibits a very high common-mode rejection ratio (CMRR) and low noise. It also offers chopper stabilization for reducing the flicker (1/*f*) noise of the CMOS transistors, which dominates the overall noise at such a frequency range.

In this paper, a low-power, low-noise and high CMRR RFE designed in the advanced 90-nm CMOS process is described. The overall architecture of the proposed bio-potential signals acquisition system is shown in Fig. 2. In accordance to the RFE described in [1], a relatively high supply voltage (V_{DD}) of 3 V is maintained to fulfill the performance requirements, and allows the use of 2 AA batteries. To ensure there is no reliability issue, thick-oxide transistors and high-

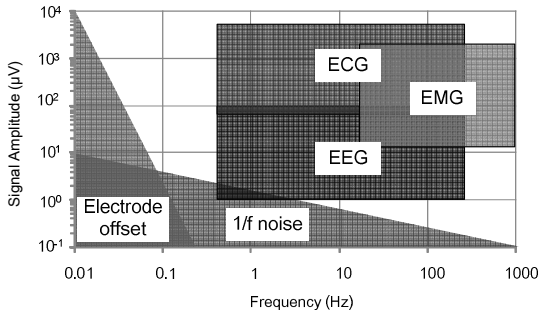

Fig. 1. Bio-potential signals and the nearby contaminating signals

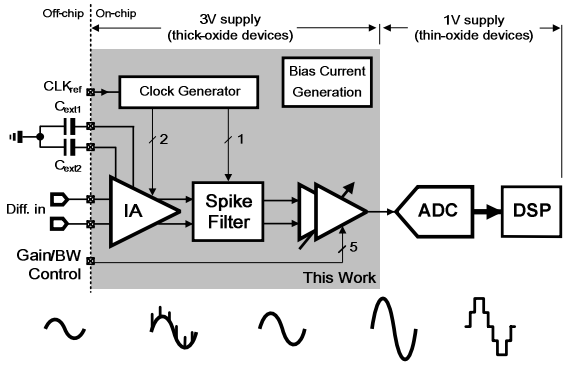

Fig. 2. Proposed bio-potential signals acquisition system.

quality passives offered by the employed 90-nm process (e.g., MiM capacitor and high-resistive polysilicon) are selected for the implementation of the RFE. On the other hand, thin-oxide transistors are preferred for the back-end circuits that involve mainly digital signal processing. Thin-oxide transistors offer the advantages of a smaller feature size and power consumption because of a lower V_{DD} (i.e., 1 V).

II. Architecture of the RFE

As depicted in Fig. 2, the front stage is a differential IA with two off-chip capacitors. Its gain is designed to be given by the ratio of two resistors for robust gain accuracy over process and temperature variations. In this way, a high CMRR can also be achieved without precise resistor matching as in conventional three-stage OpAmp counterparts [2]. The 1/*f* noise and electrode offset are suppressed by concurrent adoption of AC-coupling and chopper stabilization. Spikes generated by the chopper are removed by applying a track-and-hold-like spike filter. Its spike-tracking clock is formed by a novel parallel operation of two non-overlap clock generators. The third stage is a gain-BW-controllable amplifier.

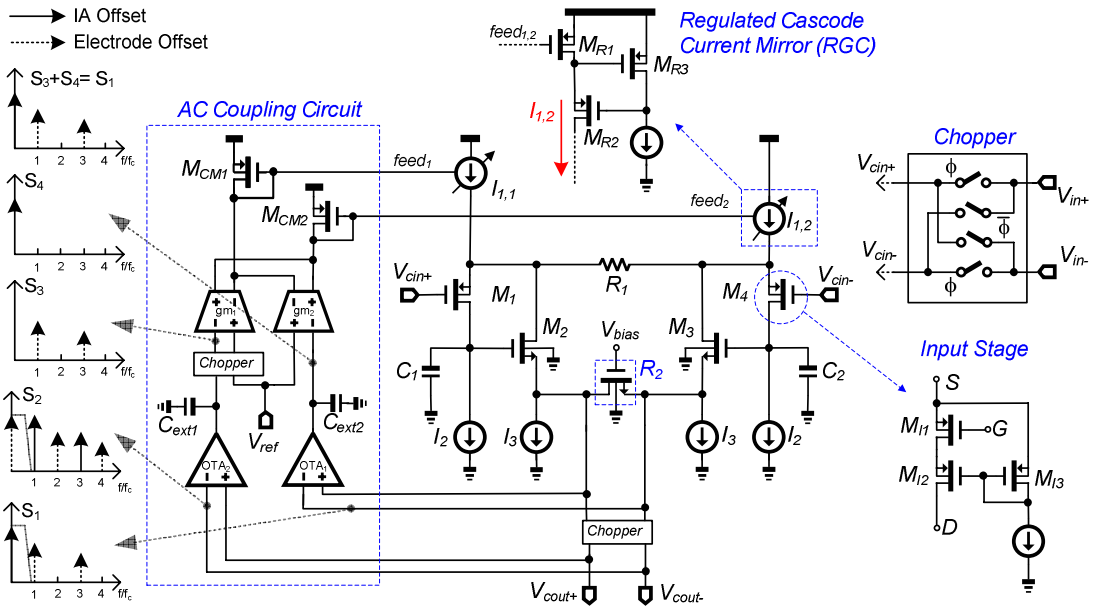

Fig. 3. Schematic of the IA including the AC-coupling circuit, regulated cascade current mirror (RGC), input stage and chopper.

III. Instrumentation Amplifier

Figure 3 shows the schematic of the IA that is designed to offer 10 V/V voltage gain. Various techniques are applied to improve the performances of the IA. Firstly, in order to remove the 1/*f* noise, the chopper modulates the input signal to a higher frequency where 1/*f* noise is neglectable, and then demodulates it back to the baseband after amplification and filtering [3]. Thus the 1/*f* noise of the signal will be filtered and without aliasing if the input-signal frequency is band-limited to less than half of the chopper clock frequency. The second technique is AC-coupling (Fig. 3 left). The output voltage before passing through the demodulating chopper has a frequency spectrum as indicated in S_1, which contains the electrode offset at odd harmonic components, and the IA dc-offset at DC. OTA_1 with low-pass cut-off frequency f_p, extracts the DC components and converts them into the frequency spectrum S_4. On the other hand, the chopped output voltage with frequency spectrum S_2 will be filtered by OTA_2 and then modulated again to become the frequency spectrum S_3. As a result, two voltage signals contain only the electrode offset and IA offset will pass through the transconductance stages (gm_1 and gm_2), which act as a voltage-to-current converter. They will convert the voltage signals into current signals and negatively feedback to the regulated cascode current sources (RGC). The feedback current will combine at R_1 and reform a spectrum same as S_1. Therefore, the electrode offset and IA offset can be cancelled at the same time.

As the transfer function of the AC-coupling feedback loop is equal to $gm_{1,2}/(1+s/2\pi f_p)$, the transfer function of the IA showed in (1) shows its highpass filter characteristic and indicates that the gain is expressed as a ratio of R_2/R_1 when the frequency is large enough (> 1 Hz):

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_2}{R_1}\frac{s+2\pi f_p}{s+A_{OTA}\,gm_{1,2}\,R_2(2\pi f_p)} \qquad (1)$$

In order to identify the tradeoff between the power dissipation and the noise, the input-referred noise power spectrum density (PSD) of the IA is analyzed and given as follows,

$$\overline{v_{in,IA}^{\,2}} = \frac{16kT}{3}\left[\frac{1}{gm_{M1}} + \frac{1}{A_v^{\,2}gm_{M2}} + \frac{3}{4}\left(\frac{1}{g_1}+\frac{1}{A_v^{\,2}g_2}\right) + \frac{(2gm_{I1}+gm_{I3}+gm_1+gm_2)}{g_1^{\,2}} + \frac{gm_{I2}}{(g_1 /\!/\, gm_{M1})^2}\right] \qquad (2)$$

where A_v is the gain of the IA, g_1 and g_2 are the reciprocal of R_1 and R_2 (where R_2 is tunable), gm_{I1}, gm_{I2}, gm_{I3} are the transconductance of the current sources, and the transconductance of M_{CM1} and M_{CM2} are set to gm_{I1} as they have the same current mirror ratio. The 1/*f* noise components are neglected in (2) since they are expected to be eliminated by the chopping technique. Equation (2) also states that the noise can be reduced by increasing the current of $M_1 - M_4$, or by lowering the values of R_1 and R_2. However, the power dissipation will be increased and the electrode offset removability will be degraded. A better solution is to operate the input-transistor pairs in weak inversion by enlarging their sizes, and to bias the current source transistors in strong inversion through their sizes' reduction.

In operation, the electrode offset and the differential signals presented at the gate of the input transistor pairs (M_1 and M_4) and drain of the current sources, $I_{1,1}$ and $I_{1,2}$, will modulate their output transconductance, resulting in degradation of CMRR. To overcome this issue, regulated cascode current mirror (RGC) [4] is applied at $I_{1,1}$ and $I_{1,2}$, and current-balancing technique [1] is applied at M_1 and M_4, such that the drain-to-source voltage of M_{I1} can be made independent to the input DC level.

IV. Spike Filter and Spike-Tracking Clock Generator

A common problem of chopping technique is that spikes will be generated due to the charge injection from the switches of

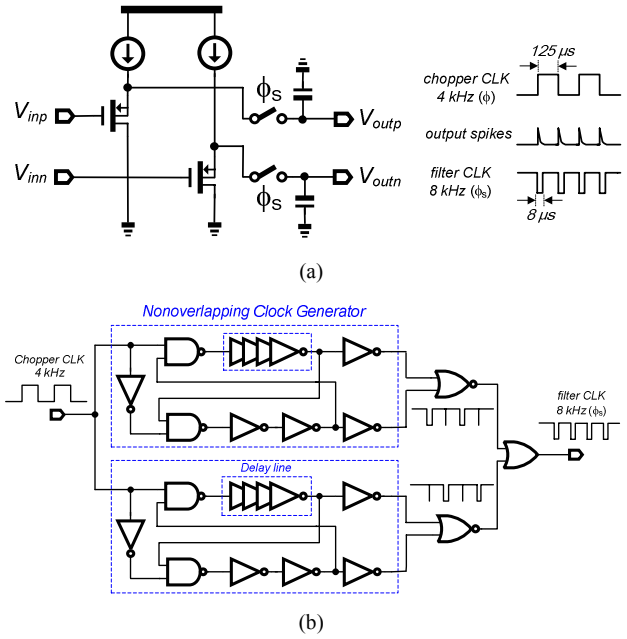

Fig. 4. (a) Schematic of the spike filter and (b) the proposed spike-tracking clock generator.

the chopper. Fig. 4(a) shows the implemented spike filter and its operating principle. The spikes are generated at the edges of the chopper clock square wave with half of the chopper clock period. Before the appearance of the chopping spike, the capacitor will sample the demodulated output signal from IA. During the presence of a spike, the switches of the spike filter are opened and the output is held on the capacitor. This principle is based on the track-and-hold operation, in which the start time of the spikes is precisely known from the chopper clock.

The proposed digital circuitry that generates the desired low-duty-cycle clock waveform is shown in Fig. 4(b). It is based on the parallel operation of two non-overlapping clock generating circuits [5] and certain logic gates. The delay line consists of a chain of inverters and pseudo capacitors with a delay time that is equal to the duration of the repetitive spikes. Two delay lines cannot be built at the same non-overlapping channel, because they will otherwise induce a large time delay at the output clock and the spikes will not be able to be tracked accurately in process variations. On the other hand, by using the proposed parallel non-overlap clock generation architecture, the delay time of each channel can be individually optimized, reducing about 30 dB from the amplitude of spikes components as shown in Fig. 5.

V. Gain-BW-Controllable Amplifier

The final gain stage consists of two gain-BW-controllable amplifiers in cascade, presented in Fig. 6 [6]. For the first stage, the mid-band gain is fixed and is set to 20 V/V, which is defined by the ratio $C_{1,1}/C_{1,2}$. The bandwidth is adjustable by the load capacitances that are implemented by nMOS transistors. In addition, the fixed gain stage also acts as a differential-to-single-ended converter. Furthermore, MOS transistors biased in the triode region act as pseudo-resistors,

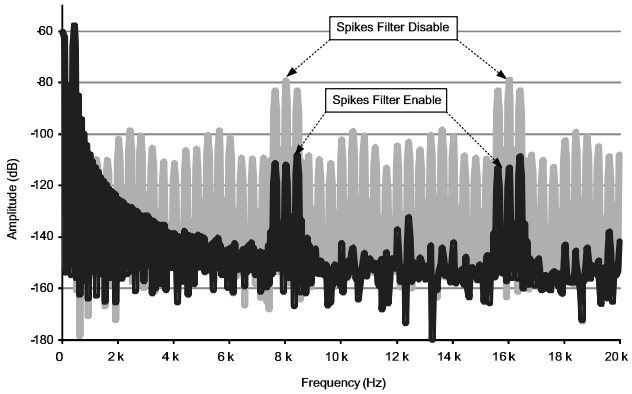

Fig. 5. Chopping spikes filtered by Spike filter

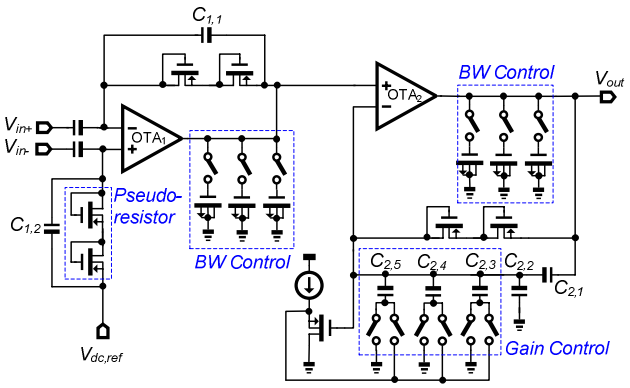

Fig. 6. Schematic of the gain-BW-controllable amplifier.

which consume lower power than resistive-feedback topologies, and simultaneously making both stages to operate in continuous-time to perform anti-aliasing filtering. The gain of the second stage is designed to be variable as given by,

$$A_{V,VGA}(s)=\left[1+s\frac{C_T}{C_{2,1}}\frac{1}{\left(s+\frac{1}{C_{2,1}R_{eq}}\right)}\right]\times\frac{1}{\left[s\left(\frac{C_T}{C_{2,1}}\frac{C_L}{g_{m,OTA2}}\right)+1\right]} \quad (3)$$

According to (3), again, the gain of the second stage is also defined by the ratio of two capacitors ($C_T/C_{2,1}$), where R_{eq} is the equivalent ON-resistance of the pseudo-resistors, and C_L is the total load capacitance. C_T can be set through the switches of the capacitor bank. If a capacitor is connected to the drain of the source follower, it does not contribute to the total capacitance since the source follower equalizes the voltage of the terminals of the capacitor. As a result, the gain of the second stage can be selected to be 2.5, 5, 7.5 or 12.5 V/V, and the total gain of the readout front-end can be continuously adjusted from 500 to 2500 V/V by changing the bias voltage of R_2, which is implemented by a triode-region nMOS transistor.

VI. Simulation Results and Comparison of Performance

The controllable gain feature of the RFE is demonstrated in Fig. 7, where the highpass cut-off frequency is equal to 0.4 Hz and can be adjusted by the external capacitors. For the lowpass cut-off frequency, it is also adjustable by controlling the switches of the capacitive loads (Fig. 6). The simulated voltage gain is consistent to the expected value with tiny gain error.

Figure 8 shows that the simulated CMRR varies with different input electrode offsets applied. The front-end can achieve 140 dB CMRR up to 1 kHz when there is no electrode offset. Since AC-coupling technique is applied to filter the electrode and IA offsets, the CMRR is still as high as 118 dB when the electrode offset is set to 50 mV.

The simulated input-referred noise of the RFE shows that the thermal noise level remained almost the same before and after applying the chopping stabilization technique at the IA. However, it was found that the noise corner frequency is significantly reduced from roughly 500Hz to 5 Hz, which indicated that the *1/f* noise is strongly suppressed after chopping. The residual 1/*f* noise is mainly due the stages after the IA.

Table I compares the simulation results to [1] and the commercial widely-used IA AD620 [7] for biomedical applications, it can be observed that although AD620 achieves the lowest noise, its noise efficiency factor (NEF) is the worst since it consumes much larger power than this work and [1]. On the other hand, this work provides a low power operation of just 50 µW from a single 3-V supply, a wide input common mode range of 1.25 V and a CMRR as high as 140 dB, not mentioning that it has the architecture advantage of being capable to be integrated together with the digital baseband, potentially resulting in a higher integration level.

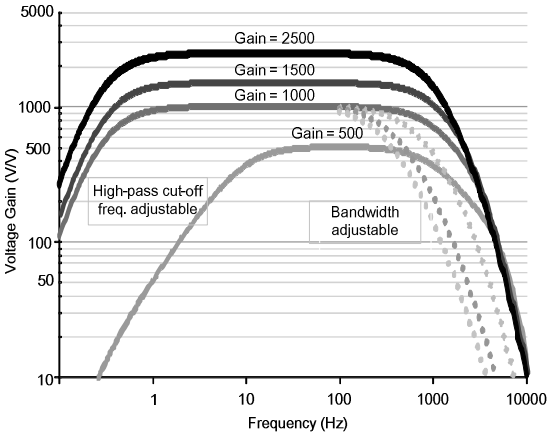

Fig. 6. Adjustable gain and bandwidth characteristics of the RFE.

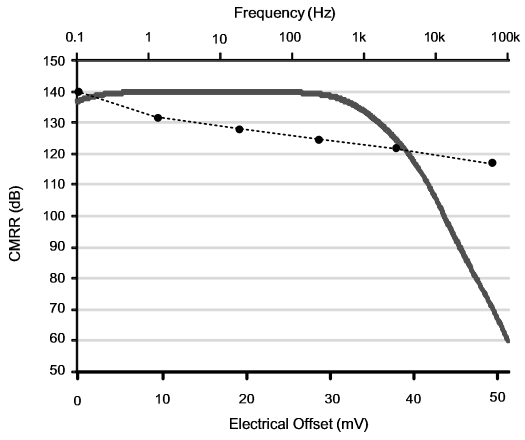

Fig. 7. CMRR characteristic and CMRR with increasing electrode offset

Table I Comparison of the designed RFE, RFE in [1] and AD620

	This work	[1][1]	AD620 [7] [1]
Technology	90 nm CMOS	0.5 µm CMOS	N/A
Supply voltage	3 V	3 V	±2.3 V - ±18 V
Supply current	16.55 µA	20 µA	1.3 mA
Input CM range	1.05 V — 2.3 V	1.05 V — 1.7 V	vary via V_{DD}
Max. gain	2,500 V/V	2,500 V/V	10,000 V/V
Gain adjustable	via internal resistor	via internal resistor	via external resistor
Bandwidth	Adjustable	Adjustable	Not adjustable
High-freq. cut-off	0.4 Hz	0.34 Hz	N/A
Input-referred noise	60.2 nV/√Hz	57.4 nV/√Hz	13 nV/√Hz
THD	0.53 %	0.52 %	N/A
CMRR (0mV offset)	140 dB	120 dB	130 dB
CMRR (50mV offset)	118 dB	110 dB	N/A
PSRR	81 dB	80 dB	140 dB
NEF	9.9	9.2	23

1 — Measurement Results

VII. Conclusion

A 3-V, 50-µW bio-potential readout front-end (RFE) with an input-referred noise of 60.2 nV/√Hz has been demonstrated in 90-nm CMOS. Chopper stabilization and AC-coupling are con- currently applied to the IA for eliminating the 1/*f* noise and filtering the input electrode offset. The achieved CMRR are 140 and 118 dB for no electrode offset and 50 mV electrode offset, respectively. For the spike filter, a novel spike-tracking clock generator is proposed. It is based on the parallel operation of two non-overlapping clock generators to form the desired spike-tracking waveform. The final gain-BW-controllable amplifier permits ECG, EMG and EEG measurements with simple logic controls, all together contributing to the high-performance metrics of the designed RFE that is highly competitive with prior designs.

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