A Highly-Linear Successive-Approximation Front-End Digitizer with Built-in Sample-and-Hold Function for Pipeline/Two-Step ADC

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***Abstract*— This paper presents an improved front-end digitizer for pipeline/two-step ADC. It achieves a high linearity by replacing the front-end stage's sub-ADC from the *flash* type that involves synchronous operation of several comparators, to the one that uses *successive approximation* (SA). This shift not only frees the ADC from an extra front-end sample-and-hold circuit, but also guarantees an inherent monotonicity because of no comparator mismatch (since the SA-ADC involves just one comparator in recursive operation). Two examples of a 100-MHz 3.5-bit/stage pipeline ADC and an 11-bit 30-MHz two-step ADC, validate the feasibility of such a digitizer.**

I. INTRODUCTION

The conventional front-end digitizer of pipeline and two-step analog-to-digital converter (ADC) employs the flash as the sub-ADC to complete the coarse analog-to-digital (A/D) conversion [1]. The threshold of comparator inside the flash, however, may spread around its desired value due to mismatch, resulting in a major source of nonlinearity. Such impairment can be resolved by the digital error correction (DEC) logic if no more than two comparators (i.e. 1.5-bit conversion) have been employed [2]. Thus, the linearity will be degraded for those pipeline ADCs that would try to benefit from the multi-bit front-end digitizer to relax its back-end requirements [3], and those two-step ADCs that typically feature a resolution of more than 3 bits at the first stage [4].

This paper introduces a novel successive-approximation front-end digitizer (SAFED). Instead of exploiting the flash structure, a successive-approximation (SA) sub-ADC [5] is used such that inherent monotonic digitization and built-in sample-and-hold (S/H) function are attained simultaneously.

II. SUCCESSIVE-APPROXIMATION FRONT-END DIGITIZER

S/H Consideration – why the traditional digitizer needs an S/H circuit at the front-end? This can be answered with the help of Fig. 1(a), where the sub-ADC exhibits a typical flash structure. Since the latch and sampling (ph1l) phases are asynchronous, the aperture error ε_{ap} limits the effective resolution of the ADC. To reduce such an error, it would be necessary to use an extra S/H circuit [Fig. 1(b)]. Differently for the proposed SAFED [Fig. 1(c)], its sub-ADC is of a SA structure. Unlike the flash ADC that performs direct

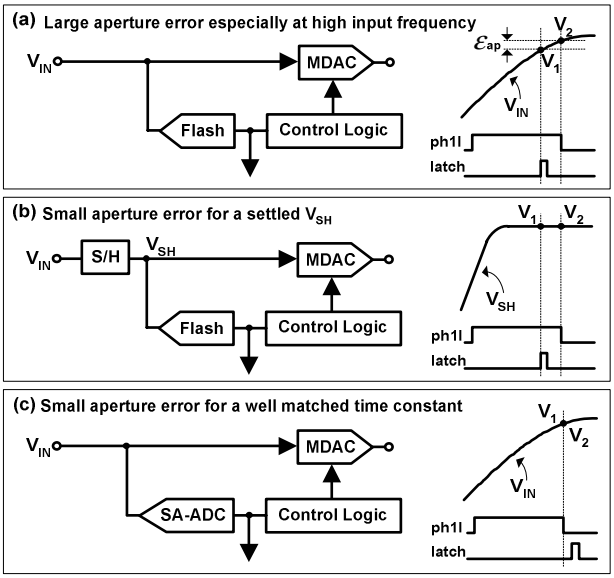

Fig. 1 Architecture and sample instance of (a) conventional front-end digitizer, (b) conventional front-end digitizer with S/H circuit, and (c) SAFED without S/H circuit.

digitization of the input, SA-ADC is a switched-capacitor circuit where its sampling branch offers a built-in S/H function. Synchronizing the falling edge of its sampling phase (at ph1l) with the multiplying digital-to-analog converter (MDAC) eliminates ε_{ap} with no overhead.

Operating Principles – a detailed diagram of the SAFED is depicted in Fig. 2(a). The redundancy of the SA-ADC is 0.5 bit. The succeeding stages should be structured with an identical SAFED for pipeline ADC whereas it will be a full SA-ADC for two-step one. The digital outputs from each stage are applied to the digital error correction (DEC) logic which tolerates the comparator's offset as long as it is less than $V_{REF}/2^{N+1}$ [Fig. 2(b)], where V_{REF} is the reference voltage of the ADC and N is the effective stage resolution.

The operation of the SAFED in every clock period is described in Fig. 2(c). In the first phase, both the SA-ADC and MDAC conducts signal sampling. The former is to perform coarse A/D conversion and produce N.5-bit digital estimation of the trapped input. Assisted by the digital control logic, the latter converts such an estimated value to

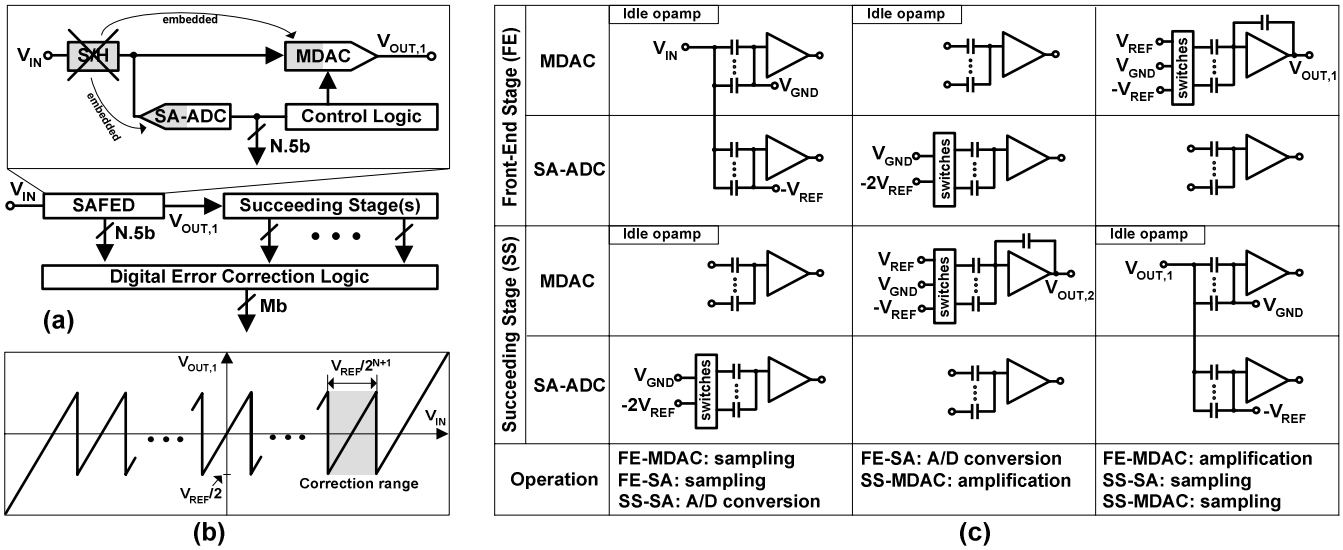

Fig. 2 (a) Architecture of SAFED implemented in pipeline/two-step ADC. (b) Transfer characteristic of a N.5-bit stage. (c) Operation diagram of SAFED and its succeeding stage.

analog, subtracts it from the sampled input, and finally amplifies the residue. The subsequent stage performs further A/D conversion of such amplified residue while the front-end repeats the abovementioned operation with the next sample.

III. SAFED Circuit Implementation

Front-End Sampling Network – the schematic of the SAFED sampling network is depicted in Fig. 3(a). The two sampling branches sample the input voltage synchronously at the falling edge of ph1l. The accuracy is determined by the matching of their time constant, i.e.,

$$R_{SG1}\times\left(C_{T1}+C_{p3}\right)=R_{SG2}\times\left(C_{T2}+C_{p4}\right) \quad (1)$$

$$R_{S1}\times\left(C_{1}+C_{p1}\right)=R_{S2}\times\left(C_{2}+C_{p2}\right) \quad (2)$$

where C_{T1} and C_{T2} are the total sampling capacitance of the MDAC and SA-ADC, respectively. R_{SG1}, R_{SG2}, R_{S1} and R_{S2} denote the ON-resistance of the switch S_{G1}, S_{G2}, S_1 and S_2, respectively. It is obvious that any timing-instance mismatch between the two sampling branches can lead to an aperture error. Assuming a single tone input: $V_{IN}=V_{REF}\sin(2\pi f_{IN}t)$, the aperture error is given by:

$$\varepsilon_{ap}=2\pi f_{IN}\cdot V_{REF}\cdot\Delta\tau \quad (3)$$

where f_{IN} is the input-signal frequency and $\Delta\tau$ denotes the sample-time difference due to mismatch in time constant. In practice, $\Delta\tau$ can be tolerated by the DEC logic as long as the resulted error is within its correction range, i.e.,

$$\Delta\tau\le\frac{V_{REF}/2^{N+1}-V_{OS}}{2\pi f_{IN}\cdot V_{REF}} \quad (4)$$

where V_{OS} denotes the SAFED's static error (such as dc-offset) that may be induced by process and temperature variation.

Successive-Approximation ADC – the architecture of a *N*.5-bit SA-ADC is shown in Fig. 3(b). Capacitive DAC is employed for its inherent S/H function. The operation of the capacitive DAC follows the charge redistribution principle, i.e., the conversion linearity is determined by the relative ratio of the employed capacitors. The detailed operation of the SA-ADC is described below:

The analog input is firstly sampled by connecting the bottom plates of all capacitors to the input signal while all top plates are connected to $-V_{REF}$. Then, all upper plates are left floating while the bottom plates are grounded, forcing the voltage of V_X to jump from zero to $-(V_{IN}+V_{REF})$. The SA iteration begins when the bottom plate of the most significant bit (MSB) capacitor is connected to $-2V_{REF}$, superposing V_{REF} onto V_X. Consequently, $-V_{IN}$ is weighed against ground and the MSB is generated when the comparator is latched. Depending on the comparator's decision, the control logic determines the connection of the MSB and MSB-1 capacitors. Similar decisions are made for each of the following capacitors until the least significant bit (LSB) switch is set.

If we simply compare the conversion speed of flash ADC with the SA ADC, the latter is typically slower because the number of clock cycles required depends on its resolution. However, in serving as a sub-ADC, the effective resolution of each pipeline stage is generally 2 to 4 bits, which is practically affordable by SA-ADC even for high-speed conversion. On the other hand, two-step ADC with SAFED can also be a favorite choice for low power and medium speed design.

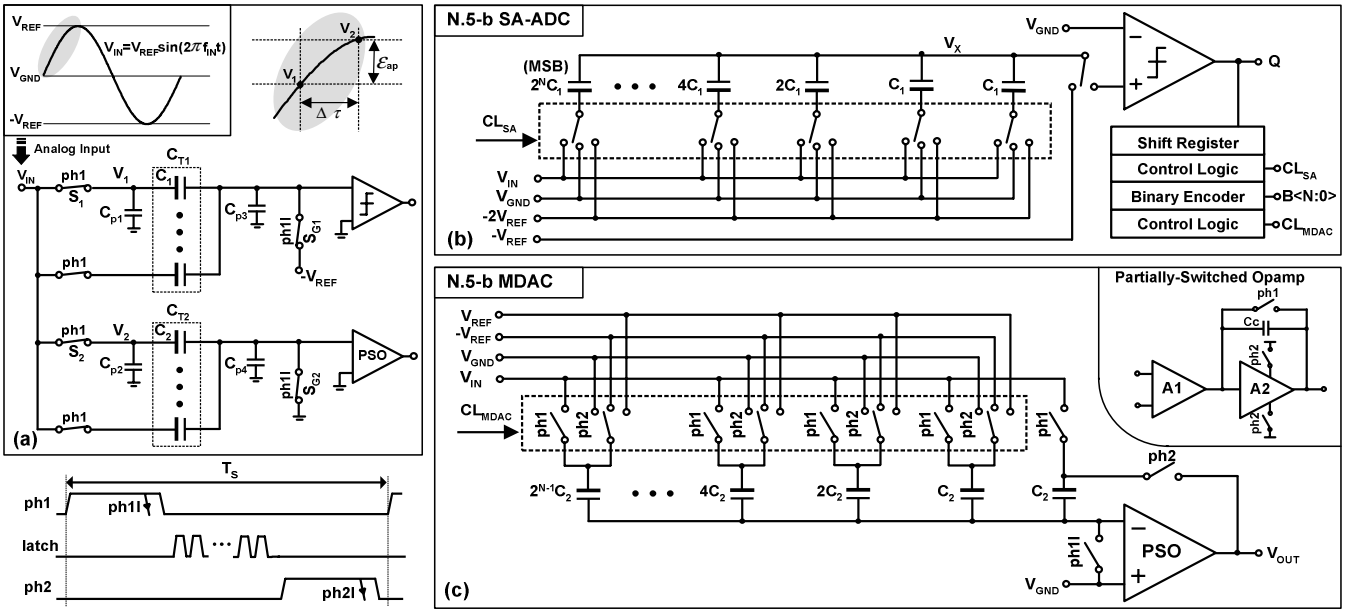

Fig. 3 Circuit implementation of (a) front-end sampling network, (b) N.5-b SA-ADC and (c) N.5-bit MDAC.

Multiplying Digital-to-Analog Converter with partially-switched opamp – a switched-capacitor MDAC with 0.5-bit redundancy is employed to eliminate the aperture error from sampling network and relax the requirement of the SA-ADC. The circuit implementation of a *N*.5-bit MDAC is shown in Fig. 3(c). The analog input is sampled by N-binary-weighted sampling capacitors as well as the feedback capacitor during ph1. The function of amplification and subtraction are performed according to the decision control which arrives at the beginning of ph2. Such amplified analog residue is given by:

$$V_{OUT} = 2^N V_{IN} - \sum_{k=1}^{N} \left(CL_{MDAC,k} \cdot 2^{k-1} V_{REF} \right) \quad (5)$$

where V_{IN} is the analog input and $CL_{MDAC,k}$ (equals -1, 0 or +1) is the subtraction control of stage k generated by the control logic regarding to the *N*.5-bit output of SA-ADC.

In every conversion cycle, the opamp is active only during the amplification phase and thus the opamp can be switched off at both sampling and latching phase to save two-third of its power consumption. In order to obtain a higher operation speed than that of switched-opamp (SO) approach [6], the partially switched-opamp (PSO) technique [7] is employed in the proposed SAFED. During the switched-off mode, the output of the opamp remains at about half of the supply voltage by enabling the second-stage power-down switches. Since only the second-stage of the opamp is switched off, the power efficiency now depends on the current ratio (denoted as R_I) of the second stage and the first stage of the opamp. The relationship between R_I and the number of active opamps is listed in Table 1. It is observed that the number of active opamps required by SAFED is less than that of the conventional structure, and it is inverse proportional to R_I. As a conclusion, the power overhead associated with the use of SAFED in terms of a shortened settling time can still be considered as low.

Architecture of front-end digitizer	Number of active opamp in one clock period T_s			
	R_I=1:1	R_I=2:1	R_I=4:1	R_I=6:1
Flash	1	1	1	1
Flash with PSO (settling time=T_s/2)	0.75	0.67	0.6	0.57
SAFED with PSO (settling time=T_s/3)	0.67	0.56	0.47	0.43

Table 1. Comparison of traditional flash digitizer and proposed SAFED in terms of the number of active opamps.

IV. Design Examples

A 10-bit 100-MHz 3.5-bit-SAFED Pipeline ADC – To demonstrate the effectiveness of the SAFED, a 10-bit pipeline ADC with 3.5-bit stages was built in both MATLAB and CADENCE environments. In the MATLAB case, the simulation was conducted with the following non-idealities: stage precision, KT/C noise, capacitor mismatch, opamp noise and comparator dc-offset. The influence of the comparator dc-offset (Gaussian-distributed with zero mean) is shown in a 100-time Monte-Carlo simulation (Fig. 4). It reveals that the conventional pipeline ADC that uses flash sub-ADC suffers strongly from the comparator mismatch, rendering aggressive performance degradation. On the other hand, the SAFED-based pipeline ADC can tolerate a comparator dc-offset up to a standard deviation (σ) of 14 LSB, relaxing the overall design complexity. The simulated integral non-linearity (INL) and differential non-linearity (DNL) are within 0.3 LSB, and the effective number of bits (ENOB) is greater than 9.8 bits, achieving a linearity comparable to that obtained in a 1.5-bit digitizer (which is inherently insensitive to comparator mismatch).

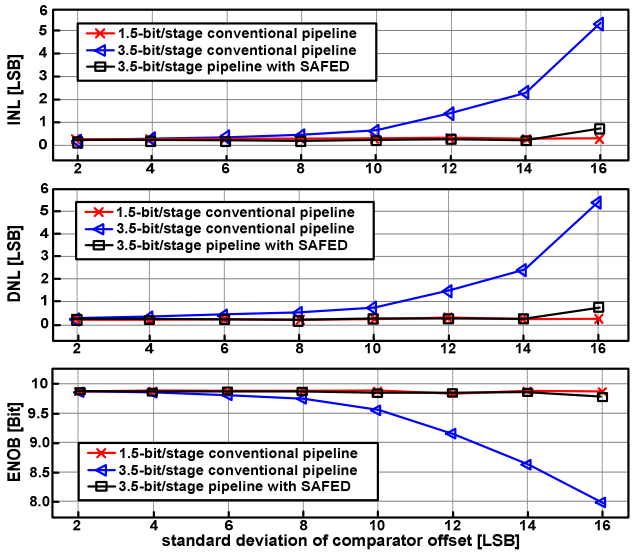

Fig. 4 INL, DNL and ENOB of a 10-bit pipeline ADC in a 100-time Monte-Carlo simulation.

In the CADENCE case, the SAFED designed using the 0.18-µm CMOS process parameters is tested separately for obtaining its stage transfer characteristic. The results obtained from 10-time Monte-Carlo (MC) simulation (under mismatch and process variation) are shown in Fig. 5(a). All results agree well with those obtained from macro-model simulation [Fig. 5 (b)] which exhibit a linear transfer curve with only a constant dc shifting at each comparator threshold.

A 11-bit 30-MHz SAFED-based Two-step ADC – another design example of a two-step ADC was implemented in CADENCE with the 0.18-µm CMOS process. Such ADC is composed by a 5.5-bit SAFED followed by a full 6-bit SA-ADC. DEC logic is essential to maintain the linearity by rectifying the static error of the front-end stage. The simulated output spectrum is shown in Fig. 6 exhibiting an ENOB of 10.8 bits. The entire ADC draws 9.7 mA from 1.8-V supply in a typical case.

V. Conclusions

A successive-approximation front-end digitizer (SAFED) that is universally applicable to both pipeline and two-step ADCs has been presented. It not only simplifies the ADC structure and reduces the power consumption by offering a built-in S/H function, but also offers a higher linearity than the typical flash-based digitizer due to comparator mismatch elimination. Detailed simulation verification validates the high linearity feature of the SAFED and its effectiveness in different types of ADC structures and specifications (i.e., a 10-bit 100-MHz pipeline ADC and an 11-bit 30-MHz two-step ADC).

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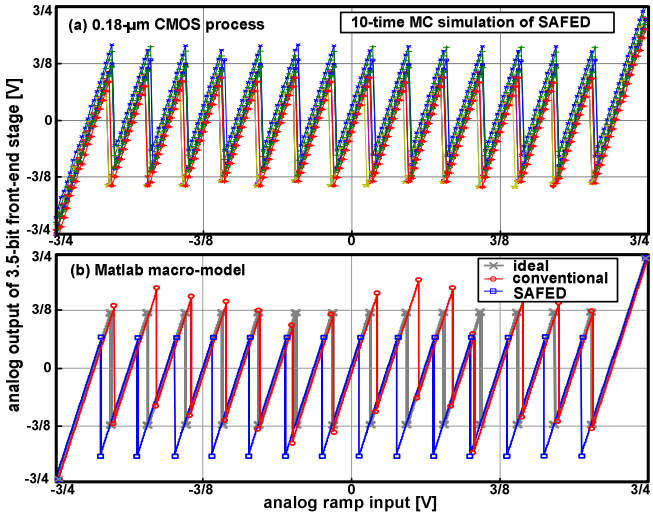

Fig. 5 Transfer characteristic of a 3.5-bit pipeline stage. (a) 10-time Monte-Carlo simulation results of the proposed SAFED in 0.18-µm CMOS. (b) Comparison of ideal, conventional and SAFED architecture in MATLAB macro-model simulation.

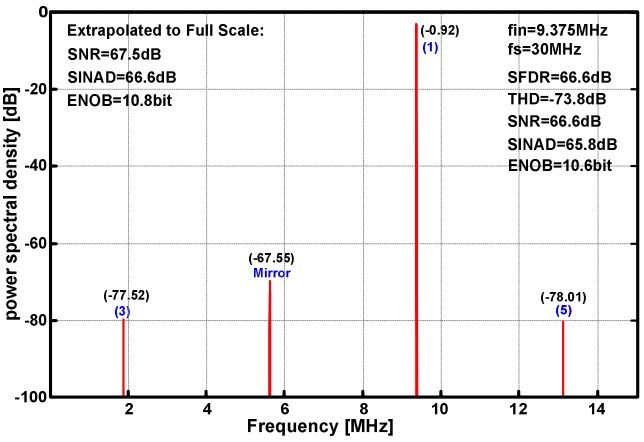

Fig. 6 Simulated FFT of the 11-bit two-step ADC using SAFED.

References

[1] J. Goes, et al., "A CMOS 4-bit MDAC with self-calibrated 14-bit linearity for high-resolution pipelined A/D converters," in *Proc. CICC*, pp. 105-108, May. 1996

[2] Terje Nortvedt Andersen, et al., "A cost-efficient high-speed 12-bit pipeline ADC in 0.18µm digital CMOS," *IEEE JSSC*, vol.40, no. 7, pp.1506-1513, Jul. 2005.

[3] Paulux T. F. Kwok and Howard C. Luong, "Power optimization for pipeline analog-to-digital converters," *IEEE Trans. on CAS-II*, vol. 46, no. 5, May 1999.

[4] Amir Zjajp, et al., "A 1.8V 100mW 12bits 80Msample/s two-step ADC in 0.18-µm CMOS." In *Proc. ESSCIRC*, pp.241-244, Sept. 2003.

[5] Dondi, S, et al., "A 6-bit 1.2GHz interleaved SAR ADC in 90nm CMOS," in *PRIME*, pp. 301-304, Jun 2006.

[6] B. Baz, et al., "A 1.5-V 10-bit 50MS/s time-interleaved switched-opamp pipeline CMOS ADC with high energy efficiency," in *Proc. VLSI Circuits Symp.,* 2004, pp. 432-435

[7] Hwi-Cheol Kim, et al., "A partially switched-opamp technique for high-speed low-power pipelined analog-to-digital converters," *IEEE Trans. On CAS-I*, vol. 53, no. 4, Apr. 2006.