A 2.4 Hz-to-10 kHz-Tunable Biopotential Filter using a Novel Capacitor Multiplier

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***Abstract*— This paper describes a high-dynamic-range 2.4 Hz-to-10 kHz wide-range tunable 5th-order Butterworth lowpass filter for biomedical applications. A differential g_m-C topology in conjunction with a subthreshold-biased wide-g_m-range OTA realizes efficiently a wide frequency tuning capability. For capacitance savings with consequent silicon area reduction, a merged use of floating *real* capacitor and grounded *multiplier-based* capacitor is proposed. Optimized in a 0.35-µm CMOS process, the filter achieves over 68-dB dynamic range, 64 dB stopband attenuation and 28 µW power consumption at a single 3-V supply.**

I. INTRODUCTION

Filter is continually a critical building block of biopotential acquisition systems for enhancing the signal quality. The frequency and amplitude ranges of common biopotential signals are shown in Fig. 1 [1]. These signals are distributed roughly from 1 Hz to 10 kHz. A wide-range tunable lowpass filter that supports most biopotential signals is of demand to minimize the cost and enhance the reusability of the system.

Achieving a wide-range of tunable bandwidth from 10 kHz down to sub-10Hz is challenging. In the literature, several techniques for lowpass filters to achieve an ultra low cutoff frequency have been reported [2]-[4]. Compared with the discrete-time switched-capacitor filters, continuous-time (CT) counterparts have their benefits of lower power consumption, and freeing the system from switching noise. Among all CT filters, transconductance (g_m)-C topology appears as the most reasonable choice. The cutoff frequency is proportional to the g_m; this allows a low-power implementation for low-frequency biopotential signals. In order to achieve an ultra low cutoff frequency with a reasonable area and power, g_m has to be minimized, such that for a low cutoff frequency (sub-10 Hz range), the associated capacitance can be relaxed. Regrettably, the fundamental noise limit is still governed by the kT/C relationship. A g_m-C pole with a small capacitance deteriorates the noise performance [3], imposing a critical tradeoff between area and noise.

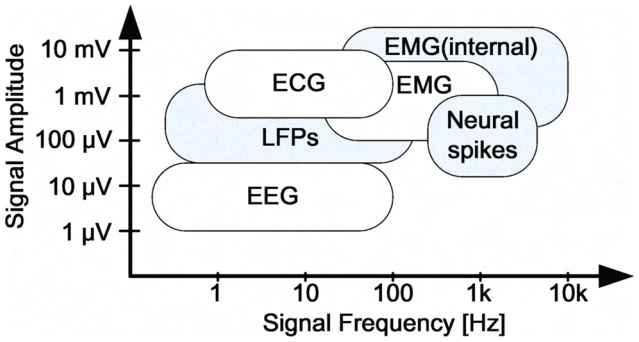

Fig. 1 Approximate frequency and amplitude distribution of common biopotential signals.

In this work, a 5th-order Butterworth g_m-C filter with an optimized differential architecture and circuits is proposed. In addition to the tunable OTA for a wide g_m range, a differential topology with a merged use of floating *real* capacitor and *multiplier-based* capacitor is adopted for area and nonlinearity reduction, while maintaining a reasonable noise performance.

II. FILTER ARCHITECTURE

The prototype of the 5th-order Butterworth lowpass filter is shown in Fig. 2, whereas its equivalent *RLC* prototype is depicted in Fig. 3. For a g_m-C filter topology, the relationship between the cutoff frequency, capacitor values, and g_m can be expressed as follows,

$$\begin{cases} C_1 = C_5 = \dfrac{49.176 \times g_m}{f_{cut-off}}(F) & C_{L2} = \dfrac{257.52 \times g_m}{f_{cut-off}}(F) \\ C_3 = \dfrac{159.12 \times g_m}{f_{cut-off}}(F) & C_{L4} = \dfrac{257.52 \times g_m}{f_{cut-off}}(F) \end{cases} . \quad (1)$$

Obviously, the cutoff frequency can be adjusted by a tunable g_m, which is inversely proportional to the capacitor size. In other words, for a given cutoff frequency, a small g_m reduces the required silicon area, at the expense of higher noise level.

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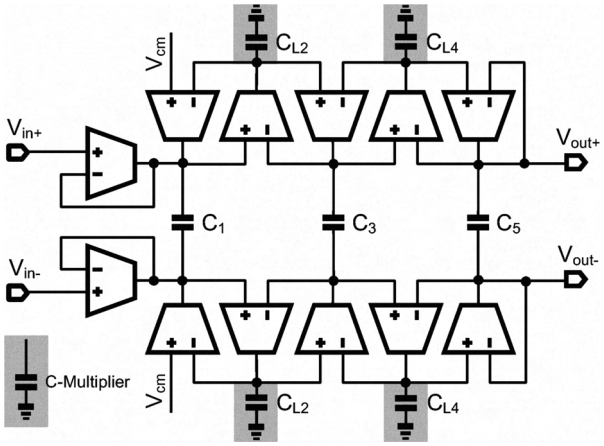


Fig. 2 Proposed 5th-order differential g_m-C lowpass filter with floating capacitors (C_1, C_3 and C_5) and mulitpler-based capacitors (C_{L2} and C_{L4}).

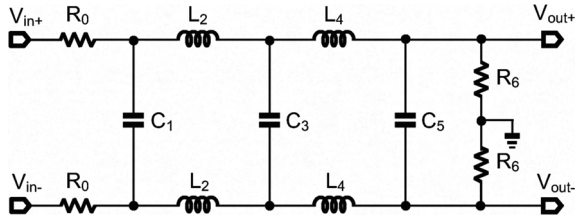


Fig. 3 Equivalent *RLC* prototype of Fig. 2.

Capacitors, regrettably, cannot be made arbitrarily small so as to ensure a reasonable noise performance. In this work, this problem is addressed by using a novel capacitor multiplier for the grounded capacitors: C_{L2} and C_{L4}, and a real (e.g., MiM and polysilicon) capacitor for the differential capacitors: C_1, C_3, and C_5. The former is based on active circuitry to emulate a bigger capacitance from a smaller value. The latter is to take advantage of the differential architecture to double the effective capacitance. The detailed design considerations are given in the next sections.

III. Wide-Gm-Range OTA

The proposed OTA, as shown in Fig. 4, is improved from the previous work [2], [3], [5] in terms of g_m-tunability. The key advantage of its original design is that it combines both current division and current cancellation techniques to achieve a low g_m. However, in terms of tunability, varying V_{B2} can only achieve a small g_m tuning range. To deal with this problem, an array of MOS is introduced to control the size of M_M, which leads to an adjustment of the bias current flowing into M_1 and M_N, resulting in a broader variability of the OTA's overall g_m. Combining this method with a tunable V_{B2}, a wide g_m range can be achieved with small circuit overhead.

A similar MOS array is also introduced to control the size of M_{BN} due to the following reason. For a low cutoff frequency design, the size of M_{BN} has to be enlarged to reduce the flicker noise generated by the transistors. However, as the size increases, the parasitic capacitance increases as well. This unwanted capacitance would reduce the effective g_m at high

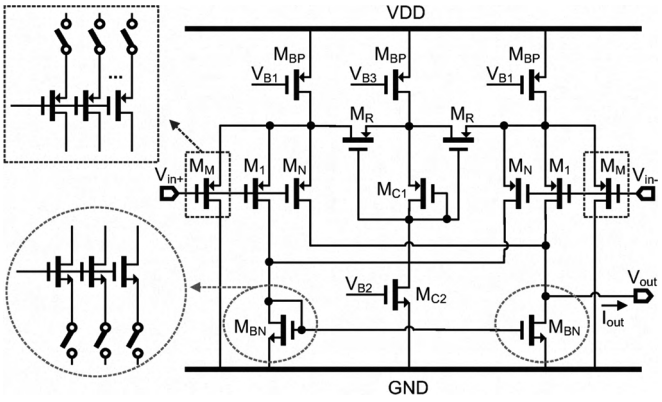


Fig. 4 OTA with a wide range of g_m tunability.

frequency. Thus, for the lowpass filter to offer a high cutoff frequency, the overall g_m of the OTA should be maintained at the same level. This operation is achieved by switching the size of M_{BN} through the use of a MOS array.

IV. Capacitor Multiplier

Bias current is the key factor in determining the amount of thermal noise and flicker noise. The capacitor-multiplier proposed in this work, as shown in Fig. 5(a), employs less active components and cascade transistors, M_{p_in1} and M_{p_in2}, to achieve a low input resistance, significantly reducing the required bias current. Compared with the conventional capacitor-multiplier [3] as shown in Fig. 5(b), the noise performance of the proposed one can be greatly improved.

In addition, to further improved the performance of the capacitor-multiplier, C_{i2} is introduced to suppress the flicker noise generated by the active components of the multiplier. Furthermore, with C_{i2}, there is no DC current injected to the circuit. This advantage avoids the capacitor-multiplier from affecting the OTA bias points.

It is of interest to analyze the proposed and conventional capacitor-multipliers using their small signal models shown in Fig. 6(a) and (b), respectively. For the proposed capacitor-multiplier, if the conditions shown in (2) are all met,

$$\frac{1}{g_{m_2}} \geq 10\left|\frac{sC_{p2}}{g_{m_1}g_{m_2}}\right| \qquad \left|\frac{1}{sC_{p1}}\right| \geq 10\left|\frac{sC_{p2}}{g_{m_1}g_{m_2}}\right| \qquad \left|\frac{1}{sC_{i1}}\right| \geq 10\left|\frac{sC_{p2}}{g_{m_1}g_{m_2}}\right| \quad when \quad f \leq 10 f_{cut-off} \tag{2}$$

the admittance of the capacitor-multiplier can be calculated using (3) and (4) as given by,

$$\frac{i_{in}}{V_{in}} = [N\frac{(r_{oMSN}\|r_{oMSPN})sC_{i2}}{1+(r_{oMSN}\|r_{oMSPN})sC_{i2}} + 1]sC_{i1} + \frac{sC_{i2}}{1+(r_{oMSN}\|r_{oMSPN})sC_{i2}} \tag{3}$$

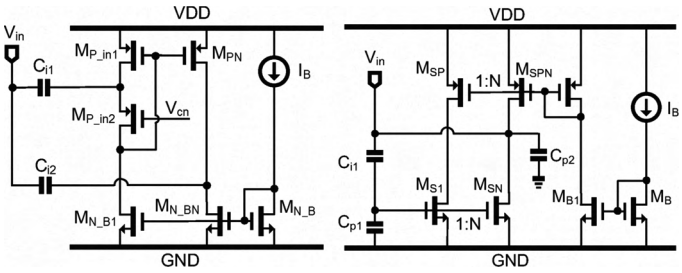


Fig. 5 Capacitor-multiplier: (a) proposed and (b) conventional.

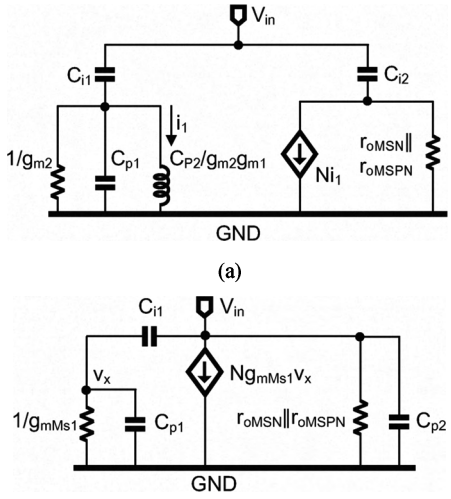


Fig. 6 Small signal circuit of the capacitor-multiplier: (a) proposed and (b) conventional.

$$\frac{i_{in}}{V_{in}} \approx \begin{cases} sC_{i1} + sC_{i2} & when \quad s \le \dfrac{1}{10\left(r_{oMSN} \| r_{oMSPN}\right)C_{i2}} \\ (N+1)sC_{i1} & when \quad s \ge \dfrac{10}{\left(r_{oMSN} \| r_{oMSPN}\right)C_{i2}} \end{cases} \quad (4)$$

In these equations, g_{m1} and g_{m2} are the transconductances of M_{P_in1} and M_{P_in2}, respectively. C_{p1} and C_{p2} denote the parasitic capacitance due to M_{P_in1}, M_{P_in2}, M_{N_B1} and M_{SPN}.

Figure 7 shows the emulated admittances versus frequency of the conventional and proposed capacitor-multipliers reference to an ideal 120-pF capacitor. The bias current for

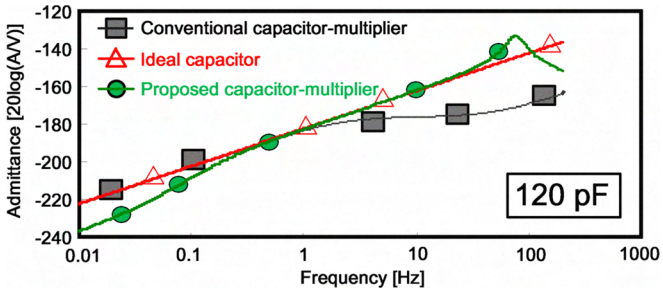
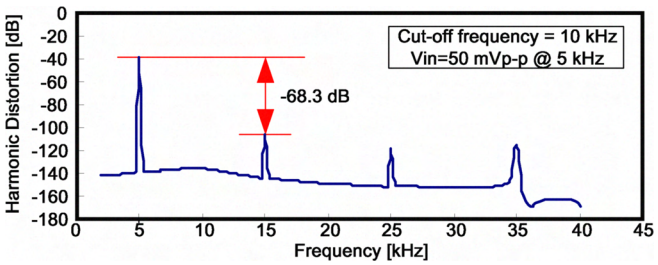
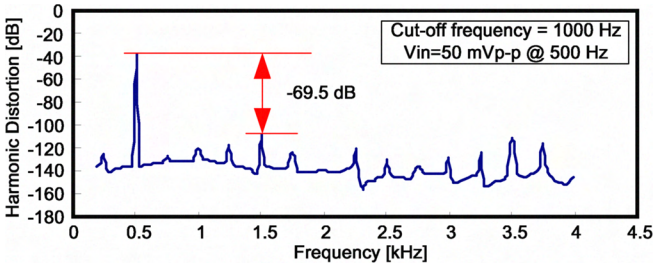


Fig. 7 Emulation quality: ideal capacitor versus conventional and proposed capacitor multiplier.



(a)



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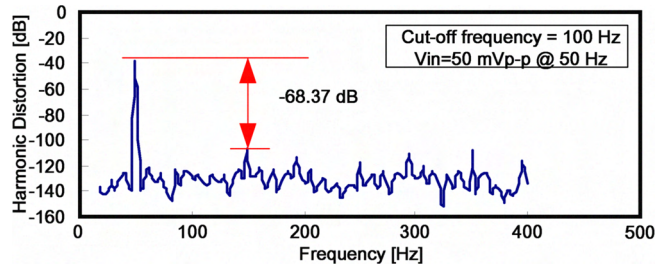
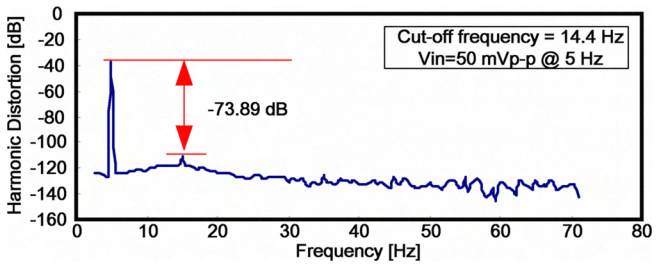
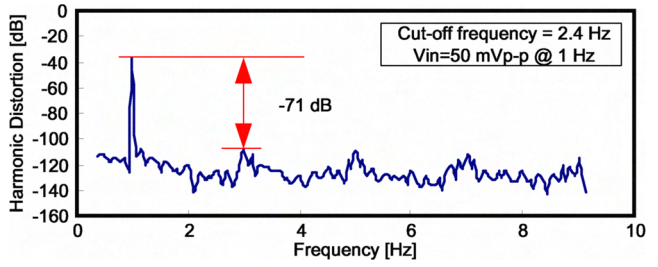


(c)



(d)



(e)

Fig. 8 Harmonic distortion of the filter with different cutoff frequencies and input signal frequencies at: (a) 5 kHz, (b) 500 Hz, (c) 50 Hz, (d) 5 Hz and (e) 1 Hz.

both kinds of capacitor-multiplier is 12 pA. The result shows that the conventional capacitor-multiplier can only emulate as

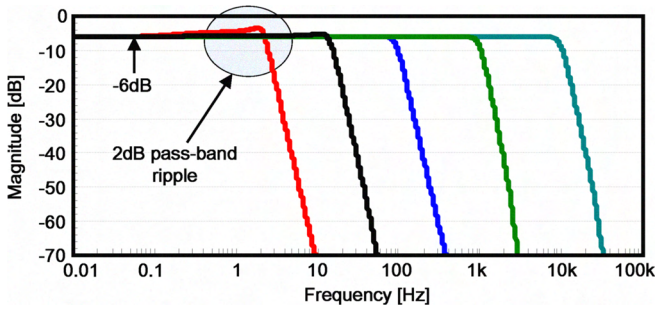


Fig. 9 Magnitude responses of the filter at different cutoff frequencies.

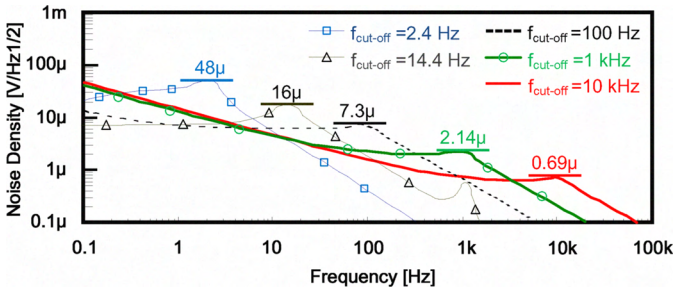


Fig. 10 Output-referred noise density of the filter at different cutoff frequencies.

a 120-pF capacitor below 1 Hz while the proposed one can emulate as a 120-pF capacitor from 1 Hz to roughly 36 Hz. Due to the effect of C_{i2}, the proposed capacitor-multiplier has a decrement of capacitance when operating below 1 Hz.

V. Simulation Results

The proposed 5th-order Butterworth lowpass filter is designed and simulated in a 0.35-µm CMOS process. The simulation parameters are as follows: g_m = 1.25 nA/V (at 2.4 Hz), $C_1 = C_5$ = 25.6 pF, C_3 = 82.8 pF and $C_{L2} = C_{L4}$ = 134.136 pF. For a capacitor multiplier ratio of 6, the *real* capacitance for C_{L2} and C_{L4} are 134.136 pF/6 = 22.356 pF.

Figure 8(a)-(e) shows the linearity performance of the filter based on single-tone tests. The even harmonics are cancelled due to a differential topology. Under different bandwidth settings, the dominant 3rd harmonic is below -68 dB for a 50-mV_{pp} sine input at 5 kHz, 500 Hz, 50 Hz, 5 Hz and 1 Hz.

The magnitude response of the lowpass filter is shown in Fig. 9. The achieved cutoff frequency tunability is from 2.4 Hz to 10 kHz. The stopband attenuation at half a decade is larger than 64 dB. At a very low cutoff frequency, the passband has a ripple up to 2 dB.

Figure 10 shows the output referred noise density of the filter. For the one with a low cutoff frequency, the filter would generate higher noise due to the use of a smaller g_m. For the one with a high cutoff frequency, since we reduce the transistor size of the OTA, the flicker noise becomes more pronounced while the white noise is reduced.

The performance summary and a comparison with a prior work [3] are listed in Table. I. This work is advantageous for its wide range of cutoff frequency tunability, better dynamic range, higher gain and stopband attenuation. The higher in-band noise and power consumption is primarily due to the use of a differential topology, but it gives the design better linearity and common-noise insusceptibility.

TABLE I.
SUMMARY AND COMPARISON WITH A PRIOR WORK

	[3]	This Work
Cutoff Frequency	2.4 Hz	2.4 to 10 kHz
Order and Topology	6th, single-ended	5th, Differential
Technology	0.8 µm CMOS	0.35 µm CMOS
Integrated input referred noise of the @ 0.1 -2.4 Hz	<50 µV	159µV
Dynamic Range	>60 dB	>68 dB
Stopband Attenuation @ Half a Decade	40 dB	>64 dB
DC Gain	-10 dB	-6 dB
Power Consumption	10 µW	28 µW
Supply Voltage	±1.5 V	3 V

[3] is experimental results

VI. Conclusions

A wide-range-tunable 5th-order g_m-C lowpass filter has been presented. A low cutoff frequency down to 2.4 Hz is achieved with a low capacitance requirement by using a wide-g_m-range OTA, a differential topology and multiplier-based capacitors appropriately. Simulated in a 0.35-µm CMOS process the filter achieves 2.4 to 10 kHz tuning range, over 68-dB dynamic range and 64-dB stopband attenuation. The power consumption is 28 µW at a single 3-V supply.

Acknowledgement

The authors would like to thank Mr. Wesley Froehlich from Biomedical Engineering, University of Minnesota-Twin Cities for the valuable discussion. This work is financially supported by the Research Committee of University of Macau and Macau Science and Technology Development Fund (FDCT).

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