# An Ultra-Low Power CMOS Smart Temperature Sensor for Clinical Temperature Monitoring

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***Abstract*—This paper presents an ultra-low power, high accuracy CMOS smart temperature sensor for clinical temperature monitoring applications. The proposed sensor trades off the sensing range and the conversion speed with improved accuracy and power consumption. The sensor consists of a power optimized analog frontend and a delta-sigma analog-to-digital converter (ΔΣADC) with dynamic element matching (DEM), as well as a modified gain stage to optimize the sensing range and relax the resolution requirement. Using a standard 0.18µm CMOS technology, the achieved accuracy and conversion speed after one-point calibration from 27°C to 47°C are ±0.1°C and 2 sample/s, respectively, while consuming only 1.1µW power.**

***Keywords—CMOS smart temperature sensor, clinical temperature monitoring application, ultra-low power, sigma-delta modulation, dynamic element matching***

## I. Introduction

Clinical temperature monitoring in biomedical usage requires high sensing accuracy (e.g. ±0.1°C as in [1]) and ultra-low power consumption for prolonged system lifetime. The power consumption should also be reduced to avoid self-heating. The sensing range should cover a range approximately from 27°C to 47°C for clinical temperature monitoring [2]. The conversion speed requirement can also be much relaxed due to the small bandwidth of bio-signals.

Compared with the traditional discrete temperature sensors like thermistors or platinum resistors, smart temperature sensor based on standard CMOS technology combines a sensor and interface electronics on a single chip to provide significant benefits including low cost and digital output. The sensor reported in [3] is a time-domain temperature sensor with a time-to-digital converter, but it is also sensitive to process variation and only achieves a moderate inaccuracy (i.e. -0.7~0.9°C from 0 to 100°C) after two-point calibration. In [4] the authors present a sensor that can achieve a high accuracy of ±0.1°C in the military range from -55 to 125°C after one-point calibration. Nevertheless, this extended sensing range is inefficient in clinical temperature monitoring.

In this paper, an ultra-low power CMOS smart temperature is presented that achieves an inaccuracy of ±0.1°C over the range from 27 to 47°C. Section II illustrates the operation principle. Section III presents the Matlab-based behavior model. Section IV shows the simulation results. The paper ends with conclusions.

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## II. Operation Principle

### A. Conventional Structure

A conventional BJT-based temperature sensor first utilizes the temperature-dependent characteristics of the BJT to generate both a proportional-to-absolute-temperature (PTAT) voltage $\Delta V_{be}$ and a complementary-to-absolute-temperature (CTAT) voltage $V_{be}$:

$$\Delta V_{be}(T) = \frac{kT}{q}\ln(p) \;\; ; \;\; V_{be}(T) = \frac{kT}{q}\ln\left(\frac{I_c}{I_s}\right) \qquad (1)$$

where $T$ is the absolute temperature, $q$ is the electron, $k$ is the Boltzmann's constant, $I_c$ is the collector current and $p$ is the current ratio of the BJT pair. The ΔΣADC is a key building block in the smart temperature sensor. With an oversampling architecture, the signal-to-noise ratio (SNR) and resolution can be optimized by the oversampling ratio (OSR). The two temperature dependent voltages are then combined by the ΔΣADC with a suitable gain stage α for a temperature-independent reference $V_{ref}$ and a linear ratiometric indication of temperature $u$ as follows:

$$V_{ref} = \alpha \cdot \Delta V_{be} + V_{be} \;\; ; \; u = \frac{\alpha \cdot \Delta V_{be}}{V_{ref}} \qquad (2)$$

In theory, the sensing range indicated by $u$ is from -273 to 300°C. For a targeted sensing range of 27~47°C, this will result in an inefficient coverage of less than 4% of the range. Meanwhile, if the error contribution of quantization noise is designed to be less than 0.01°C, a 16-bit resolution is expected, leading to a high OSR requirement and a large integrator bandwidth. These lead to a large power consumption.

### B. Proposed Structure

To relax the resolution requirement for further power optimization, the proposed structure samples $\Delta V_{be}$ and $V_{be}$ with two sets of gain stages ($K_1$, $K_2$ and $K_3$, $K_4$) based on the ΔΣADC bit-stream output ($bs$) as shown in Fig. 1. The gain stages are constructed by a capacitor array with DEM. According to the principle of charge balancing, the charging, discharging and ratiometric readout relationship can be expressed as:

$$Q_0 = C_{int} \cdot (K_1 \cdot \alpha \cdot \Delta V_{be} - K_2 \cdot V_{be}) \qquad (3)$$

$$Q_1 = C_{int} \cdot (K_3 \cdot \alpha \cdot \Delta V_{be} - K_4 \cdot V_{be}) \qquad (4)$$

$$u' = \frac{(K_1+K_2)\cdot\alpha\cdot\Delta V_{be}}{(K_1-K_3)\cdot V_{ref}} - \frac{K_2}{K_1-K_3} \qquad (5)$$

The integration cap $C_{int}$ is charged by (3) with a charge of $Q_0$ when $bs$ is 0, and discharged by (4) with a charge of $Q_1$ when $bs$ is 1, so that an average charge of 0 across $C_{int}$ can be maintained. The gain and offset of the ratiometric output $u'$ in (5) can be achieved by different $K_1$, $K_2$, $K_3$ and $K_4$, with good

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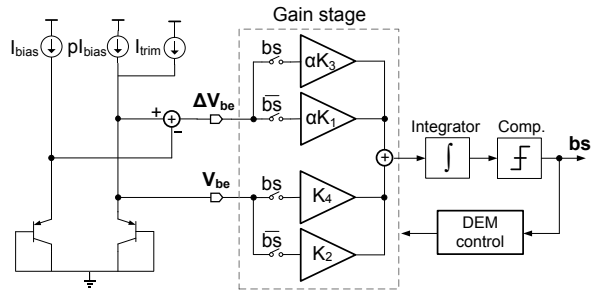


Fig. 1 Architecture of the proposed temperature sensor.

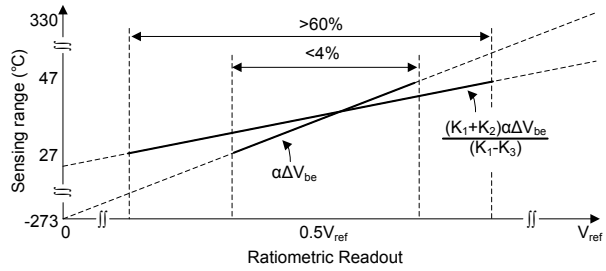


Fig. 2 Comparison of ratiometric output between conventional and proposed structures.

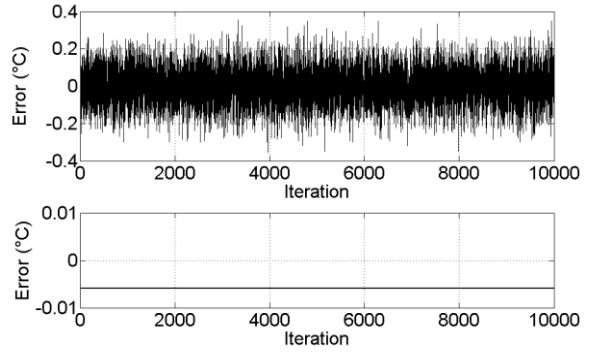


Fig. 3 Error by cap. mismatch without (top) and with (bottom) DEM.

matching accuracy by DEM. After amplifying and offsetting, the proposed structure has a higher efficiency use of the dynamic range (>60%) when compared to the conventional one (<4%), as shown in Fig. 2, and further reduction in power while maintaining high accuracy can be achieved with reduced OSR and integrator bandwidth requirement.

## III. Behavior Model Analysis

Behavior model [5] is used to analyze the performance of the proposed design in Fig.1 on the effects of capacitance mismatch due to large capacitor array size and finite DC gain. We generated 10,000 different capacitor arrays, each with a 3σ capacitor mismatch of 1%. As shown in Fig. 3, an error of ±0.4°C is introduced. This error can be significantly reduced to a negligible offset of -0.005°C by using DEM. The finite OpAmp DC gain also has an impact on the performance. As observed in Fig.4, the error introduced by the finite DC gain is no longer significant when the gain is larger than about 80dB.

## IV. Simulation Results

The proposed circuit is also implemented in a standard 0.18µm CMOS process. The BJT pair is biased with $I_{bias}$=30nA (Fig.1). Coarse and fine current trimming is also included to compensate for the process variation [4]. A first-order ΔΣADC with an OpAmp open-loop DC gain of 80dB samples and combines the $V_{be}$ signals to generate a

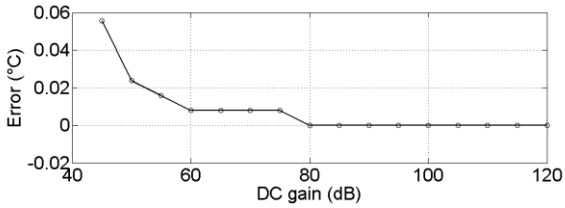


Fig. 4 Error caused by finite DC gain at 37°C.

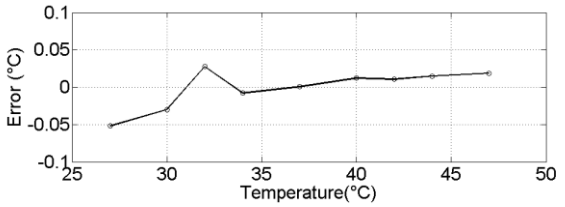


Fig. 5 Simulation Result in the defined sensing range.

TABLE I. Performance Summary

| | This work# | [3]* | [4]^ | [6]^ |
|---|---|---|---|---|
| **Process** | 0.18µm | 0.35µm | 0.7µm | 0.16µm |
| **Temp. Range (°C)** | 35~45 (27~47) | 0~100 | -55~125 | -55~125 |
| **Inaccuracy (°C)** | ±0.04 (±0.1) | -0.7-+0.9 | ±0.1 | ±0.15 |
| **Power (µW)** | 1.1 | 10 | 187.5 | 5.1 |
| **Samp. Rate (Sa/s)** | 2 | 10k | 10 | 188 |
| **Calibration point** | 1 | 2 | 1 | 1 |

# Simulation results.
* Measurement results.
^ 3σ measurement results.

PTAT voltage $\Delta V_{be}$ and a reference $V_{ref}$. The bit-stream is produced and converted into a ratio-metric readout by an accumulator. The error shown in Fig.5 indicates that the target inaccuracy of less than ±0.1°C after one-point calibration at 37°C can be achieved.

## V. Conclusions

An ultra-low power, high accuracy CMOS temperature sensor is presented in this work. The power consumption is as low as 1.1µW which achieving an inaccuracy of ±0.1°C suitable for clinical temperature monitoring.

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