20.5 A 2-/3-Phase Fully Integrated Switched-Capacitor DC-DC Converter in Bulk CMOS for Energy-Efficient Digital Circuits with 14% Efficiency Improvement

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Reducing the supply voltage of digital circuits to the sub- or near-threshold regions minimizes dynamic power consumption and achieves better efficiency [1]. This technique is widely used in energy-efficient applications, and is especially beneficial for wirelessly powered devices such as wearable electronics, biomedical implants and smart sensor networks. Such devices have long standby times and battery-less operation is highly desirable. As shown in Fig. 20.5.1, for a typical wireless power transmission system, there is a gap between the rectified V_{IN} (>2V) and the low supply voltage V_{OUT} (<700mV) for powering up energy-efficient digital circuits. To bridge this voltage gap without sacrificing compact size, fully integrated power converters with a low voltage conversion ratio ($M=V_{OUT}/V_{IN}$) and high efficiency are needed. However, a low M results in low efficiency for linear regulators and fully integrated buck converters. On the other hand, fully integrated switched-capacitor power converters (SCPCs) are good alternatives that can achieve high efficiency at low M in low power applications [2-5].

Reconfigurable SCPC designs with multiple conversion ratios could provide low output voltages and maintain high efficiency [3, 4]. In [3], four power stages are cascaded in recursive sequence and achieve 15 linear ratios, providing a low output voltage down to 0.1V. However, this 2-phase SCPC needs many flying capacitors and power transistors. In [4], four conversion ratios are used to support an output voltage range of 0.45 to 1V from a 1.225V input. In [6], 3-phase operation was introduced to realize more conversion ratios using the same number of flying capacitors.

In this paper, a fully integrated 2-/3-phase reconfigurable step-down SCPC with an input voltage range of 1.5 to 2.5V and an output voltage range of 0.4 to 0.7V is proposed (Fig. 20.5.1). The power stage consists of only 2 flying capacitors and 8 switches (Fig. 20.5.2). For V_{IN}<2V, the converter operates in 2-phase mode with M=1/3; and for high V_{IN} (2-2.5V), it operates in 3-phase mode with M=1/4. For simplicity, consider the no-load case such that capacitor voltages do not change from phase to phase. The 1/3X mode operates with two phases and the subtraction operation is adopted (see Fig. 20.5.3). In Φ_1, C_2 is stacked on top of C_1 in parallel with C_L, and $V_{IN}=V_{C2}+V_{C1}$ with $V_{C1}=V_{OUT}$. In Φ_2, C_2 is discharged by C_1 in series with C_L, and $V_{OUT}=V_{C2}-V_{C1}$ meaning that $V_{OUT}=V_{IN}/3$. The 1/4X mode operates with three phases. In Φ_3, we have $V_{C1}=V_{OUT}$; in Φ_1, $V_{IN}=V_{C2}+2V_{OUT}$; and in Φ_2, $V_{C2}=2V_{OUT}$ meaning that $V_{OUT}=V_{IN}/4$. With the 1/4X mode, efficiencies of low output voltages are improved, and the 3-phase operation requires no additional flying capacitor.

For a bulk-CMOS process, MOS capacitors have the highest capacitance density but also have large parasitics that reduce the overall efficiency. Effective alternatives have been reported, such as using ferroelectric capacitors [2] or high-density MIM capacitors [4]. However, these require special processes. In our proposed SCPC, two approaches are suggested to reduce parasitic losses: 1) An on-chip voltage doubler that provides high N-well bias voltage for P-type MOS capacitors to reduce the N-well parasitic capacitance, and 2) A subtraction operation of capacitors that helps reduce the parasitic loss to 1/4 of the heuristic summation operation. Consequently, this design results in 14% improvement in the peak efficiency.

Figure 20.5.1 shows the 9-cell interleaving SCPC architecture that achieves reduced output voltage ripple and maintains high efficiency. Each cell is composed of a dual-branch power stage, a 2-/3-phase clock generator and local dead time drivers. To avoid phase mismatches due to long-distance clock distribution and process variations, the clock for the power stage is generated locally by the 2-/3-phase clock generator, and the local dead time drivers prevent shoot-through currents. Two voltage domains, V_L=1.2V and $V_H=V_{IN}$-1.2V, are used to tackle breakdown issues and to minimize switching loss. In particular, an on-chip voltage doubler that uses thick-oxide transistors is built to provide high voltage biases for integrated capacitors with reduced parasitic junction capacitances.

Figure 20.5.2 shows the transistor implementation of the power stage. Local dead times are generated by transistors $M_{D1\text{-}8}$ and the corresponding inverters to uphold the break-before-make mechanism to prevent shoot-through currents from passing through transistor-pairs, $M_{P1\text{-}8}$ and $M_{N1\text{-}8}$, even at very high switching frequencies. This scheme is easily extended to accommodate more interleaving cells without increasing the circuit complexity. Flying capacitors C_1 and C_2 are stacked with on-chip MIM, MOM and MOS capacitors in a vertical hierarchy, and achieves a capacitance density of ~15fF/μm^2. Parasitics of MOS capacitors are dominated by channel capacitance C_C and well-junction capacitance C_W. P-type MOS capacitors with deep N-well isolation can be used to reduce them. With reference to the equivalent circuit, C_C is shorted by resistors R_W and R_C. As C_W is inversely proportional to its bias voltage, the deep N-well is connected to the output of the on-chip voltage doubler that does not need to provide current and is very low-power and area-efficient (50x100μm^2).

Figure 20.5.3 shows two 1/3X configurations. It is easy to show that in the summation mode, $V_{C1}=V_{C2}=V_{IN}/3$, while in the subtraction mode, $V_{C1}=V_{IN}/3$ and $V_{C2}=2V_{IN}/3$. Next, consider the negative-plate parasitic capacitor, C_{p1}, of C_1. In the summation mode, V_{Cp1} swings from $2V_{IN}/3$ to 0, while in the subtraction mode, it swings from $V_{IN}/3$ to 0. As switching loss is given by CV^2f, the parasitic loss due to C_{p1} in the subtraction mode is reduced to 1/4 that of the summation mode. Hence, the subtraction mode gives lower parasitic loss, and is employed in [2]. To verify the above qualitative analysis, both the summation mode and the subtraction mode are implemented using the same circuit parameters for fair comparison. Switching at 60MHz and 100MHz, the measured efficiency at various current densities with V_{IN}=2V and $V_{OUT}\approx$0.6V are shown in Fig. 20.5.3. The peak efficiency enhancement is 11.8%, and can be higher in light load conditions.

The proposed 2-/3-phase SCPC is fabricated in a UMC 65nm CMOS process. It occupies an area of 500x850μm^2 (0.23mm^2 active area). Figure 20.5.4 shows the measured efficiency of the 1/3X and 1/4X modes with respect to the current density, the input voltage and the output voltage. The results with the on-chip voltage doubler enabled (V_{bias}=5V) or disabled (V_{bias}=2V) are shown for comparison. The converter achieves peak power efficiencies of 79.5% in 1/3X mode and 69% in 1/4X mode at 56mA/mm^2. In enabling the voltage doubler, the efficiencies are increased by approximately 3%. Figure 20.5.5 shows the conversion efficiency versus reverse-bias voltages generated by the voltage doubler for the integrated capacitors at current densities of 56 and 109mA/mm^2, respectively. Compared to directly biasing the capacitors by V_{IN}, the efficiency improvement is approximately 3% by using 2.5V I/O devices. If 3.3V I/O devices are available, the enhancement could reach 4.5% at V_{bias}=6.6V.

Figure 20.5.6 shows the comparison of recent fully integrated power management ICs in standard bulk-CMOS that have a sub- or near-threshold output voltage range (V_{OUT}<700mV). The chip micrograph is shown in Fig. 20.5.7, including the comparative work for the two 1/3X topologies.

This work discusses the design of SCPCs with low voltage conversion ratio (2.5V to 0.5V). By introducing the 3-phase mode and the parasitic insensitive topology with on-chip voltage doubler for C_W reduction, the proposed SCPC achieves an overall 14% efficiency improvement and shows high efficiency at the sub-/near-threshold region without using advanced processes or sacrificing the current density.

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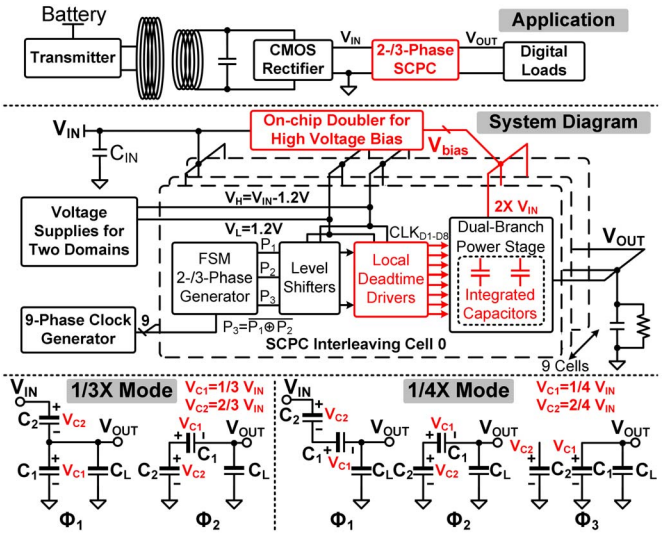

Figure 20.5.1: Block diagram of a wireless power system, the proposed 2-/3-phase SCPC, and operation principles.

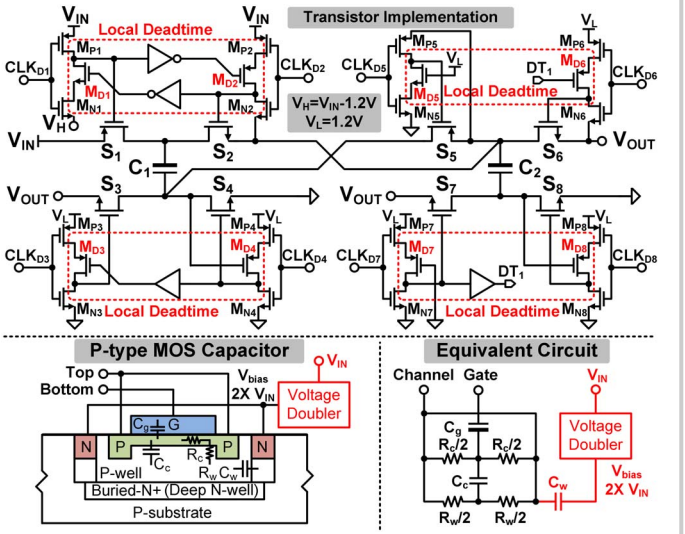

Figure 20.5.2: Transistor implementation of the power stage, a P-type MOS capacitor, and its equivalent circuit.

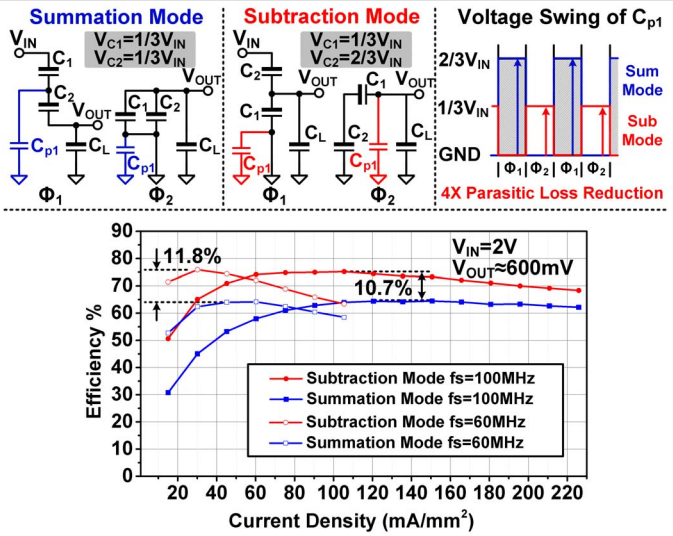

Figure 20.5.3: Operation principles of the summation and subtraction modes and measured efficiency at 100MHz and 60MHz.

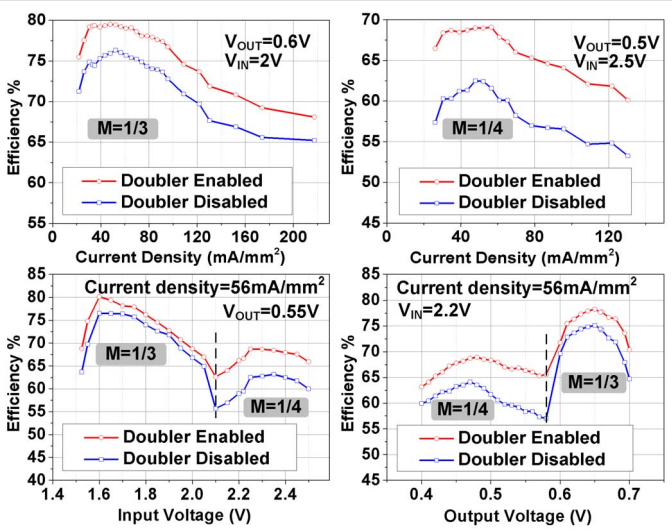

Figure 20.5.4: Measured efficiency versus current density, input voltage, and output voltage.

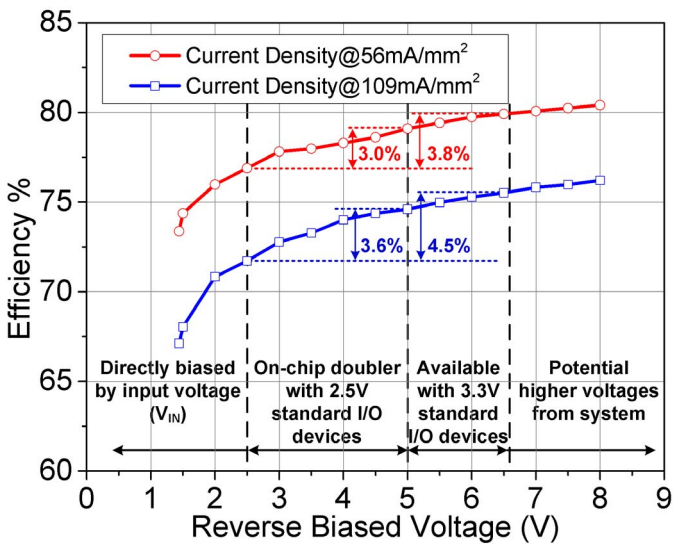

Figure 20.5.5: Measured efficiency versus reverse biased voltages.

Work	2013-JSSC [5]	2014-ISSCC [3]	2014-JSSC [4]	This work
Technology	130nm CMOS	250nm CMOS	22nm CMOS	**65nm CMOS**
Topology	Step-Down SC	Step-Down SC	Step-Down SC	**Step-Down SC**
Ideal Conversion Ratios	1/2, 1/3	4-bit Recursive	1, 4/5, 2/3, 1/2	**1/3, 1/4**
Passive Type	Dual-MIM, MOS	MIM	High-Density MIM	**MIM, MOM, MOS w/ Well-bias**
V_{IN}	1.2V	2.5V	1.225V	**1.5-2.5V**
V_{OUT}	0.3-0.55V	0.1-2.18V	0.45-1V	**0.4-0.7V**
$P_{OUT,\ MAX}$	22mW	4.36mW	25mW	**26mW**
η_{peak} @ Sub-/Near-Threshold Region	67% @0.50V 64% @0.45V	60% @0.6V 55% @0.5V 50% @0.4V	74% @0.70V 70% @0.55V 62% @0.40V	**79.5% @0.6V** **69% @0.5V** **63% @0.4V**
Current Density @ Sub-/Near-Threshold Region	12.25mA/mm^2	0.43mA/mm^2	144mA/mm^2	**56mA/mm^2**

Figure 20.5.6: Comparison with prior art.

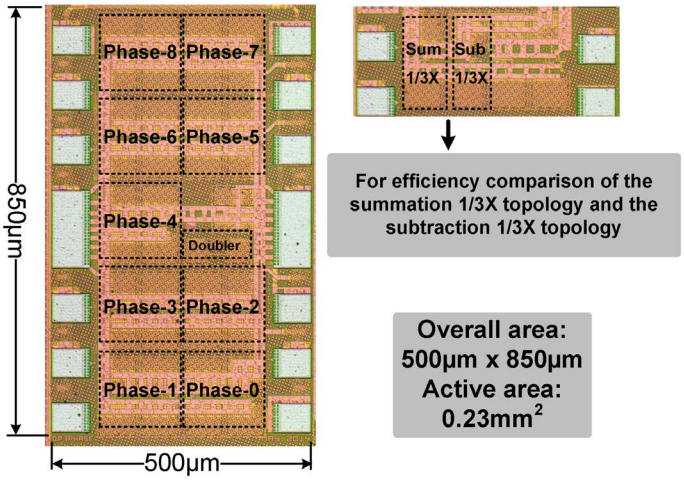

Figure 20.5.7: Chip micrograph of the 2-/3-phase fully integrated SCPC.

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