# A Self-Timing Switch-Driving Register by Precharge-Evaluate Logic for High-Speed SAR ADCs

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***Abstract*— Novel self-timing switch-driving registers for high-speed Successive Approximation Register (SAR) ADC is proposed. This circuit can provide fast charging path from comparator output to DAC array of SAR ADC and store the comparison results simultaneously at each approximation bit-cycle. The propagation delay from input to output of the register is about 60ps only in a 90nm CMOS process. By using this technique, the 5-bit SAR ADC achieves 30.3dB SNDR with 285MS/s high sampling-rate, power consumption is 10.5mW.**

## I. INTRODUCTION

Recently the SAR ADC [1]-[4] becomes the most popular prototype of analog-to-digital converter, numerous significant techniques and design methods for improving the performance of SAR ADC have been proposed continually, including asynchronous operation [5], charge sharing technique [6], as well as split capacitive array [7] using charge recycling, etc. They let SAR ADC to be able to achieve high power efficiency and higher speed in medium resolution range.

The asynchronous processing technique [5] optimizes the internal comparison time of each approximation cycle, which depends on each resolvable input level. It substantially increases the conversion speed compared to the traditional synchronous design. The capacitor splitting technique [6] achieves charge recycling in a binary-weighted capacitor array and it can reduce the DAC settling time and has been proven to be energy efficient. The passive charge-sharing techniques [7] pre-charges the reference voltage (obtained from the supply voltage) into its capacitor array before each conversion process, thus it does not need the power consuming reference ladder and also avoids the resettling problem from reference ladder charging to DAC in general charge-redistribution SAR ADC.

All the above significant techniques target improving the speed of the SAR ADC, either by improving the regeneration-time of the comparator or by reducing the RC-settling time of the capacitor array. Nevertheless, one of the dominant speed limiting factors is the propagation delay in the Successive Approximation (SA) loop, which relies on the efficient implementation of the SA logic. This paper proposed a new switch-driving register to reduce the logic propagation delay in the loop of SAR conversion.

## II. CONCEPT OF PROPOSED CIRCUIT

The architecture of conventional SAR ADC is shown in Fig.1, consisting of a capacitive DAC array, a comparator and SA control logic. The SA control logic includes SR latch, bit caches, shift registers and buffer which control the DAC operation by performing the binary-scaled feedback during the successive approximation. The SR latch detects the comparator differential output and holds the comparison result, and the bit caches save the results of each SA cycle. The shift registers generate the multi-phase clock pulse to control the bit caches turn on/off. The DAC capacitor array is the basic structure of the SAR ADC and it serves both to sample the input signal and as a DAC for creating and subtracting the reference voltage. In general, the SR latch is composed of two NAND gates, and the bit caches are

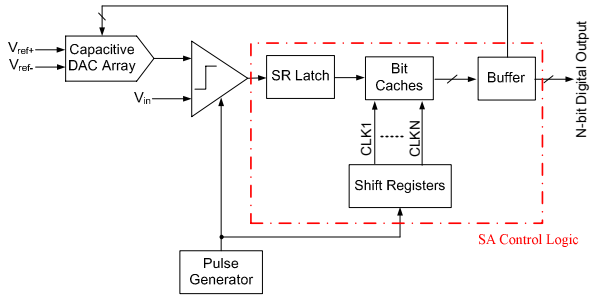


Fig. 1: Block diagram of conventional SAR ADC architecture.

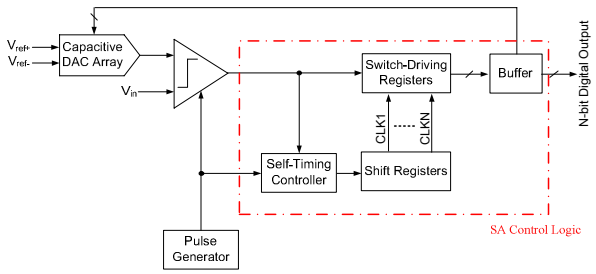


Fig. 2: Block diagram of SAR ADC architecture utilizing switch-driving registers & self-timing controller in [8].

composed of D Flip-Flops (DFFs), both of them are the sequential bi-stable circuits, whose states are determined by the current inputs as well as the previously applied input variables, consequently introduce large propagation delay to the path of comparator output through two feedback loops. To shorten the signal path from comparator output to DAC array, the SR latch and bit caches could be replaced with switch-driving registers [8] such as Fig. 2. The switch-driving registers employed by the precharge-evaluate logic (one important kind of dynamic logics) circuits can capture the comparison results straight away, which are being substituted for two bi-stable feedback loops requiring numbers of transistors and causing large propagation delay.

In order to reduce the SA cycling time in SAR ADC, the slower static logic should be replaced by the faster dynamic logic. The SAR ADC in [8] utilized the precharge-evaluate logic to implement the switch-driving registers. Furthermore, [8] exploited self-timing controller to assist with the shift registers to produce clock phases in SA loop efficiently as shown in Fig. 2. The theory of self-timing [9] is to stint the comparator decision time and relax the time for analog signal to settle in the DAC capacitor array. In other word, once the comparator output has settled, the remaining clock period is borrowed to charge the DAC array. However, to detect if the comparator output has settled or not, extra logic gates must be inserted into the comparator output path indirectly, at least 1 XNOR gate, 1 NAND gate and 1 NOT gate, amount to 7 transistors delay in the situation of [8]. The proposed switch-driving registers co-operate with a simple conversion detector to accomplish the function of self-timing and achieve more shorten propagation delays by precharge-evaluate logic, the block diagram of SAR ADC utilizing proposed circuits is shown as Fig. 3.

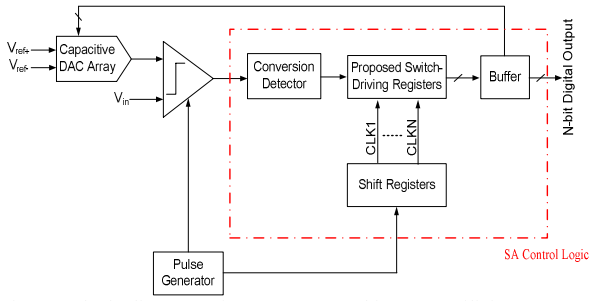


Fig. 3: Block diagram of SAR ADC architecture utilizing proposed switch-driving registers and conversion detector.

## III. CIRCUIT DESIGN AND IMPLEMENTATION

In following sections a 5-bit SAR ADC will be described as an example to demonstrate the function and performance of proposed circuits. Fig.4 shows the main part of SA controller formed with the proposed switch-driving registers and the shift registers (cascaded DFFs). As mention before, shift registers offer the clock pulses VQ1, VQ2, … VQ6 successively to activate the switch-driving registers during every SA cycle. Two sets of 5-bit switch-driving registers with their outputs B1P, B2P … B5P, B1N, B2N … B5N store the comparison results, as well as control the differential DAC array to connect with positive or negative reference voltage separately. Notice that the proposed 5-bit switch-driving registers have six inputs of successive pulses from the shift registers, since each bit-branch of switch-driving registers needs two successive pulses to trigger two actions in sequence. The first action is to pre-charge the branch output to the shifting "1" ("0" at verf- switching-driving registers), and the next action is to capture the result of evaluation / comparison.

Fig. 5 shows the schematic of conversion detector working together with the 5-bit proposed switch-driving registers. It is composed by a NOT gate & 4 transistors $M1_0$~$M4_0$. While the CLK is low, *Y* is pre-charged to VDD through $M1_0$, and the comparator is in reset-state. When the CLK is high, $M4_0$ turns on and if the comparator output is well defined, $M2_0$ and $M3_0$ are always driven in the same direction to decide the output *Y* as high or low. When the comparator output is metastable and does not resolve, $M2_0$ and $M3_0$ cannot turn on simultaneously, *Y* will keep high. This will not affect the comparison result since when the comparator is in meta-stability state, the comparator input is very close to the threshold and it does not matter to generate logic one or zero at the comparator output.

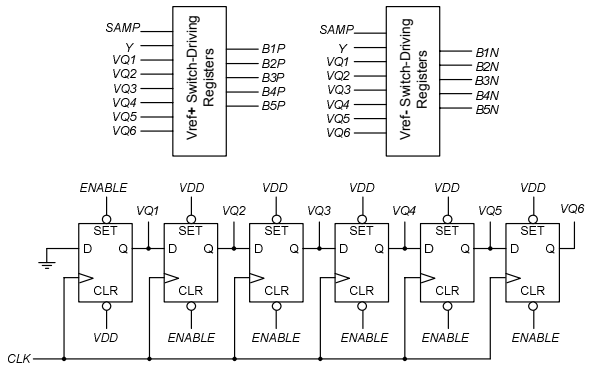


Fig. 4: The main part of SA controller. The cascade DFFs at bottom are the shift registers. The 5-bit Vref+ switch-driving registers and Vref- switch-driving registers control the differential DAC array separately.

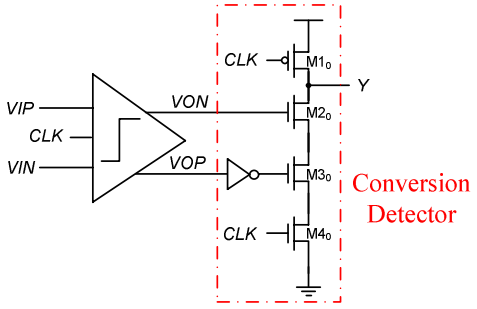


Fig. 5: The NOT gate & $M1_0$~$M4_0$ assemble the conversion detector to follow the comparator.

The schematic of 5-bit Vref+ switch-driving registers is shown as Fig. 6. It is composed of five branches, and each branch is working with the same mechanism. The operation

of first branch is described below. During sampling, transistors $M2_{1P}$ reset B1P to low, $M6_{1P}$ pre-charge the drain of $M5_{1P}$ to prevent charge sharing effects happening to $M3_{1P}$ & $M4_{1P}$ being turned on. During SA cycling, transistors $M1_{1P}$ provide VDD charging path for B1P upon the rising edges of VQ1. While the comparator is regenerating, $M5_{1P}$ put B1P in known state through the inverted output $\overline{Y}$ of conversion detector instantly therefore the self-timing function could be attained.

The schematic of 5-bit Vref- switch-driving registers is shown as Fig. 7, whose working mechanism is similar with the 5-bit Vref+ switch-driving registers but the working voltage is inverted. The little difference here is at the first cycle of SA, transistors MS2, MS3, MS4 & MS5 reset B2N, B3N, B4N & B5N to high.

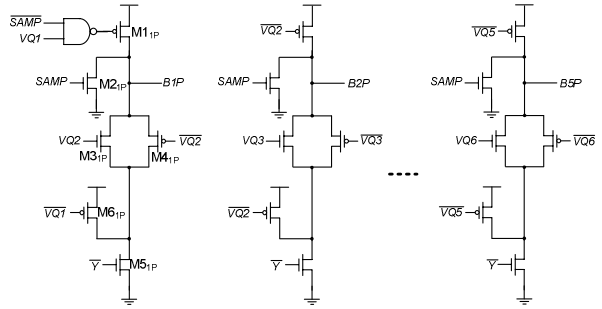


Fig. 6: The schematic of 5-bit Vref+ switch-driving registers.

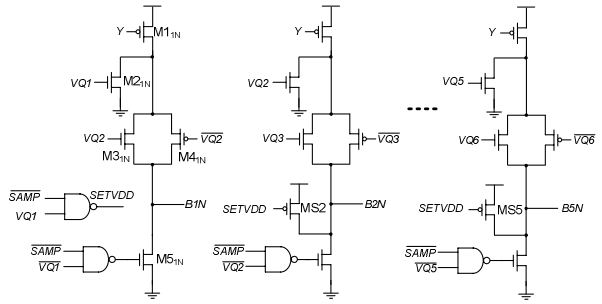


Fig. 7: The schematic of 5-bit Vref- switch-driving registers.

The timing diagram of the 5-bit SAR ADC is shown as Fig.8, which consists of the sampling operation and the first three SA cycle. While SAMP is high and ENABLE is low, the analog input signal is sampled into the capacitive DAC array, all shift registers and switch-driving registers reset to clear the memory effect. When ENABLE becomes high, the successive approximation starts, and the rising edge of CLK will trigger comparator and shift registers in each SA cycle. This timing-diagram shows three possible outcomes of the comparators (i.e. high, low and metastable) to demonstrate the working principles of the proposed circuits. For example, at the first SA cycle, the differential output of comparator is low, transistors $M2_0$ and $M3_0$ of conversion detector turn on concurrently, thus charging $Y$ to low and eventually setting B1P to "0" and B1N to "1". At the second SA cycle, the differential output of comparator is high, $M2_0$ and $M3_0$ keep

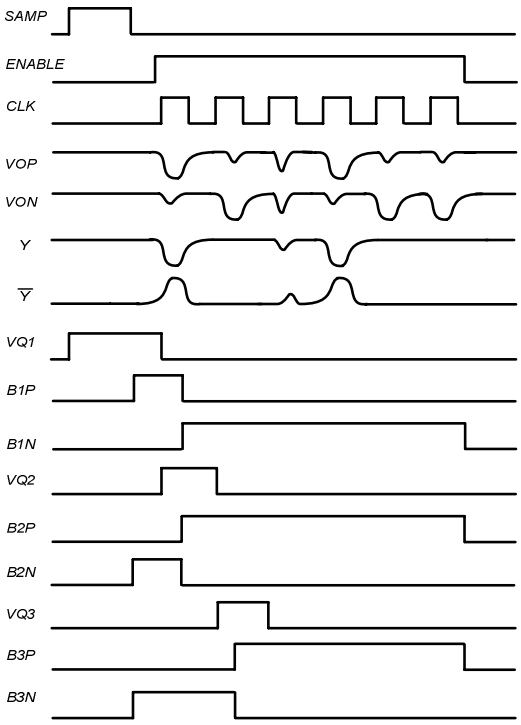


Fig. 8: Timing diagram of 5-bit SAR ADC utilizing proposed switch drive registers.

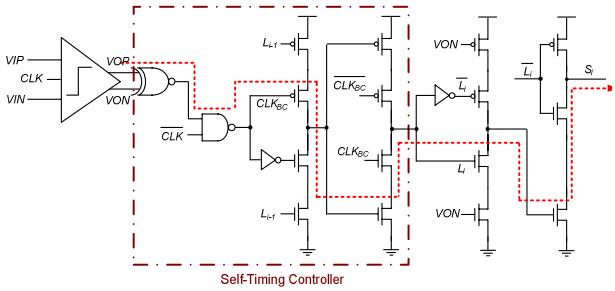


Fig. 9: The signal path from the comparator to the output of the switch-driving registers in [8].

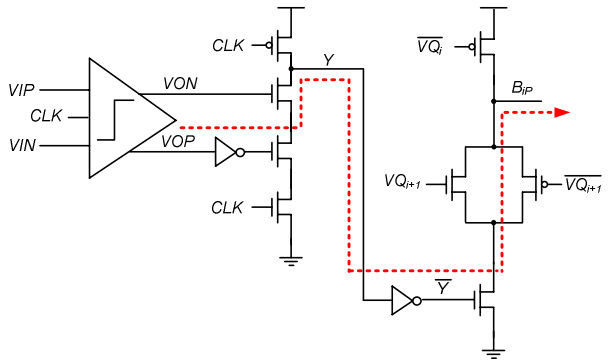


Fig. 10: The signal path from the comparator to the output of the proposed self-timing switch-driving registers.

off at the same time, after that *Y* maintains high moreover holding B2P on "1" and B2N on "0". At the third SA cycle, the comparator is metastable, transistor $M2_0$ switches off but $M3_0$ switches on, so the conversion detector output *Y* preserves high then sustaining B3P at "1" and B3N at "0".

The proposed circuit can improve the speed of the SA loop by the reduction of the propagation delay, compared to the design in [8] as shown in Fig. 9. Since the self-timing controller inserted several logic gates into the critical signal path, the total number of transistors in the path is about 12. The output signal path of the proposed self-timing switch-driving register is shown as Fig. 10, and its total number of transistors in the signal path is about 6 only. The delay of one transistor is around 10ps in 90nm CMOS process, hence the proposed circuit can achieve around 60ps reduction in propagation delay, and this would significantly improve the speed of the SAR ADC since such propagation delay will be appeared in each SA cycle. Fig. 11 shows the comparison of propagation delay between the proposed circuit and [8] in simulation of TT, FF & SS models. Apparently, the speed of proposed circuit is faster than [8] by above 50%.

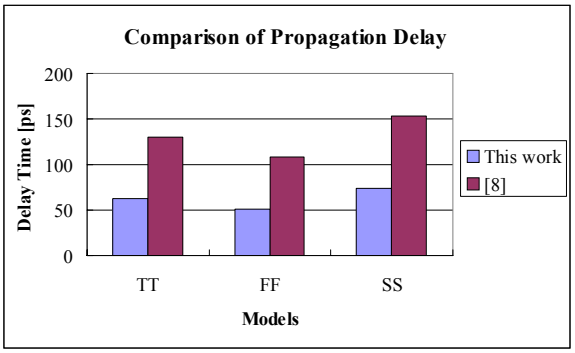


Fig. 11: Comparison of propagation delay between [8] and proposed self-timing switch-driving register in simulation of TT, FF SS models.

## IV. SIMULATION RESULT

The proposed self-timing switch-driving register has been implemented into a 5-bit SAR ADC and simulated at full transistor-level using a 90nm CMOS process. For utilizing the fully-differential architecture, the full scale differential input range of the SAR ADC is set to $1.2V_{PP}$ at 0.6V common voltage, which means that Vref+ = 0.9V and Vref- = 0.3V. The capacitive DAC array is employed by binary-weight structure whose unit-capacitor is 25fF using MOM capacitors. The SNDR of Nyquist input frequency achieve 30.3dB at 285 MS/s sampling-rate. Including the power of reference ladder, the total power consumption of the SAR ADC is 10.5mW. The performance of the SAR ADC has been listed in TABLE1.

## V. CONCLUSIONS

This paper presents a novel self-timing switch-driving register by precharge-evaluate logic circuit, which can avoid the uncertainty (metastability) of comparator, relax the settling time of capacitive DAC array by applying the self-timing principle, and provide a shorten propagation delay path from comparator output to the DAC array of SAR ADC.

| | |
|---|---|
| **Technology** | 90nm CMOS |
| **Resolution** | 5-bits |
| **Supply voltage** | 1.2V |
| **Input Range** | 1.2Vpp |
| **Sampling Frequency** | 285MS/s |
| **Input Frequency** | 142MHz |
| **ENOB** | 4.7bit |
| **SNDR** | 30.3dB |
| **Total Power** | 10.5mW |

TABLE I: PERFORMANCE OF SAR ADC IMPLEMENTED BY PROPOSED CIRCUITS


### ACKNOWLEDGMENT

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