27.3 A Piezoelectric Energy-Harvesting Interface Using Split-Phase Flipping-Capacitor Rectifier and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3× Energy-Extraction Improvement

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Piezoelectric energy harvesters (PEH) exhibit promising features to scavenge the ambient vibration energy for ubiquitous miniaturized internet of things (IoT) devices. For the traditional PEH using a full-bridge rectifier (FBR), the inherent capacitance (C_P) limits the extractable AC-DC electrical power. By extending the damping duration, PEH interfaces employing non-linear techniques, such as the parallel-synchronized-switch harvesting-on-inductor (P-SSHI) [1], can increase the harvestable energy. However, they typically require bulky external high-Q inductors to enhance the extracted power. Recently, various inductor-less PEH interfaces exploiting only capacitors for flipping the PEH voltage during the zero-crossing of the PEH current (I_P) have been reported [2-4]. However, their achievable energy extraction improvement depends highly on the number of flipping phases. This work proposes a split-phase flipping-capacitor rectifier (SPFCR) implementation entailing only 4 capacitors, while achieving the highest number of phases (21) when compared to prior art [2-4]. To resolve the lack of input power (P_{in}) adaptability in [2-4], this work proposes a capacitor-reuse multiple voltage-conversion-ratio (VCR) switched-capacitor (SC) DC-DC converter to reduce the charge redistribution loss. Maximum power point tracking (MPPT) is also accomplished using the fractional FBR open circuit voltage ($V_{OC,FBR}$) for relaxed voltage tolerance, while raising the PEH extracted energy. This work demonstrates a measured 9.3× energy-extraction improvement when compared to a conventional FBR interface.

Figure 27.3.1 depicts our PEH system that consists of 4 flying capacitors (C_{1-4}), an AC-DC rectifier, a mode selector, a phase generator, two switch arrays with drivers, as well as a MPPT arbiter. Generally, a DC-DC converter is necessary to reduce the efficiency loss due to the mismatch between the system output V_{OUT} and the PEH MPP voltage (V_{MPP}). As the PEH voltage flipping time (t_{FLIP}) is typically less than 10% of the external excitation period to ensure a large conduction time, both SPFCR and SC DC-DC operations can be realized using the same capacitors (C_{1-4}). Theoretically, PEH achieves maximum power at $V_{OC}/2$, and the fractional V_{OC} MPPT approach is widely used for its simplicity. However, as V_{OC} is twice the nominal V_{MPP}, high voltage devices or device stacking is necessary; inevitably jeopardizing the system cost and/or robustness. This problem is even worse for PEH interfaces similar to P-SSHI, with the PEH voltage biased to be much higher than that in conventional FBR implementations. As shown in Fig. 27.3.1, there exists an empirical ratio between $V_{MPP,SPFCR}$ and $V_{OC,FBR}$ (depending on the PEH characteristics and interface parameters) which is almost constant over a wide P_{IN} range. We exploit this correlation for efficient MPPT without sustaining a high $V_{OC,SPFCR}$.

For capacitive PEH interfaces, different flying capacitors (C_{FLY}) are conventionally connected to bias the PEH with equal voltage steps [2-4], leading to inefficient voltage flipping. Figure 27.3.2 presents the capacitor reconfiguration examples from [2] and the proposed capacitor phase splitting technique using three C_{FLY} during the first-half of the positive transition cycle (PTC) of I_P. By systematically arranging C_{FLY}, we can generate extra augmented phases (i.e. connecting different number of flying capacitors in series) and extended phases (i.e. connect one single capacitor in each phase instead of parallel connections) during the sharing/recharging period. This work implements a 21-phase SPFCR using only 4 flying capacitors (out of the theoretical 31) taking into consideration the voltage flipping efficiency and the implementation complexity.

Figure 27.3.3 displays the MPPT arbiter and its operation, which harnesses the correlation between $V_{OC,FBR}$ and V_{MPP}. It comprises of a C_P reset circuit, a peak detector, a capacitive divider, and a 3-level ADC with processing. The exertion of V_{RST} triggers V_M when $I_P = 0$, enabling the MPPT arbiter while disconnecting the rectifier and capacitors from the PEH. The peak detector samples the peak-to-peak PEH V_{OC}, as in conventional FBR operation. The sampled voltage (V_S) is further processed by the capacitive divider, and subsequently compared with V_{REF} to determine the best VCR that matches V_{OUT} with $V_{MPP,SPFCR}$. One extra excitation cycle is used to reduce the residual V_S error during sampling. V_{OUT} is regulated using pulse frequency modulation (PFM) with an external f_S for testing flexibility. The pulse generator block employs differential pulse-delay cells (10 each) followed by a digital processing block to generate the required 21 sequential digital pulses, which can be also adjusted externally. The mode selection block generates V_{MODE} by utilizing the ϕ_{-10} and ϕ_{10} signals, with proper delays, to ensure robust mode switching. For the SC DC-DC converter, the implemented VCRs are {2, 1, 2/3, 1/3}, mainly determined by the flying capacitor voltages at the end of the 21-phase SPFCR ($V_{C1} = 0.27 \cdot V_{RECT}$, $V_{C2} = 0.32 \cdot V_{RECT}$, $V_{C3} = 0.19 \cdot V_{RECT}$ and $V_{C4} = 0.1 \cdot V_{RECT}$). This can reduce the charge redistribution loss due to the capacitor voltage mismatch during the SPFCR and SC DC-DC operations. Figure 27.3.3 also shows the capacitor utilization at different VCRs. At 2×, C_{EQ1} (i.e. C_{1-4} connected in series) is charged up during ϕ_C, and stacked on top of V_{RECT} to generate V_{OUT} at ϕ_D. This can significantly reduce the charge redistribution loss when compared with parallel-connected C_{1-4}. Similarly, we use C_{EQ2} (C_2) and C_{EQ3} (C_3 in series with C_4) at VCR = $^1/_3$ and $^2/_3$, and disconnect all C_{1-4} at VCR = 1.

The proposed PEH interface with a 21-phase SPFCR is fabricated in 0.18μm 1.8/3.3/6V CMOS, occupying an area of 0.2mm^2. We placed the MIDE PEH (PPA-1021) on a shaker at an excitation frequency (f_{EX}) of 200Hz. Each C_{1-4} is 68nF, and the corresponding C_P, C_R and C_L are 22, 100 and 30nF. The 1.5V supply powers the phase generator for flexible delay adjustment. Figure 27.3.4 plots the SPFCR operation with the 21-phase voltage flipping steps at $V_{OUT} = 2V$ and an acceleration (a_G) of 0.12g; as well as the corresponding PEH voltage swing before (VCR = 2) and after (VCR = $^2/_3$) MPPT. The extracted ratio between $V_{MPP,SPFCR}$ and $2 \cdot V_{OC,FBR}$ from measurement demonstrates a pseudo-constant relationship within 2.2-2.35 with $P_{IN,FBR} > 0.4\mu W$ (a_G varying from 0.08-0.19g), which can lead to ~2% energy loss when compared to the exact MPP case. As $P_{IN,FBR}$ drops, the ratio reduces due to the excessive control loss, resulting in up to 25% MPPT energy loss when $P_{IN,FBR} = 0.1\mu W$ ($a_G = 0.05g$). As observed, the $V_{RECT,SPFCR}$ (3.2V) is successfully biased to ~2.3× of $2 \cdot V_{OC,FBR}$ (1.4V) after MPPT, which is consistent with the extracted $V_{MPP,SPFCR}$. Figure 27.3.5 shows the measured P_{OUT} under different V_{RECT}, achieving a MOPIR of up to 9.3× at $a_G = 0.12g$ and $V_{OUT} = 1V$. The MPP at $V_{OC,SPFCR}/2$ can clearly be observed, and $V_{OC,SPFCR}$ can exceed the device breakdown voltage at strong vibrations ($a_G = 0.16g$). With a wide P_{IN} range (measured using FBR), the proposed PEH system can improve the achievable MOPIR using different VCRs, with a slight drop at low $P_{IN,FBR}$ due to the increased intrinsic loss. The FCR can deliver up to 64μW at $f_{EX} = 200Hz$ and $a_G = 0.16g$. Figure 27.3.6 show a table summarizing key chip characteristics and performance benchmarks. Without a bulky external inductor, this work achieves a high MOPIR of 9.3× compared to [2-3]. Instead of 8 capacitors to achieve 17 phases as in [4], this work demonstrates a 21-phase SPFCR operation using half the capacitors. It also features multiple-VCR SC DC-DC and $V_{OC,FBR}$-based MPPT, improving the system P_{IN} adaptability without using extra passives nor tolerating excessively high V_{OC}. Figure 23.3.7 shows the die micrograph.

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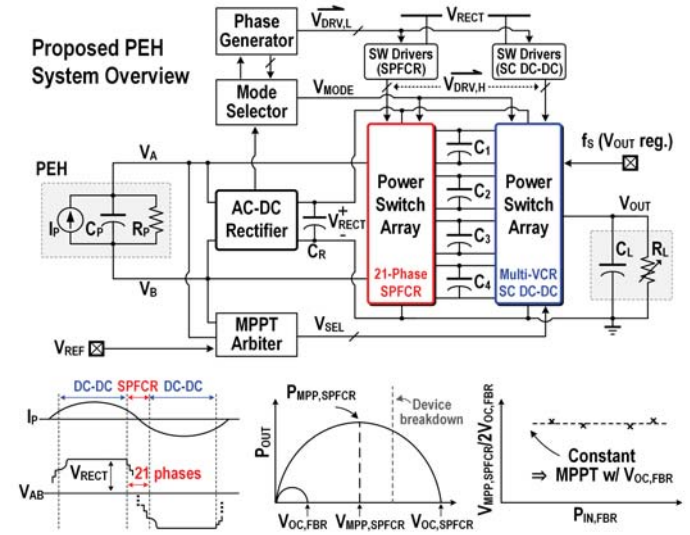

Figure 27.3.1: Proposed split-phase flipping-capacitor rectifier (SPFCR) for piezoelectric energy harvesting with capacitor-reuse SC DC-DC and MPPT.

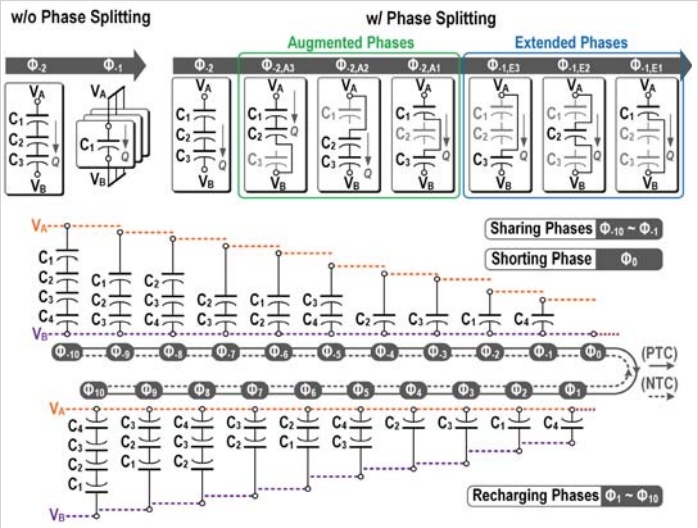

Figure 27.3.2: Proposed SPFCR with 3 C_{FLY} during half PTC (top); and 21-phase SPFCR for both the positive/negative transition cycles (PTC/NTC) (bottom).

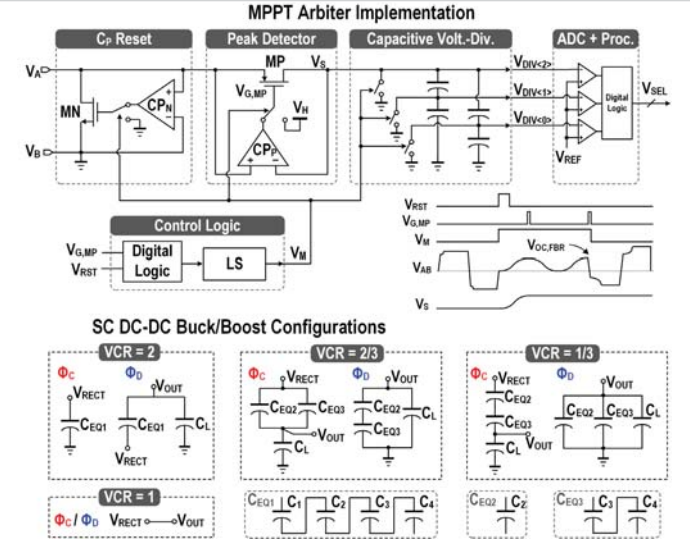

Figure 27.3.3: MPPT arbiter implementation (top) and SC DC-DC configurations (bottom).

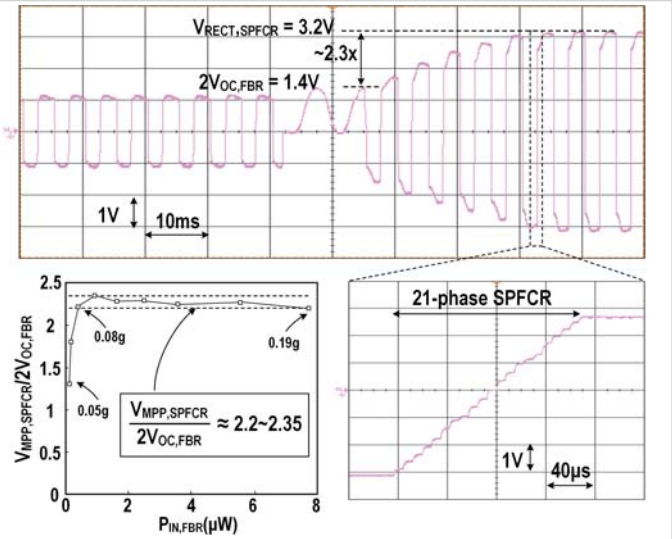

Figure 27.3.4: Measured MPPT operation (top); the 21-phase SPFCR and the extracted ratio between $V_{MPP,SPFCR}$ and $2 \cdot V_{OC,FBR}$ at VCR = 1 (bottom).

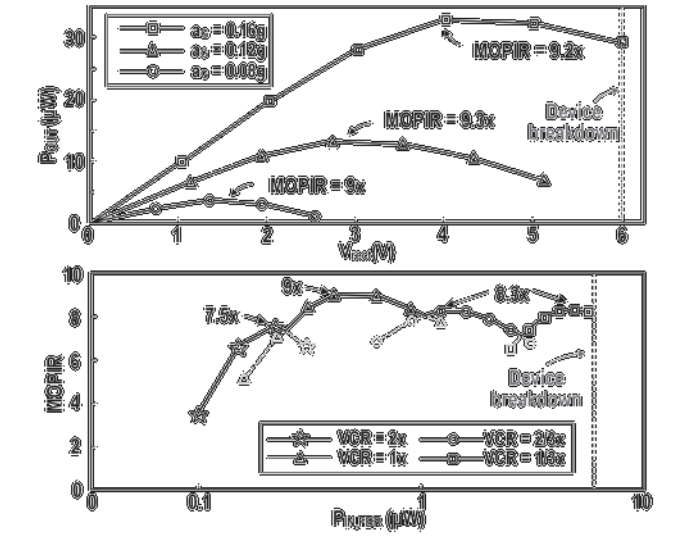

Figure 27.3.5: Measured P_{OUT} vs. V_{RECT} at different a_G (top); and MOPIR vs. $P_{IN,FBR}$ with VCR = {2, 1, $^2/_3$, $^1/_3$} at a_G = 0.05-0.19g and V_{OUT} = 2V (bottom).

	This work	JSSC'17 [4]	JSSC'17 [2]	ISSCC'18 [3]	ISSCC'16 [1]
Technology	**0.18 µm**	0.35 µm	0.18 µm	0.18 µm HV	0.35 µm
Energy Extraction Technique	**SPFCR**	SSHC	FCR	SE-SSHC	P-SSHI
Piezoelectric Harvester	**MIDE PPA1021**	MIDE V21BL	Piezo Systems Inc. (P5A4E @ 5mm^3)	Custom MEMS	MIDE V21B & V22B
Key Component	**4 Capacitors 21 phase**	8 capacitors 17 phase	4 Capacitors 7 phase	8 Capacitors 17 phase	Inductor
MOPIR	**9.3x**	9.7x	4.83x	8.21x	6.81x
P_{in} adaptation	**Capacitor-reuse Multi-VCR SC DC-DC**	no	no	no	Shared inductor
MPPT	**yes**	no	no	no	yes
Chip Size	**0.2 mm^2**	2.9 mm^2	1.7 mm^2	5.3 mm^2	0.72 mm^2
Output Power	**0.5 to 64 µW**	161.8 µW	50.2 µW	186 µW	160.7 µW
Operating Freq.	**200Hz**	92 Hz	110 kHz	219Hz	225 Hz

Figure 27.3.6: Performance summary and benchmark with prior art.

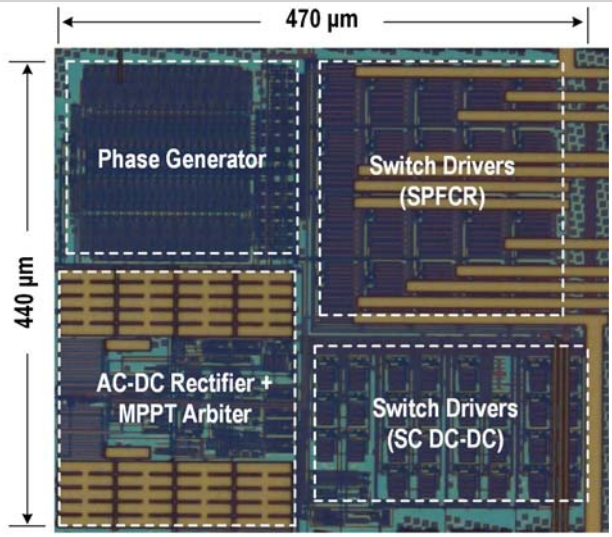

Figure 27.3.7: Die micrograph of the proposed PEH interface in 180nm 1.8/3.3/6V CMOS.

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