Design and Optimization of a Class-C/D VCO for Ultra-Low-Power IoT and Cellular Applications

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***Abstract*—The proper analysis of design tradeoffs of Voltage-controlled oscillators (VCOs) embedded in state-of-the-art multi-standard transceivers is tedious and impractical, as a large amount of conflicting performance figures obtained from multiple modes, test benches and/or analysis must be considered simultaneously. In this paper, the performance boundaries of a complex dual-mode class-C/D VCO are extended using a framework for automatic sizing of radio-frequency (RF) integrated circuit (IC) blocks, where an all-inclusive test bench formulation enhanced with a measurement processing system enables the optimization of "everything-at-once" towards its true optimal tradeoffs. The dual-mode design and optimization conducted provided 512 design solutions with figures-of-merit above 192 dBc/Hz, pushing this topology to its performance limits on a 65 nm technology, by reducing 24% of the power consumption of the original design, while also showing its potential for ultra-low power, with more than 94% reduction.**

I. Introduction

VCOs play a key role in modern RF IC multi-standard transceivers, and, therefore, are subject to continuous research efforts that push the boundaries of their multifaceted performance/power efficiency in state-of-the-art applications and integration technologies. Usually, different wireless systems have various requirements for the VCO performance. For IoT applications, the VCO should maintain a low power consumption while the phase noise (PN) performance can be quite relaxed, e.g., −102 dBc/Hz at 2.5 MHz offset for the Bluetooth low energy receiver at 2.4 GHz carrier frequency [1]. On the other hand, Cellular applications require very stringent PN performance, e.g., −162 dBc/Hz at 20 MHz offset at 900 MHz carrier frequency for the GSM transmitter (TX) [2] and −160 dBc/Hz at 30 MHz offset at 2 GHz carrier frequency for the LTE/WCDMA TX [3].

To overcome the difficulties found on manual sizing of RF circuits, which iterates over designer-defined analytical equations, as shown in Fig. 1(a), different optimization-based electronic design automation (EDA) approaches were applied to efficiently explore the design space [4-5]. They can be applied over performance models that capture several circuit and inductor characteristics [6], however, the use of foundry-provided device models and a circuit simulator as evaluation engine proved to be the most accurate and widely adopted approach for RF [7–9]. Nonetheless, designers often end up using EDA tools to solve only sub-problems of the manual design, i.e., change a sub-set of the design variables, ***x***, to tackle isolated optimizations, as shown on Fig. 1(b). This mixed iterative/sequential optimization design leads to sub-optimal solutions, as the tradeoffs between conflicting performance figures can't be properly weighted. Therefore, for modern VCO applications this approach doesn't fit, as more complex topologies and a wider set of requirements must be simultaneously balanced, e.g., multi-mode operation or attain a limit frequency pushing due to supply voltage variation.

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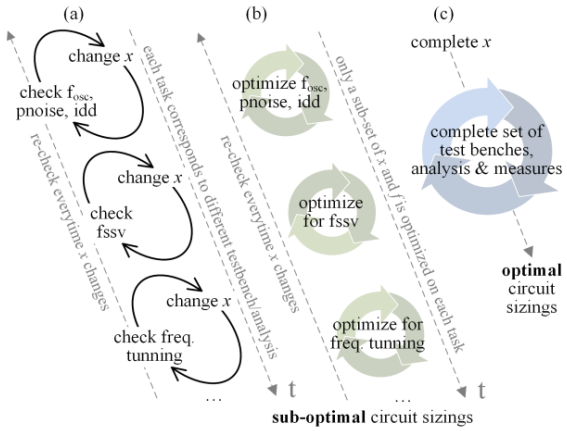

Fig. 1. (a) Knowledge-based manual design; (b) mixed iterative/sequential optimization design approach; and (c) adopted optimize "everything-at-once" approach, where x is the design variables' array.

This paper applies an EDA framework to bypass the difficulties faced on the sizing of complex RF IC blocks, and, particularly, a dual-mode Class-C/D VCO for state-of-the-art IoT and Cellular specifications is here designed and optimized. The possibility to meet extreme operational requirements with the same framework setup is discussed, by analyzing the complete tradeoffs between power consumption, PN and frequency pushing, obtained with a many-objective optimization. The adopted EDA methodology enables the optimize "everything-at-once" approach of Fig. 1(c), leading to a more systematic design flow that reduces the risk of bad design decisions while balancing all design challenges simultaneously. The remainder document is organized as follows. In section II, we introduce the problem definition of the Class-C/D VCO design and the architecture of the EDA framework. Afterwards, in section III, we provide the optimization results, and, finally, in section IV, we address the conclusions.

II. Automatic Design Methodology

Fig. 2 introduces the schematic of the VCO where we applied the proposed optimization method. We used a low supply voltage of 0.35 V to achieve a power-efficient design, in a 65 nm CMOS technology design kit. The VCO can operate in either the class-C or class-D mode depending on the size of M_1/M_2. For IoT applications, we need a small size for M_1/M_2 and the VCO operating in the class-C mode to reduce the power consumption. For Cellular applications, a larger size of M_1/M_2 is necessary to enable the VCO operating in the class-D mode, which boosts the output swing to ~$3V_{DD}$ thus reducing the PN [10]. We also employ a 4-bit binary-sized switched-capacitor array (SCA) together with A-MOS varactors to tune the VCO frequency from 3.8 to 4.9 GHz continuously. The SCA biasing voltage V_{DDH} and V_{DDL} are 1 V

and 0.5 V, respectively. The inductor topology adopted is an octagonal spiral inductor in ultra-thick metal and the inductor model provided by the foundry supports the change of different dimension parameters.

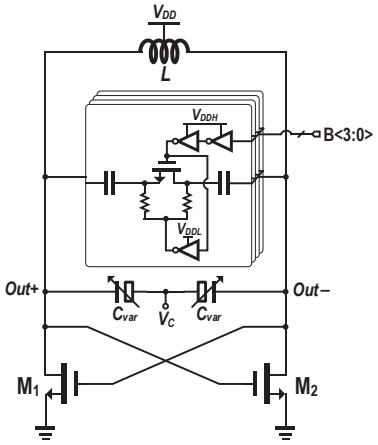

Fig. 2. Dual-mode class-C/D VCO with SCA for increased tunning range.

A. Design Variables

The netlist of the VCO was fully parameterized (LC tank, 4-bit binary-sized SCA and SCA control) using a commercial IC design suite and the netlists exported. In total, there are 28 optimization variables related to the sizing of 43 devices. Table I details the limits and ranges of each variable.

TABLE I. OPTIMIZATION VARIABLES & DESCRIPTION

Variable	Units	Min.	Grid	Max.
ind_radius[1]	µm	15	5	90
ind_nturns[1]	-	1	1	6
ind_spacing[1]	µm	2	1	4
ind_width[1]	µm	3	1	30
mccl[2], **m1l**[5]	nm	60	20	240
mccw[2], **m1w**[5]	µm	0.6	0.2	6
mccnf[2], **m1nf**[5]	-	1	1	32
mccm[2]	-	1	1	100
moscapw[3]	µm	0.4	0.2	3.2
moscapl[3]	µm	0.2	0.2	3.2
mimvw[4], **mimvl**[4], **mim1w**[6]	µm	2	0.2	20
r1l[7], **r2l**[7], **r3l**[7], **r4l**[7]	µm	1	0.2	10
r1m[7], **r2m**[7], **r3m**[7], **r4m**[7]	-	1	1	20
nfn1[8], **nfn2**[8], **nfp1**[8], **nfp2**[8]	-	1	1	100

[1]**ind_radius**, **ind_nturns**, **ind_spacing** and **ind_width** are the inner radius, number of turns, spacing between conductors and conductor width, respectively, of the inductor L; [2]**mccl**, **mccw**, **mccnf** and **mccm** are the length per finger, width per finger, number of fingers and device multiplier, respectively, of the cross-coupled M_1/M_2 transistors; [3]**moscapw** and **moscapl** are the width and length per finger (for 8-finger structures), respectively, of the varactors; [4]**mimvw** and **mimvl** are the width and length, respectively, of the MIM capacitors of the tank; [5]**m1l**, **m1w** and **m1nf** are the length per finger, width per finger and number of fingers, respectively, of the N-type transistors from the 4-bit SCA, using a device multiplier ratio of 8:4:2:1; [6]**mim1w** is simultaneously the width and length of the MIM capacitors from the 4-bit SCA, using device multiplier ratio of 8:4:2:1; [7]**r1l** and **r1m** are the segment length and multiplier, respectively, for a fixed segment width of 0.5 µm of the resistors from the 1st bit of SCA. **r2l**, **r2m**, **r3l**, **r3m**, **r4l** and **r4m** are the respective variables for the 2nd, 3rd and 4th bits; [8]**nfn1/nfp1** are the number of fingers from N-type/P-type transistors from the VDDH inverters of the 4-bit SCA, for a fixed length per finger of 60 nm and width per finger of 500 nm. **nfn2** and **nfp2** are used for the VDDL inverters.

B. Test benches and Measurements

For each different tuning frequency of the SCA control B<3:0>, we define two different test benches. In the first, we perform a steady-state (SST) and SST noise analysis to extract the f_{osc}, PNs and power for the standard supply voltage, and, in the second test bench, we only perform a SST analysis to extract the f_{osc} for a supply voltage of 0.4 V. These test benches are henceforward designated by SST@0.35_{bxxxx} and SST@0.40_{bxxxx}, respectively. To optimize the complete tuning range meticulously, 32 test benches would be required to sweep all combinations from SCA control. However, as a proof of concept, only the 4.9 GHz (B<0000>) and 3.8 GHz (B<1111>) tunings are here detailed and used for optimization. Table II schematizes the complete list of measurements adopted. We used the processing that will be introduced in section II.D to define two distinct measures, firstly, frequency sensitivity due to a supply variation, *fssv*, of 50 mV:

$$fssv = \left| \frac{f_{osc}@Vdd_2 - f_{osc}@Vdd_1}{Vdd_2 - Vdd_1} \right| \quad [Hz/V] \tag{1}$$

where $f_{osc}@Vdd_1$ is the oscillation frequency at reference supply voltage Vdd_1, i.e., 0.35 V, and $f_{osc}@Vdd_2$ at a different supply voltage, i.e., 0.4 V. And, figure-of-merit (FOM), given by:

$$FOM = -10\log\left[\frac{P_{dc}}{1mW}\cdot\left(\frac{\Delta\omega}{\omega_0}\right)^2\right] - L(\Delta\omega) \quad [dBc/Hz] \tag{2}$$

where ω_0 is the oscillation frequency, P_{dc} the power consumption, $\Delta\omega$ is the offset from the output frequency and $L(\Delta\omega)$ is the oscillator PN. The FOM allows to assess the overall performance of the VCO, which is better with a higher absolute value of FOM.

C. Optimization Constraints and Objectives

Table II also details the optimization constraints, which are set on the f_{osc} to meet the desired range, at PNs, and, FOMs above 190 dBc/Hz. Two different sets of objectives for two independent set of optimizations were defined following an experience designer insight: (1) the first targeted for IoT, i.e., ultra-low power consumption with relaxed PN. Therefore, the optimization was set to simultaneously minimize the largest power value measured, maximize the lowest FOM value measured, and, minimize the highest *fssv* value measured (Table III.A). In this case, each PN constraint of Table II is relaxed by 10 dBc/Hz; (2) the second set is targeted for Cellular applications, i.e., stringent PN performance. It is intended to simultaneously minimize the worst PN at 10 MHz value measured, maximize the lowest FOM value measured, and, minimize the highest *fssv* value measured (Table III.B).

Additionally, an alternative setup was defined that targets individual specification figures without attempting to bias the optimization toward either Cellular or IoT specifications. This third set, attempts to meet the two extreme specifications, i.e., Dual-mode, by minimizing the largest power value measured, minimize the worst value of PN at 10 MHz measured, and, minimize the highest fssv value measured (Table III.C). In this case the FOM is inherently optimized.

D. Optimization Framework

Fig. 3 illustrates the proposed design methodology, built over a framework for the automatic synthesis of analog ICs, AIDA [11]. The architecture represents K test benches as parameterized netlists with common $\boldsymbol{x}$. All circuit netlists and test benches required for optimization can be exported from a common IC design suite, e.g., Cadence™, and are specific to a simulator. Moreover, the native simulator measure descriptions necessary to obtain the measure values are also incorporated in the netlist(s) setup. At each iteration of the optimization process, the framework simulates all the test benches in parallel or sequentially, using Cadence's Spectre®, Mentor Graphics' Eldo® or Synopsys HSPICE®, as parsers were internally developed for each of the output standard formats, i.e., .MDL, .AEX and .MEASURE, respectively, for each supported simulator. The measured values are then passed to the measure processing unit to obtain the circuit's performance expressions that define the objectives and constrains, that are considered in the evolutionary algorithm. It is important to note that the circuit expressions are always functions of the simulations' output. In the developed framework, the

TABLE II. MEASURES, OPTIMIZATION CONSTRAINTS AND PERFORMANCE COMPARISON

Section II.B				Sect. II.C	Section II.D								
Measure	**Units**	**Description**	**Measured from / Computed by**	**Constraint Target(s)**	***JSSC sim.*[5]**	***JSSC meas.*[6]**	**IoT_a[8]**	**$Dual_a$[8]**	**Cel_b[9]**	**$Dual_b$[9]**	**IoT_c[10]**	**Cel_c[10]**	**$Dual_c$[10]**
$f_{osc}[b_{0000}]$@0.35V	GHz	f_{osc} for b_{0000} at 0.35V supply	SST@0.35V_{0000}	≥ 4.8 ≤ 5.0	4.800	4.800	4.870	4.805	4.807	4.874	4.900	4.958	4.991
$f_{osc}[b_{1111}]$@0.35V	GHz	f_{osc} for b_{1111} at 0.35V supply	SST@0.35V_{1111}	≥ 3.7 ≤ 3.9	3.000	3.000	3.871	3.855	3.853	3.886	3.859	3.703	3.730
$f_{osc}[b_{0000}]$@0.40V	GHz	f_{osc} for b_{0000} at 0.40V supply	SST@0.40V_{0000}	n/d	n/a	n/a	4.852	4.777	4.786	4.853	4.900	4.957	4.991
$f_{osc}[b_{1111}]$@0.40V	GHz	f_{osc} for b_{1111} at 0.40V supply	SST@0.40V_{1111}	n/d	n/a	n/a	3.861	3.839	3.857	3.891	3.859	3.703	3.730
PN[b_{0000}]@10kHz	dBc/Hz	PN at 10KHz for b_{0000}	SST@0.35V_{0000}	≤ -59	n/a	n/a	-74.5	-73.9	-82.0	-82.4	-69.1	-71.5	-71.2
PN[b_{0000}]@100kHz	dBc/Hz	PN at 100KHz for b_{0000}	SST@0.35V_{0000}	≤ -86	-100.0	-90.5	-94.8	-94.8	-102.9	-102.9	-92.5	-97.3	-97.2
PN[b_{0000}]@1MHz	dBc/Hz	PN at 1MHz for b_{0000}	SST@0.35V_{0000}	≤ -108	-124.0	-118.5	-114.8	-114.9	-123.1	-123.0	-113.1	-118.7	-118.7
PN[b_{0000}]@10MHz	dBc/Hz	PN at 10MHz for b_{0000}	SST@0.35V_{0000}	≤ -129	-144.0	-143.5	-134.6	-134.9	**-143.0**	**-143.3**	-133.0	-138.8	-138.6
PN[b_{1111}]@10kHz	dBc/Hz	PN at 10KHz for b_{1111}	SST@0.35V_{1111}	≤ -65	n/a	n/a	-78.0	-77.3	-75.0	-74.6	-74.3	-78.35	-78.8
PN[b_{1111}]@100kHz	dBc/Hz	PN at 100KHz for b_{1111}	SST@0.35V_{1111}	≤ -92	-108.0	-100.5	-98.3	-98.3	-102.2	-101.8	-96.4	-100.9	100.8
PN[b_{1111}]@1MHz	dBc/Hz	PN at 1MHz for b_{1111}	SST@0.35V_{1111}	≤ -113	-129.5	-127.0	-114.8	-118.4	-124.4	-124.1	-116.7	-121.3	-121.2
PN[b_{1111}]@10MHz	dBc/Hz	PN at 10MHz for b_{1111}	SST@0.35V_{1111}	≤ -134	-150.0	-149.5	-137.7	-138.1	**-143.0**	**-143.6**	-136.4	-140.3	-140.2
power[b_{0000}]	mW	Power consumption for b_{0000}	SST@0.35V_{0000}	n/d	2.1[7]	4.0	**0.117**	**0.119**	1.598	1.536	0.188	0.765	0.758
power[b_{1111}]	mW	Power consumption for b_{1111}	SST@0.35V_{1111}	n/d	5.4	6.8	**0.117**	**0.119**	1.597	1.535	0.188	0.767	0.760
fssv[b_{0000}]	MHz/V	Frequency sensitivity for b_{0000}	XML (Fig. 5)[1]	n/d	600	n/a	352	556	422	426	**< 1**	**6**	**2**
fssv[b_{1111}]	MHz/V	Frequency sensitivity for b_{1111}	XML (Fig. 5)[2]	n/d	175	n/a	196	312	86	100	**< 1**	**6**	**2**
FOM[b_{0000}]	dBc/Hz	Figure-of-merit for b_{0000}	XML (Fig. 5)[3]	≥ 190	194.4	191.0	197.7	197.7	194.6	195.2	194.1	193.9	193.7
FOM[b_{1111}]	dBc/Hz	Figure-of-merit for b_{1111}	XML (Fig. 5)[4]	≥ 190	192.2	190.0	198.8	199.0	192.7	193.6	195.4	192.9	192.9

[1] $abs\left[\left(f_{osc}\left[b_{0000}\right]@0.35V - f_{osc}\left[b_{0000}\right]@0.35V\right)/0.05\right]$ [2] $abs\left[\left(f_{osc}\left[b_{1111}\right]@0.35V - f_{osc}\left[b_{1111}\right]@0.35V\right)/0.05\right]$

[3] $-10*\log_{10}\left[\left(power\left[b_{0000}\right]*1E3\right)*\left(10E6/f_{osc}\left[b_{0000}\right]@0.35V\right)\right] - PN\left[b_{0000}\right]@10MHz$ [4] $-10*\log_{10}\left[\left(power\left[b_{1111}\right]*1E3\right)*\left(10E6/f_{osc}\left[b_{1111}\right]@0.35V\right)\right] - PN\left[b_{1111}\right]@10MHz$

[5]Simulation values on a 65 nm technology, 0.4 V supply and tuning range from 3.0 GHz to 4.8 GHz [10]; [6]Measurements on the same conditions of *JSSC sim.*; [7]Value inferred from Eq. (25) of [11], due to its excellent agreement between theoretical and simulated values; [8]Points from the IoT and Dual-mode optimizations with lowest power; [9]Points from the Cellular and Dual-mode opt. with lowest PN; [10]Points from the IoT, Cellular and Dual-mode opt. with lowest *fssv*.

expressions are defined by the designer in the graphical user interface using logical (*conditional statements*, *equal*, *larger* and *smaller*) and arithmetic operators (+, -, /, *). Additionally, operations such as *max*, *min*, *rms*, *mag*, etc., are also supported.

TABLE III. OPTIMIZATION OBJECTIVES FOR IOT APPLICATION, CELLULAR APPLICATION AND DUAL-MODE

A. IoT Application	**Target**	**Units**
Max(power[b_{0000}], power[b_{1111}])	minimize	mW
Min(FOM[b_{0000}], FOM[b_{1111}])	maximize	dBc/Hz
Max(fssv[b_{0000}], fssv[b_{1111}])	minimize	Hz/V
B. Cellular Application	**Target**	**Units**
Max(PN[b_{0000}]@10MHz, PN[b_{1111}]@10MHz)	minimize	dBc/Hz
Min(FOM[b_{0000}], FOM[b_{1111}])	maximize	dBc/Hz
Max(fssv[b_{0000}], fssv[b_{1111}])	minimize	Hz/V
C. Dual-mode	**Target**	**Units**
Max(power[b_{0000}], power[b_{1111}])	minimize	mW
Max(PN[b_{0000}]@10MHz, PN[b_{1111}]@10MHz)	minimize	dBc/Hz
Max(fssv[b_{0000}], fssv[b_{1111}])	minimize	Hz/V

III. RESULTS AND ANALYSIS

In this work, the RF circuit simulator adopted is the Mentor Graphics' Eldo. The three optimizations detailed in the section II.C were carried with populations of 512 elements and optimized for 1000 generations. The Pareto optimal fronts (POFs) of IoT, Cellular and Dual-mode optimizations provided 65, 512 and 512 optimal sizing solutions, respectively, drawn in Figures 4, 5 and 6.

Due to the nature of the FOM metric, on Fig. 4, power consumption is almost linearly correlated with the FOM. The exception is on extreme ultra-low power values (and therefore, ultra-high FOMs) where *fssv* becomes significantly worst, i.e., equal and higher than 140 MHz/V. For Fig. 5, despite the FOM dependency from PN, the POF presents three different regions spreading through different ranges of FOM. At a first glance, the lower region of the figure with better PN values seems to dominate the two other regions, however, due to the dimensionality introduced with the *fssv* it is possible to visualize the boundaries of a tradeoff not explored in previous works.

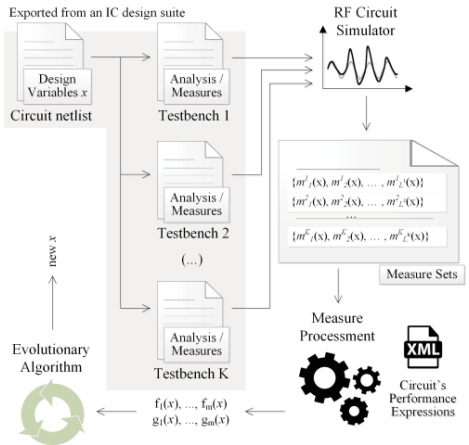

Fig. 3. Framework of the multi-test bench RF IC sizing optimization with measure processing unit.

The Dual-mode POF of Fig. 6 inherently optimized the FOM metric, with all solutions equal or above 192 dBc/Hz. From the projection of Fig. 7 (b) it is clear to observe two distinct regions of the design space, one tailored for IoT application, with power ranging from 0.119 mW to 0.188 mW for worst PN values (between -133.4 dBc/Hz and -135.1 dBc/Hz), and, another region for Cellular application, with PNs ranging from -137.9 dBc/Hz to -143.27 dBc/Hz for worst power values (between 0.508 mW and 1.562 mW). The detailed performances of some sizing solutions from the three optimizations are highlighted in the last columns of Table II. As observable, the Dual optimization matched the best results of both independent optimizations.

The simulated performances of the original publication [10] (*JSSC sim.*) are used as reference values to benchmark the optimized fronts with respect to remaining state-of-the-art in VCO design, even though the circuit was originally sized for a 0.4 V

supply voltage and a 3.0 to 4.9 GHz tuning range, which benefits the PNs especially at the lower range, i.e., B<1111>. The measured performances (*JSSC meas.*) are also highlighted, which provide some insights of expected performance degradation after manufacturing. For a fair comparison, from B<0000> power and PNs of columns *JSSC sim.,* Cel_b^9 and $Dual_b^9$ of Table II, the proposed methodology found solutions with less 23.9% and 26.9% power consumption than original sizing, for similar PN reference values, which is also reflected positively on the FOM. By observing the *JSSC sim.,* IoT_a^8 and $Dual_a^8$ columns of Table 2, the potential to address this circuit in ultra-low power applications is proved, as power consumption was reduced more than 94% in both cases with respect to the original pre-layout design, achieving impressive FOMs above 197.7 dBc/Hz for the higher tuning range, and 198.8 dBc/Hz for the lower. Moreover, when the original circuit is tuned to 3.7 GHz (≈B<1111>), it consumes 3.54 mW pre-layout with a FOM of 192.87 dBc/Hz and 400 MHz/V *fssv*, sub-optimal results when comparing with the optimized ones. Obtained results are extremely promising even when expecting a significant increase in power consumption after manufacturing,.

Finally, in the last columns of Table 2, i.e., IoT_c^{10}, $Cell_c^{10}$ and $Dual_c^{10}$, the points with better *fssv* from each optimization are highlighted. Due to the nature of the many-objective optimizations performed, this complex tradeoff was explored and weighted at each evaluation, achieving solutions with extremely low frequency pushing figures, unlike previously published results [10]. This fact is extremely relevant, as it is one of the most critical issues in the design of class-C/D VCOs for real-life product at low V_{dd} values.

IV. Conclusions

In RF IC manual design, analyzing multiple performance figures through multiple conflicting modes, test benches and/or analysis at once is an unbearable task. This paper promotes an optimize "everything-at-once" approach, and therefore, allowing to properly analyze the optimal tradeoffs between all relevant performance figures. The complex Class-C/D VCO adopted, originally proposed in a renowned international journal of the area, was optimized to comply with IoT and Cellular requirements in a single optimization. Obtained solutions pushed to the limits this circuit topology for a 65 nm CMOS technology. As future research directions, it is desired to perform variability and layout-aware optimization of the VCO, as well as including accurate electromagnetic-simulated [12] inductor performances in-the-loop.

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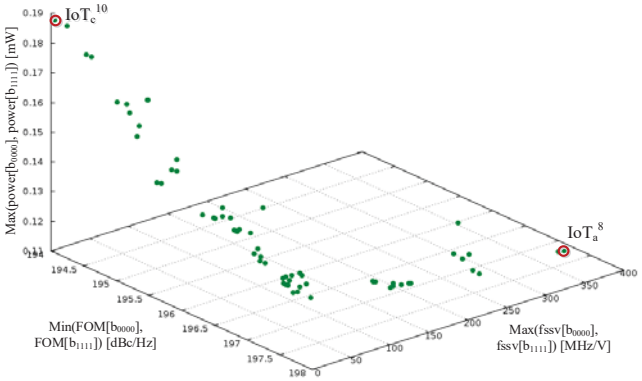

Fig. 4. POF for the IoT tradeoff (Table III.A) with 65 optimal sizing solutions. The solutions spread from 0.117 mW to 0.188 mW power, 194.07 dBc/Hz to 197.76 dBc/Hz FOM, and, < 1 MHz/V to 352 MHz/V fssv.

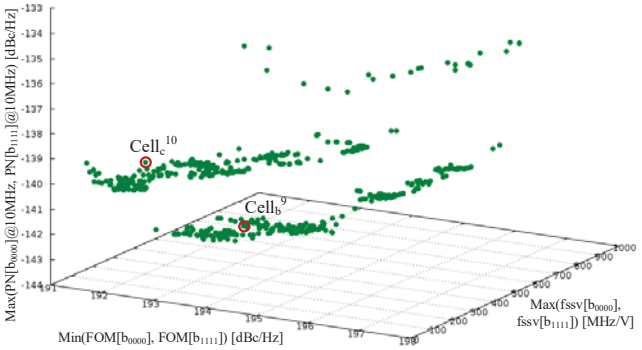

Fig. 5. POF for the Celular tradeoff (Table III.B) with 512 optimal sizing solutions. The solutions spread from -133.42 dBc/Hz to -143.02 dBc/Hz PN, 191.44 dBc/Hz to 197.62 dBc/Hz FOM, and, 6 MHz/V to 918 MHz/V fssv.

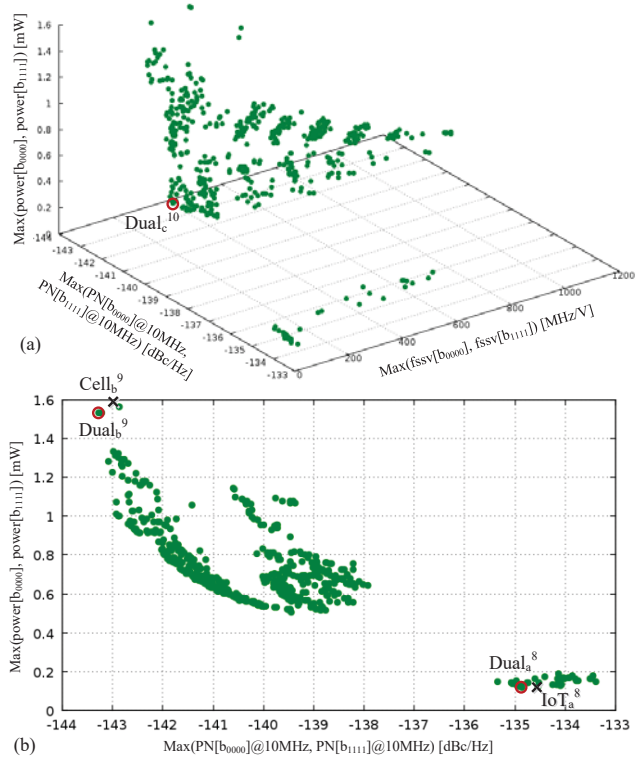

Fig. 6. POF for the Dual-mode tradeoff (Table III.C) with 512 optimal sizing solutions. The solutions spread from 0.119 mW to 1.562 mW power, -133.40 dBc/Hz to -143.27 dBc/Hz PN, and, 2 MHz/V to 1092 MHz/V fssv. (a) 3-D representation; (b) Projection Power vs. PN. IoT_a^8 and Cel_b^9 are overlapped in the figure.