A DC-Offset-Compensated, CT/DT Hybrid Filter with Process-Insensitive Cutoff and Low In-Band Group-Delay Variation for WLAN Receivers

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ABSTRACT

A continuous-time/discrete-time (CT/DT) hybrid channel-selection filter (CSF) with a built-in pole-controllable dc-offset canceller (DOC) for WLAN receivers is proposed. Optimized in a 90-nm CMOS process, a 4th-order CT/DT Hourglass architecture plus one frequency-extended real pole approximates the shape of a generic 5th-order pure CT (active-*RC*) Butterworth structure, while achieving a stable cutoff frequency (i.e., ±10%) without calibration and small in-band group delay variation (i.e., 34 ns). The entire CSF consumes 10.3 mW at 1.2 V. The IIP3 is +15 dBm and the 0.2-mW DOC reduces more than 50% of the dc-offset, while providing a pole controllable feature to flexibly suit the different reception modes of WLAN systems.

1. INTRODUCTION

Wireless local area network (WLAN) receivers require a highly-linear baseband channel-selection filter (CSF) to suppress the power of the adjacent channels such that the dynamic range requirement of the analog-to-digital converter (ADC) can be minimized. However, due to process variation, the CSF's cutoff frequency may vary significantly. In order to desensitize the accuracy of the filter from process variation, a continuous-time/discrete-time (CT/DT) hybrid CSF appears as a promising alternative [1]. By using switched-capacitor (SC) circuits as the DT part, the cutoff frequency will be more stable, potentially eliminating the essential of a *RC*-tuning circuit.

This paper describes the design of a dc-offset-compensated, CT/DT hybrid 4th-order CSF [Fig. 1(a)] using the Hourglass approximation to meet the stopband rejection requirement together with a stable cutoff frequency over process variation, and smaller in-band group delay variation than the "pure" CT active-*RC* 5th-order Butterworth CSF [Fig. 1(b)] that was the general choice of most existing IEEE 802.11a/b/g WLAN systems [2]. The preamble and normal reception modes [3] are accomplished through the introduction of a pole-controllable dc-offset canceller (DOC). The track-and-hold output can be directly digitized by the ADC without necessitating a sample-/track-and-hold circuit.

2. FILTER DESIGN

2.1 CT/DT Hybrid CSF

The schematic of the CT/DT hybrid CSF is shown in Fig. 2. The differential structure starts with a passive-RC real pole followed by a 4th-order Hourglass filter (2 Biquads in cascade). The 1st Biquad is of active-*RC* Tow-Thomas architecture. It is designed to provide 12-dB gain for lowering the overall input-referred noise, and has a servo loop embedded for cancelling the dc-offset generated from the mixer and itself due to unavoidable component mismatches. The real pole and the 1st Biquad also serve as the anti-aliasing filter for the 2nd Biquad that possesses a SC architecture clocked at 160 MHz. The pole-zero plot of the proposed CSF is shown in Fig. 3. A low-Q Biquad followed by another with a high-Q minimizes the filter sensitivity to process variation [4]. The complex zero pair derives from the Hourglass approximation in order to eliminate the passband ripple. The repeated zeros at z=-1 are due to the track-and-hold operation of the 2nd Biquad.

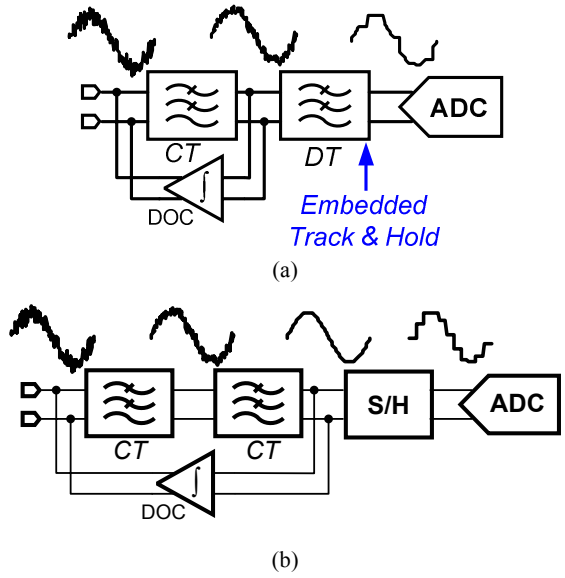

Fig. 1. CSF architecture: (a) proposed and (b) conventional.

2.2 Pole-Controllable DOC

The schematic of the proposed DOC is depicted in Fig. 4. The input stage serves to extract the dc-offset imbalance with a tunable time-constant, whereas the output stage is to feed the correction current signals back to the operational amplifier (OpAmp) at the virtual ground nodes for dc-offset removals.

To interface with the OpAmp's differential outputs that feature high signal swing, the input stage employs resistors R_1 and R_2 for voltage-to-current conversion first. The resultant current signals are then amplified by M_1 and M_2 in a common-gate configuration. M_1 and M_2 are biased in subthreshold region to maximize the output impedance. They, in conjunction with the use of parallel-compensated depletion-mode MOS capacitor C_{MOS} [5] and metal-

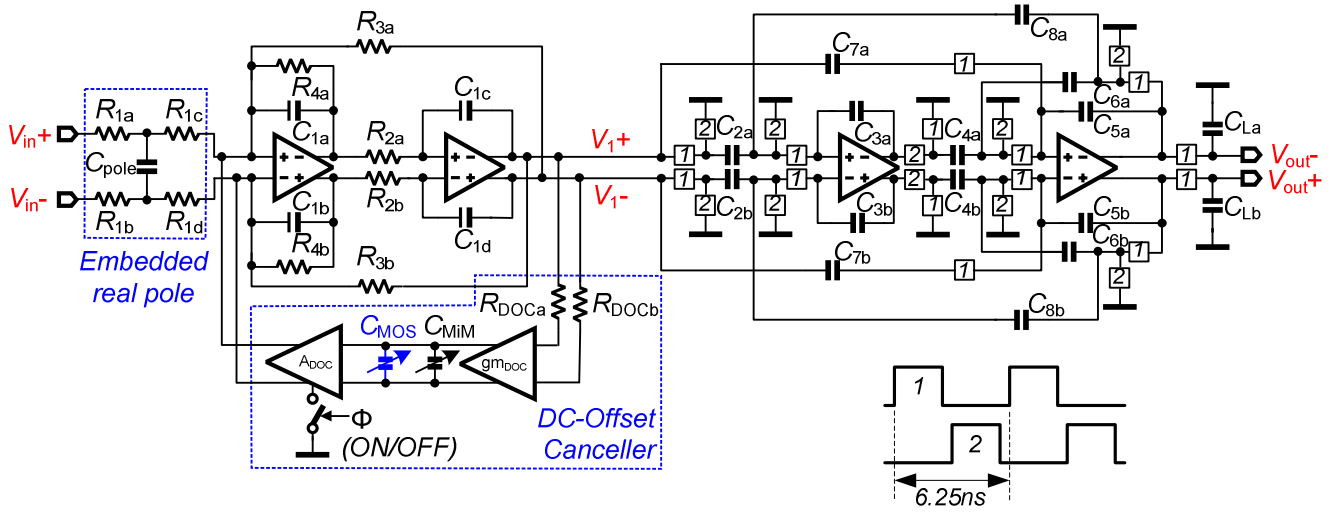

Fig. 2. Schematic of the proposed CT/DT hybrid CSF.

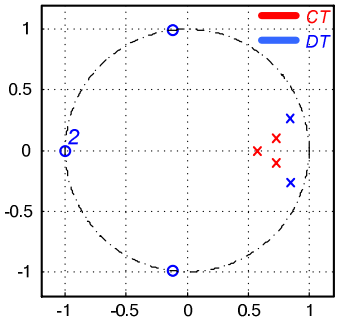

Fig. 3. Pole-zero plot of the proposed CT/DT hybrid CSF.

insulator-metal capacitor C_{MiM}, form a subthreshold-biased *gm-C* integrator that occupies only very small area. Both C_{MOS} and C_{MiM} are made tunable such that the highpass cutoff frequency can be adjusted to be sufficiently low (~10 kHz) in normal reception, while sufficiently large (~1 MHz) for a faster settling in preamble reception mode, in which only pilot tones are received.

The output stage is an output-drain differential pair, where the common source node of M_7 and M_8 provides the common-mode signal that can be feed back to the input stage (through M_3 and M_4)

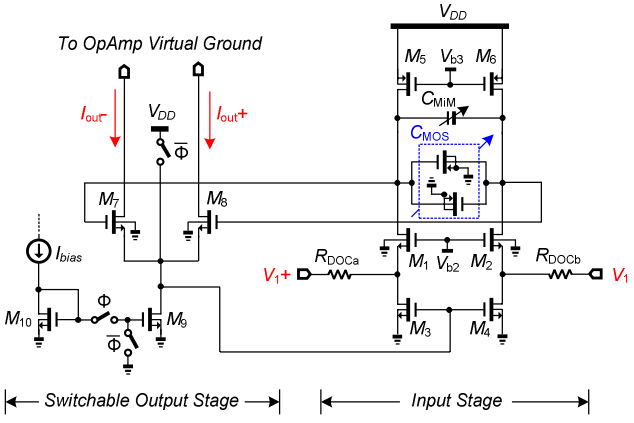

Fig. 4 Schematic of the proposed DOC.

to stabilize the common-mode voltage at the high-impedance node: drain of M_1 and M_2. The output stage is also designed to be switchable (via Φ and $\overline{\Phi}$) such that the DOC can be flexibly added or removed from the OpAmp in a multi-stage filter design.

2.3 DC-Offset Rejection of the Proposed CSF

This section presents the comparison between the dc-offset rejection capability of the proposed CT/DT hybrid filter and the conventional active-*RC* filter. The details are as follows:

Figure 5(a) shows the mathematical model of a generic filter that has the impairment of dc-offset. For the conventional active-*RC* filter, the DOC can be placed around the 1st and 2nd stages. However, for the proposed filter, due to its hybrid nature, it is only convenient to place the DOC just around the 1st stage, as shown in Fig. 5(b) and 5(c). In this model, G_1, G_2 and H denote the DC gain of the two Biquads and the DOC, respectively. $\overline{V_{OS1}}$, $\overline{V_{OS2}}$ and $\overline{V_{OS3}}$ denote the input-referred dc-offset generated by the 1st Biquad and its previous stage (for example a mixer), the 2nd Biquad and the DOC, respectively. The statistical characteristics and correlations of these three variables can be obtained from Monte-Carlo simulations. The equivalent output-referred dc-offset voltages can be derived as follows:

$$\overline{V_{OST1}} = G_1G_2\overline{V_{OS1}} + G_2\overline{V_{OS2}} \tag{1}$$

$$\overline{V_{OST2}} = \frac{G_1G_2\overline{V_{OS1}} + G_2\overline{V_{OS2}} + G_1G_2H\overline{V_{OS3}}}{1+G_1G_2H} \tag{2}$$

$$\overline{V_{OST3}} = \frac{G_1G_2\overline{V_{OS1}} + G_1G_2H\overline{V_{OS3}}}{1+G_1H} + G_2\overline{V_{OS2}} \tag{3}$$

Comparing (2) and (3), we can observe that the dc-offset generated by the 2nd stage will not be suppressed by the DOC. However, since the 1st Biquad is designed to offer 12-dB gain, both the input-referred dc-offset and noise are minimized. Moreover, since SC filters have better matching than their active-RC counterparts, the dc-offset rejection capability of the hybrid filter remains roughly the same, as confirmed by the simulation results given in the next section.

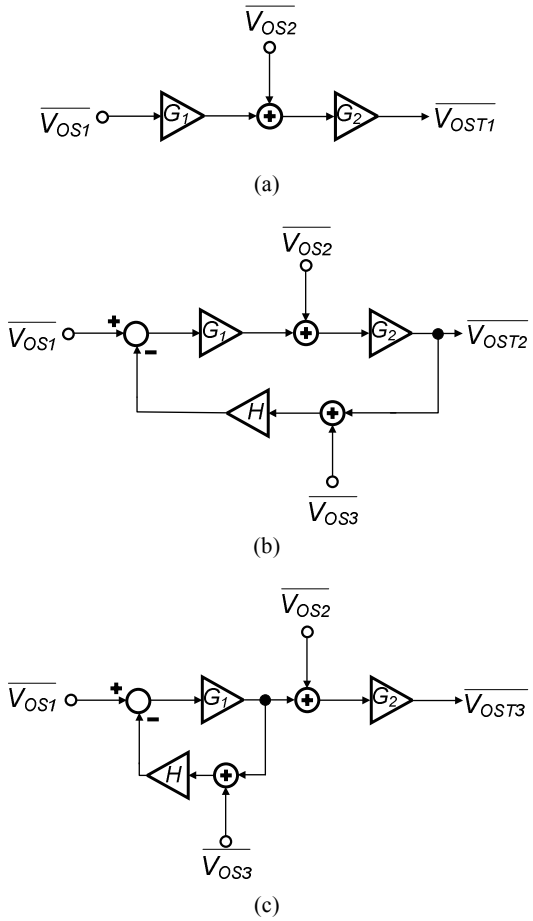

Fig. 5. Mathematical model of generic CSF: (a) without DOC, (b) DOC closes the 1st and 2nd stages. (c) DOC closes the 1st stage only.

3. SIMULATION RESULTS

To demonstrate the advantages of the proposed CT/DT hybrid Hourglass CSF, a 5th-order active-*RC* Butterworth CSF that meets the same specification is designed for comparison. This section summarizes the simulation results obtained in *Cadence* based on the ST 90-nm CMOS General-Purpose process with *Spectre* as the simulator. The supply voltage is 1.2 V.

3.1 OpAmp

The 1st Biquad employs a generic two-stage OpAmp, which shows 68-dB midband gain, 578-MHz unity-gain frequency and 61° phase margin at 2-pF load. The 2nd Biquad employs a gain boosted folded-cascode OpAmp. Its common-mode feedback (CMFB) circuit exhibits a typical SC structure that consumes no static power. The key performance metrics are 60-dB midband gain, 453-MHz unity-gain frequency and 68° phase margin at 2-pF load. The power allocated to each OpAmp is 2.2 mW.

3.2 Pole-Controllable DOC

Figure 6 shows the pole-controllable feature of the proposed DOC. It can provide a 1-MHz cutoff to receive only the pilot tones and a 10-kHz cutoff for normal reception.

The dc-offset removability of the proposed DOC is verified through Monte-Carlo simulations. The results show that, with the DOC disabled, the standard deviation of the output-referred offset, σ_{os}, in both cases is around 7 mV. With the DOC enabled, σ_{os} in both cases is suppressed to around 3 mV, corresponding to more than 50% reduction. Such a result verifies that even if the dc-offset generated by the SC Biquad is not suppressed; the overall dc-offset performance is not degraded.

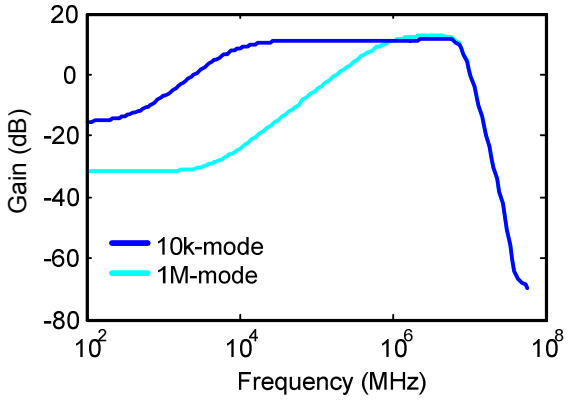

Fig. 6. Pole-controllable feature of the proposed DOC.

3.3 CT/DT Hybrid CSF versus pure CT active-*RC* CSF

Figure 7 shows the simulated frequency responses and in-band group delays of both CSFs. Since Hourglass has a faster roll-off in the transition region, a 4th-order architecture in conjunction with a passive-*RC* real pole at 14 MHz (optimized by

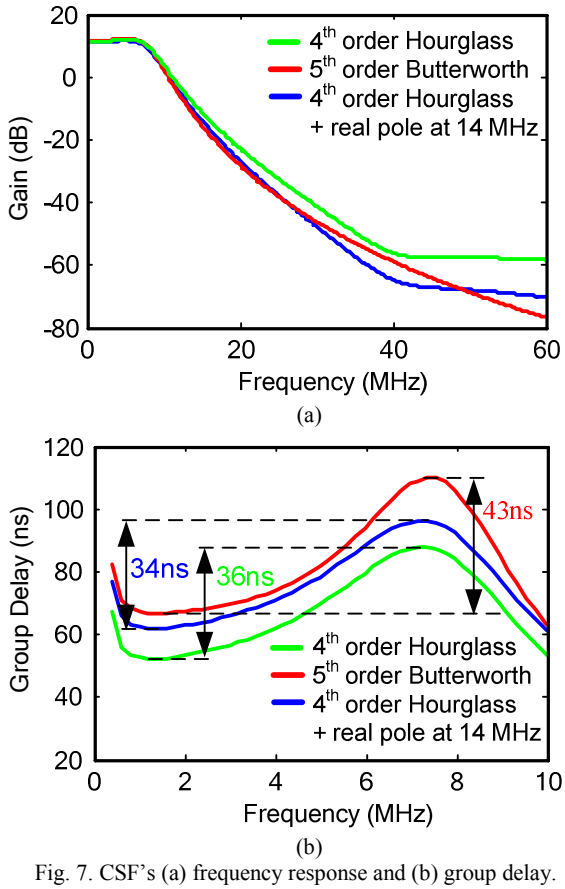

Fig. 7. CSF's (a) frequency response and (b) group delay.

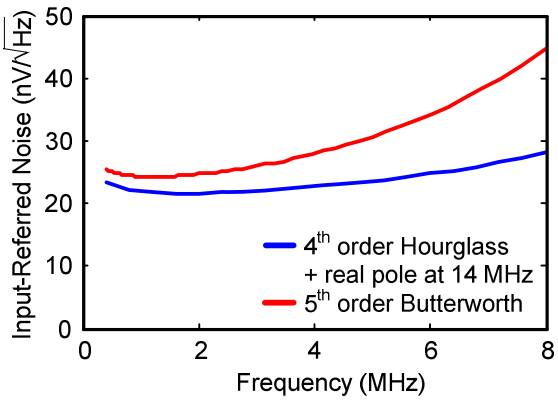

Fig. 8. Simulated noise responses of both conventional and proposed CSFs.

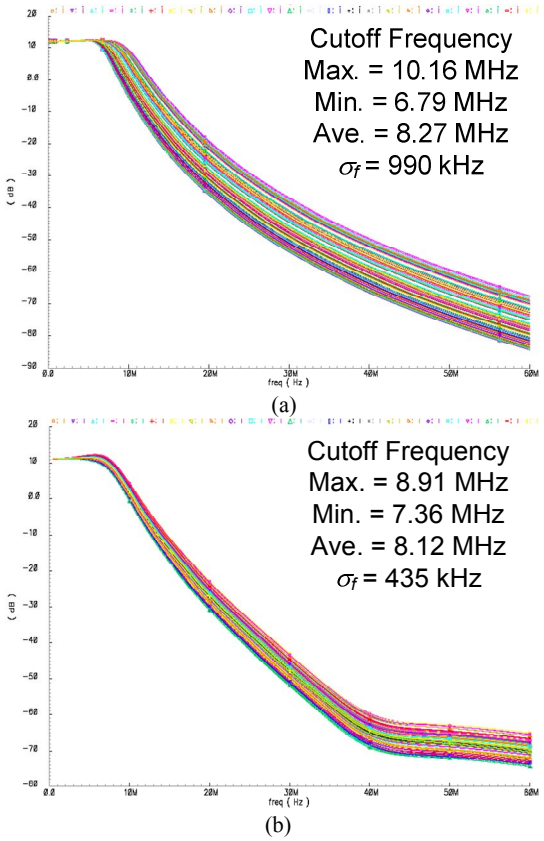

Fig. 9. Frequency responses from 100-time Monte-Carlo simulation: (a) active-*RC* CSF and (b) CT/DT hybrid CSF.

simulation) shows a stopband rejection that is comparable to a 5th-order Butterworth while offering smaller in-band group delay variation. The simulated midband gain is 11.61 dB and the stopband rejection at 20/40/60 MHz is 38.7/76.3/81.7 dB. The inband input-referred noise density of the proposed CSF is also better than that of the conventional structure, as shown in Fig. 8.

Since half of the proposed filter is SC-based, the cutoff frequency is expected to be much more stable when compared with the active-*RC* filter. Obtained through 100-time Monte-Carlo simulations, the cutoff of the proposed CSF varies 50% less than that of the active-*RC* one [i.e., σ_f in Fig. 9(a) and (b)].

Table I presents the simulations results of the proposed filter and the conventional active-*RC* filter.

Table I. Summary of the simulation results

		CT/DT Hybrid Hourglass Filter	Active-*RC* Butterworth Filter
Power Supply		1.2 V	
Power		10.3 mW	9.6 mW
In-band Group Delay Variation		34 ns	43 ns
-3-dB Cutoff Frequency	Mean (Variation)	8.12 MHz (-9.4%, +9.7%)	8.27 MHz (-17.9%, +22.9%)
	σ_f	435 kHz	990 kHz
Output-Referred Offset	σ_{os} w/o DOC	7.25 mV	7.77 mV
	σ_{os} w DOC	3.38 mV	3.28 mV
IIP3		+15 dBm	+21 dBm

4. CONCLUSIONS

This paper described a novel CT/DT hybrid CSF with a built-in pole-controllable DOC for WLAN receivers. A 4th-order Hourglass approximation with one frequency-extended real pole meets the stopband rejection specifications while offering a much more stable cutoff frequency (i.e., ±10%) and in-band group delay (i.e., 34 ns) than that of the conventional active-*RC* 5th-order Butterworth CSF. On the other hand, the adoption of the proposed DOC results in >50% reduction of the dc-offset. The DOC consumes only a small amount of power (i.e., 0.2 mW) and is minimized in area by introducing a subthreshold-biased integrator and a parallel-compensated depletion-mode MOS capacitor for the dc-offset extraction.

ACKNOWLEDGMENT

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