An SC CCIR-601 Video Restitution Filter With 13.5 Msample/S Input And 108 Msample/S Output

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1. Abstract

This paper presents a design and implementation of a low-power Switched-Capacitor filter for NTSC/PAL digital video restitution system with CCIR-601 standards. The filter which employs optimized structures including coefficient-sharing, spread-reduction, semi-offset-compensation, mismatch-shaping, double-sampling and analog multirate & multistage techniques achieves linear-phase lowpass response with 5.5-MHz bandwidth, 108 Msample/s output from 13.5 Msample/s video input and active area about 3.3 mm^2 and about 80 mW power consumption. Both behavior-, transistor- and layout-extracted level simulations will be presented for illustrating the effectiveness of the circuit in 0.35 μm CMOS technology.

2. Introduction

A high-performance and economic solution for digital video in modern consumer and professional applications entails a high integration of the large digital system with traditionally external analog interfaces on a single chip, like DVD players, TV-output in DVD-equipped PCs, PC multimedia video editing systems, digital set-top boxes, digital still cameras, video phones as well as studio and broadcast video systems and so on. However, many currently available video encoders in the market still require an external passive inductive-capacitive (LC) filter for post signal restitution filtering to the standard analog composite (NTSC or PAL) or S-video outputs for rejecting the images from the inherent sampling process in digitizing analog video [1-4]. The implementation of high-order monolithic continuous-time (C-T) filters together with phase-equalization for wideband video applications is still not straightforward and cost-efficient due to the limitation of the inherently inaccurate time-constant in current IC technology [5-6].

This paper presents the design and realization of a high-frequency, power-efficient SC filter for NTSC/PAL digital video with CCIR-601 standards, i.e., equi-ripple gain (< ±0.25 dB) & linear phase characteristics (< ±10 ns group delay variation) in 5.5 MHz passband with typically a 40 dB stopband attenuation [1-4], and with embedding an 8-fold sampling rate increase from input 13.5 MHz to the output at 108 MHz, thus allowing a very relaxed 1st-order continuous-time post filter, e.g. -3dB-frequency can be varied within ±20% around the nominal 18 MHz, thus leading to a low-cost full single-chip alternative, as shown in Fig.1.

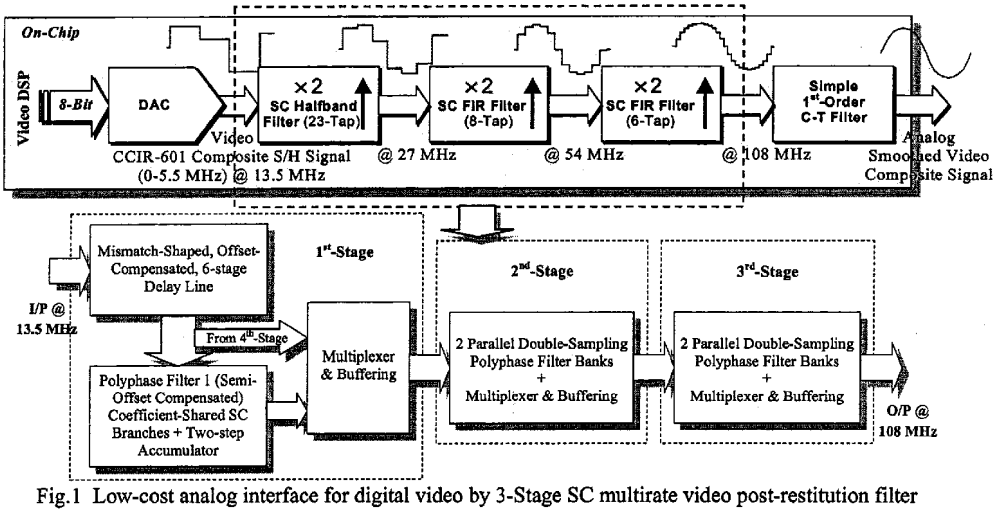

Fig.1 Low-cost analog interface for digital video by 3-Stage SC multirate video post-restitution filter

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3. Circuit Structure and Implementation

The circuit employs 3-stage multirate-FIR-polyphase-based structures [7] to achieve linear-phase, reduced sampled-and-hold shaping distortion and relaxed speed need for OTA's as well as minimized capacitance spread. The overall 3-stage circuit structure is presented in Fig.1.

The critical 1st-stage requires a high-order (23-tap) function due to its sharp-selectivity response, a delay-line-based FIR structure is used. However, in order to reduce the accumulated errors along the delay line especially the offset errors which will lead to fixed pattern noise located at lower input sampling rate and its multiples that considerably lower the SNR, autozeroing techniques with embedding mismatch-free property are employed for offset compensation and 1/f noise reduction in the 1st-stage. The number of delay line has also been optimized from original about 20 to only 6 for reducing the power, accumulated gain and phase errors using rotating-switch multirate delay and halfband filtering schemes with consideration of autozeroing and coefficient-sharing discussed below.

Especially, some less-sensitive SC coefficient branches are not implemented in autozeroing and coefficient sharing in order to reduce the number of delay block or OTA's by using parallel structure, and the simulations show that their resulting errors are within the circuit tolerance. Coefficient-sharing with together half-band filtering techniques [8], which significantly relax the area and power consumption, are implemented in 1st-stage for those mismatch-sensitive and large coefficients. This has been illustrated in Fig.2. Besides, the split-summing-capacitor and two-step accumulation schemes are also employed for further reduction of capacitance spread, so that the final optimized spread when taking into account of the use of 3-stage multirate structure is only 20 comparing to the original more than 2000.

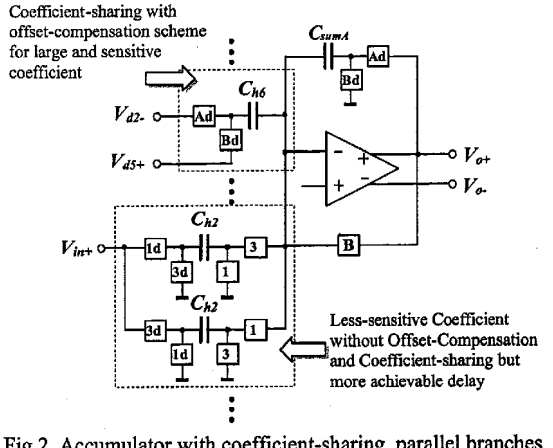

Fig.2 Accumulator with coefficient-sharing, parallel branches and autozeroing in the 1st-stage

Having lower filter order in the 2nd and 3rd stages, we used here both the sole parallel multi-unit-delay SC branches instead of active delay line to minimize the power. With the employment of 2-parallel polyphase structure plus also double-sampling in each stage, their OTA speed is significantly relaxed, thus maximizing the power saving.

Special mismatch-free SC multiplexers [7] are employed for interfacing different stages and providing enough driving capability, and they are actually not the power-hungry one due to the increased feedback factor and reduced slew rate requirements, even through they operate at higher output sampling rate.

Fully-differential structures are utilized for reducing common-mode noise coupling especially from the multiple clock generator. And together with the phase-delayed sampling scheme, the signal-dependent clock feedthrough & charge injection errors will be minimized.

The single-stage telescopic OTA structure with wide-swing biasing circuitry is adopted here for its superior high-speed and low-power capability, as shown in Fig.3. The common-mode voltage is stabilized at 1.1 V by a dynamic SC common-mode feedback circuit. The fastest OTA achieves 70 dB gain, 302 MHz GBW with 64° PM at 4 pF capacitor loading, and 6.5 ns settling time and occupies 6.6 mW of power from layout-extracted Cadence simulation results.

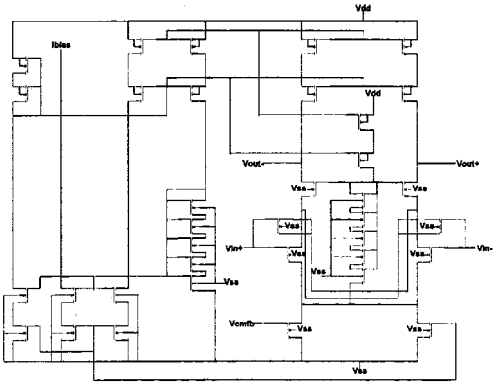

Fig.3 OTA schematic

Digital phase generation network whose block diagram is shown in Fig.4 needs to provide totally 44 phases including fall-time delayed version. Robust synchronization among submasters and all multiple phase outputs with different period was achieved by optimized logic structures, so that the systematic mismatches could only happen in the phase-width control and buffer circuitry. Monte-carlo HSPICE simulations show that the time skews are smaller than 100ps which result the unwanted images due to the non-uniformly sampling that overlap onto the attenuated signal bands all below –55 dB.

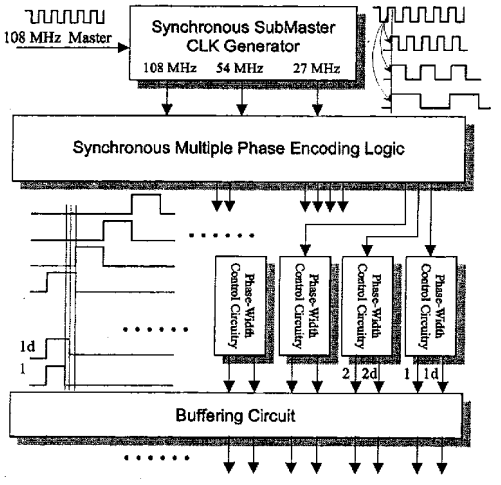

Fig.4 Multiple phase generation block diagram

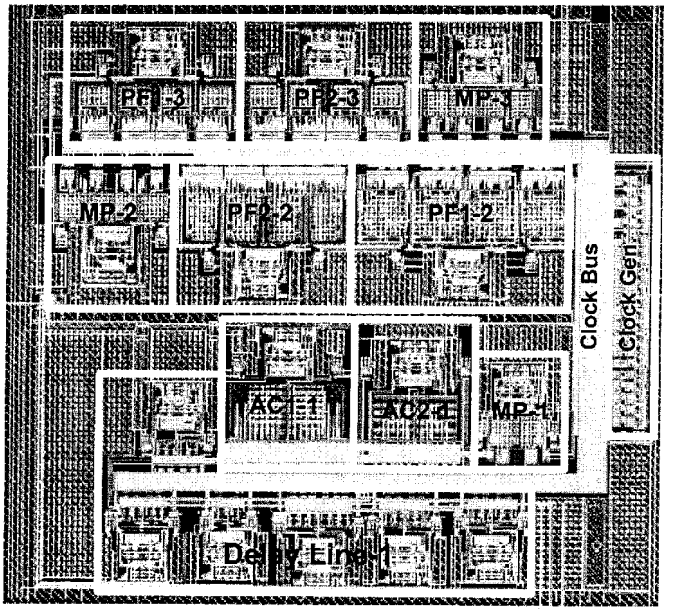

Fig.5 Circuit Layout (AC-Accumulator, PF-Polyphase Filter, MP-Multiplexer)

4. Circuit layout

The circuit has been designed and implemented by using 0.35 μm double-poly triple-metal CMOS technology. Special cares including common-centroid plus dummy periphery and mirror-symmetrical arrangements have been taken for the mismatch-sensitive analog parts, like OTA differential pair, critical capacitor group. Separate analog and digital VDD supplies but with same shared ground, which biases the whole chip substrate with ample substrate contacts, in addition to the on-chip decoupling are employed to reduce the power supply noise caused by inductive package. This leads to that all signals inside the chip will now refer to the same ground and, more importantly, the return currents due to the clock signal transferring between digital and analog parts which are the most current-spike-consumed part of SC filters will be flowed inside the chip rather than through the inductive package.

In addition, Shielding by lower layer or N-well is widely used in the layout for either sensitive analog signal or noisy digital clock lines. On-chip MOS capacitors between VDD and ground are inserted in any empty area for having enough decoupling capacitance which are approximately counted about 1.5 nF. The overall circuit layout is shown in Fig.5 with active area about 3.3 mm^2 including both analog and digital parts.

5. Simulation results

To evaluate the random capacitance coefficient mismatch errors, Monte-Carlo amplitude simulation for capacitance ratio being independent zero-mean Gaussian random variables with the deviation within 1.5 % has been performed and the results are shown in Fig.6a. It shows that the upper and lower bound deviation in passband are within the desired ±0.25 dB including the output S/H shaping effect, and the unwanted image bands located at 13.5 MHz, 27 MHz, 54 MHz have been all attenuated by the 1st-, 2nd- & 3rd-stage subsequently greater than 40 dB.

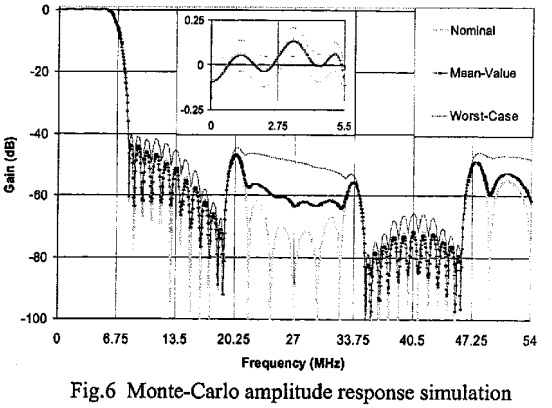

Fig.6 Monte-Carlo amplitude response simulation

The circuit have also verified by the transistor-level Periodic Swept Steady-State (PSS) AC analysis from SpectreS simulation from Cadence, and the responses for the 1st and last 2 stages (2nd+3rd) which are presented in Fig.7 show that the circuit meets well the specifications.

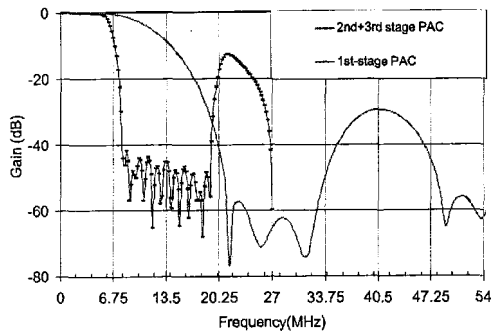

Fig.7 Periodic swept steady-state AC (PAC) response from transistor-level Simulation

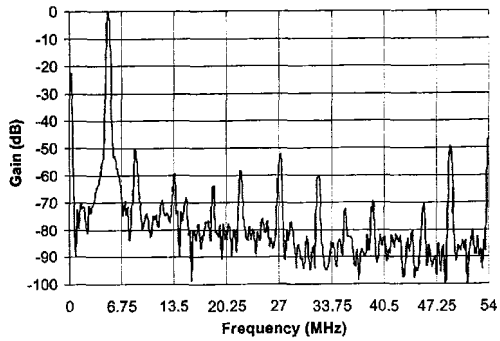

Fig.8 Spectrum of 5 MHz @ 108 MHz output signal from the worst-case transistor-level simulation

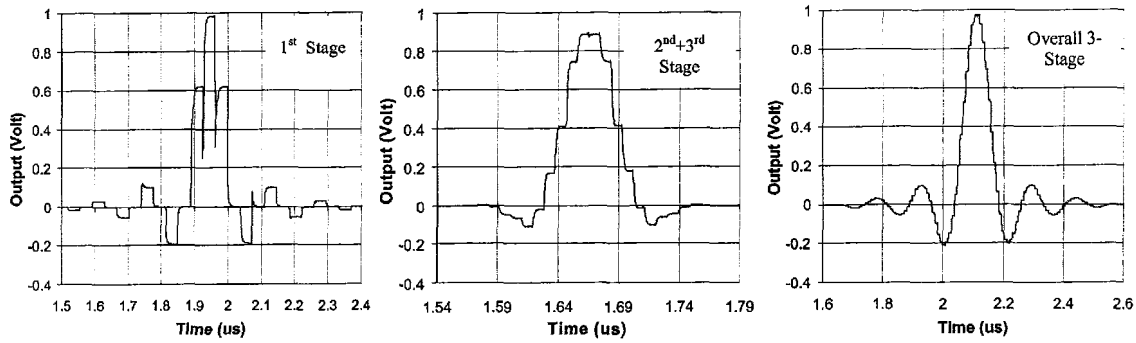

Fig.9 Impulse transient response from layout-extracted simulation

Fig. 8 presents the spectrum of 108 Msample/s output signal from the 3-stage SC filter with a 5 MHz, 1.3Vp-p, 13.5 Msample/s input. The result is obtained from FFT of the worst-case transistor-level transient simulation with OTA transistors sized with Monte-Calro mismatches at max. 6 %. It is obvious that the unwanted images of input baseband signal and the fixed pattern noise tones around 13.5, 27 and 54 MHz have been supressed below 45dB, and the rest spurs are the frequency translated-images of the harmonics sampling at different input & output rates and their multiples which result THD still below –60 dB.

Fig.9 are the impulse transient responses of 1st-, 2nd+3rd stage and the whole system obtained from the layout-extracted simulations. They show clearly achieved 23-tap half-band, 8-tap and 6-tap as well as overall 3-stage symmetrical impulse response of the SC FIR system.

6. Conclusions

An efficient structure, design and implementation of a 13.5 Msample/s to 108 Msample/s 3-stage upsampling SC linear-phase FIR filter for post image rejection of CCIR-601 NTSC/PAL digital video has been presented. Special issues for deigning this high-frequency SC filter have been addressed and validated on the basis of behavioral-, transistor- and layout-extracted level simulations. The circuit, implemented with 0.35 μm CMOS, consumes an active area of 3.3 mm^2, and 50 mW static analog and 30 mW average digital power at 3V supply, which is attractive when compared to more than 300 mW in typical analog video filter products [6,9].

7. Reference

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